Splitter for EPD as FCS Preshower

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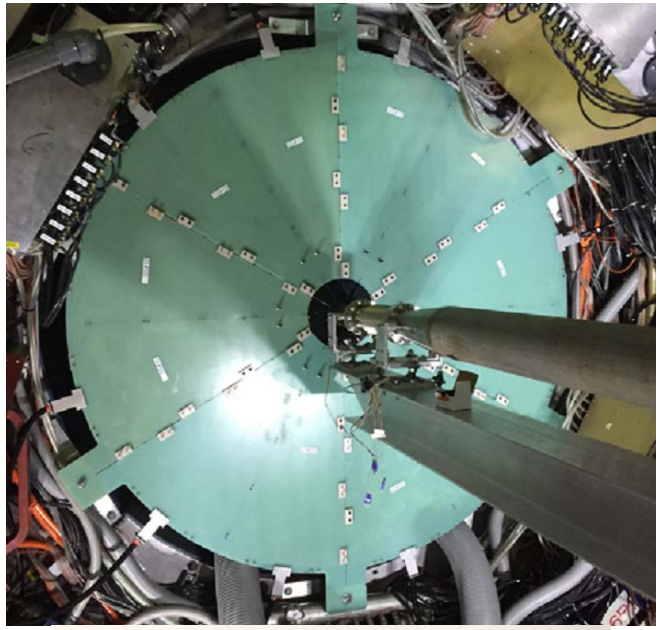
Reminder on the West EPD

tiles: 372, 24 (ϕ) × 15 (η) + 12 more (ϕ) near the beamline
FEE: NW and SW boxes, 12 boards each, 16 ch/board



J. Adams, A. Ewigleben, S. Garrett et al. *Nuclear Inst. and Methods in Physics Research, A 968 (2020) 163970*

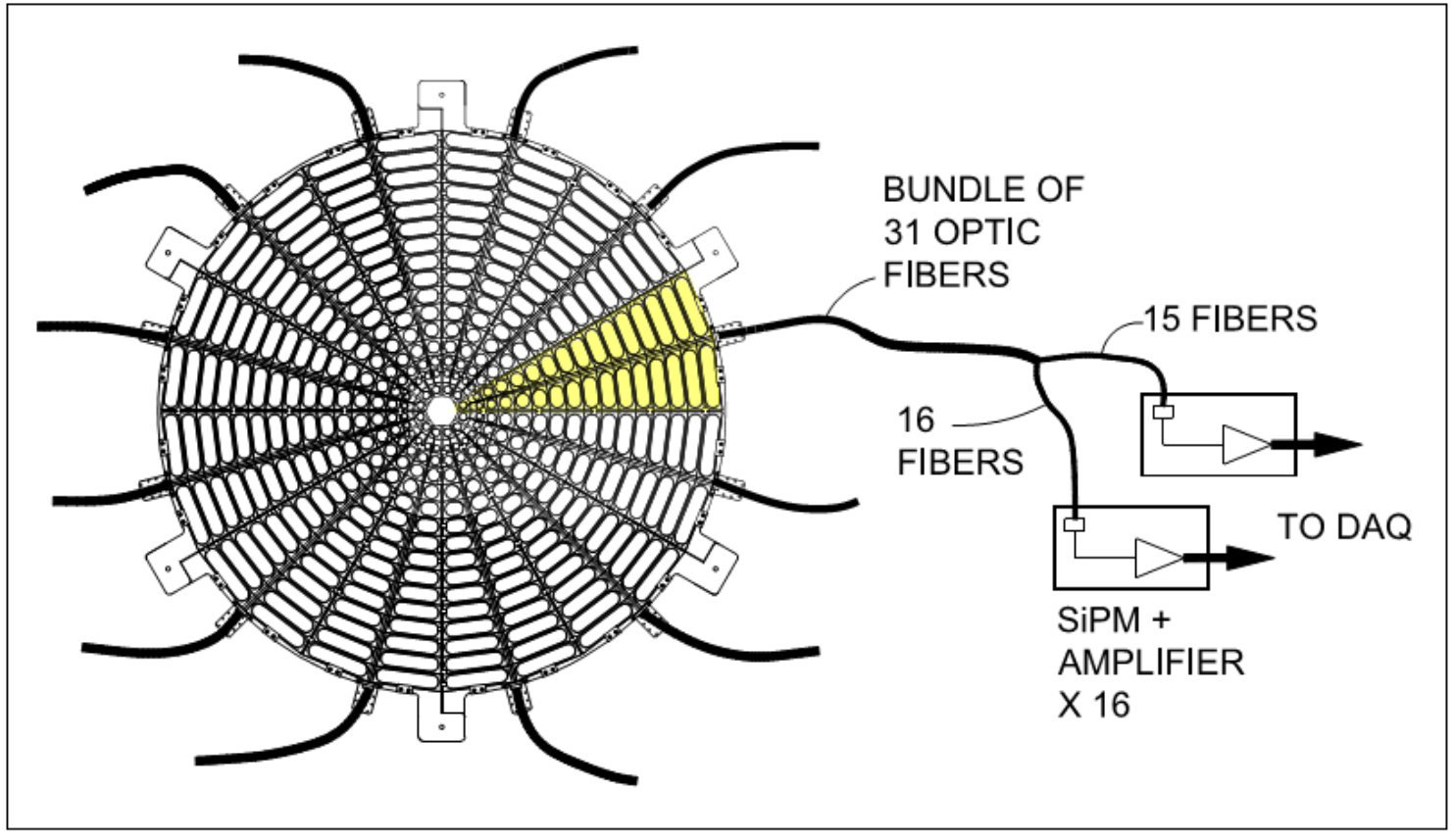
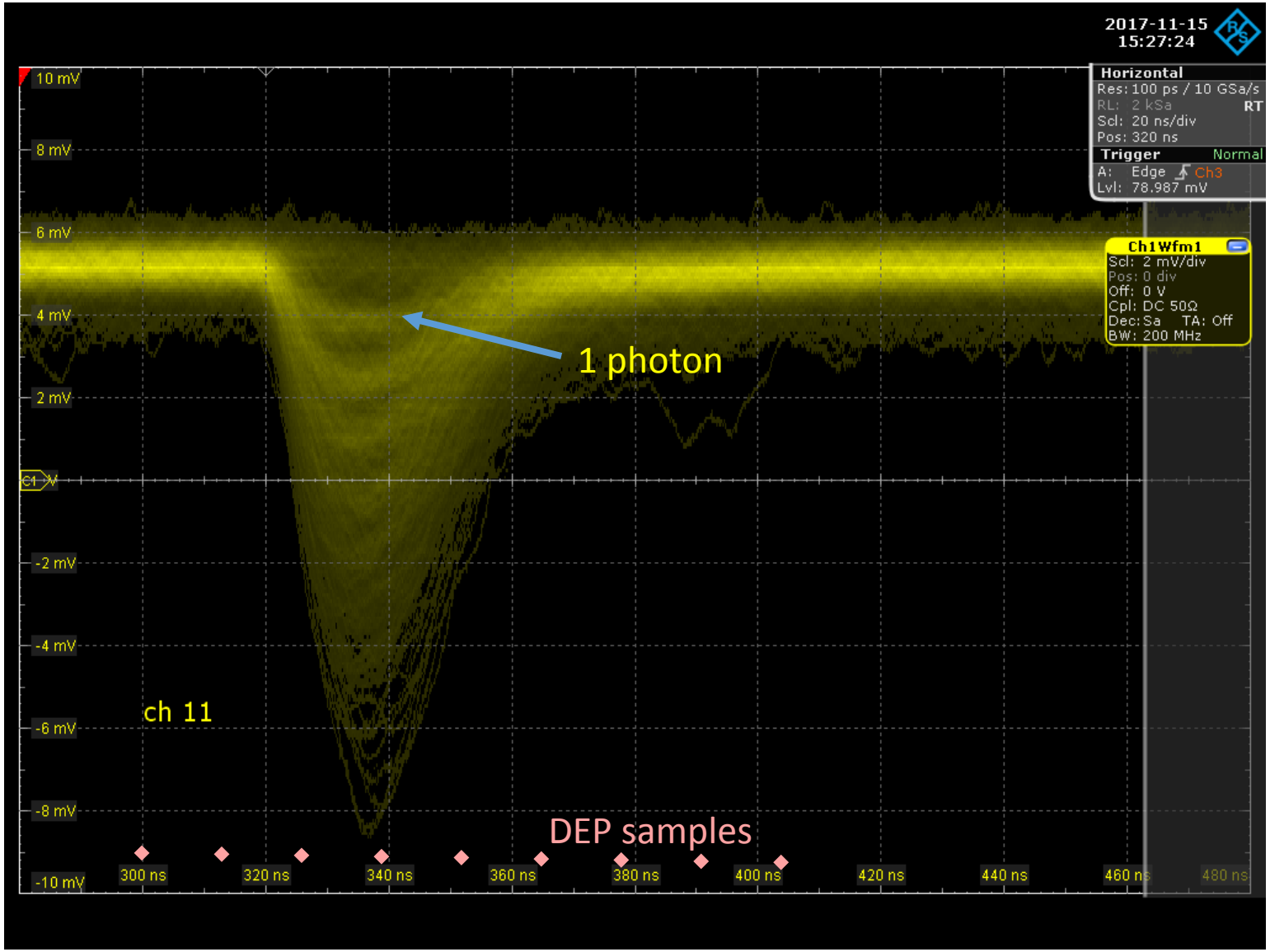


Fig. 1. A sketch of the EPD system. One of two EPD wheels is shown. The 31 tiles from each of 12 supersectors are connected via optical fiber bundles to silicon photomultipliers and amplification electronics. See text for details.

Reminder on the West EPD

signals (as seen by QT – *signals on MDR cable are slightly faster…*)



It was made about as fast as possible due to limitations of QT readout (gate width and imperfections).

It is probably too fast for DEP readout.

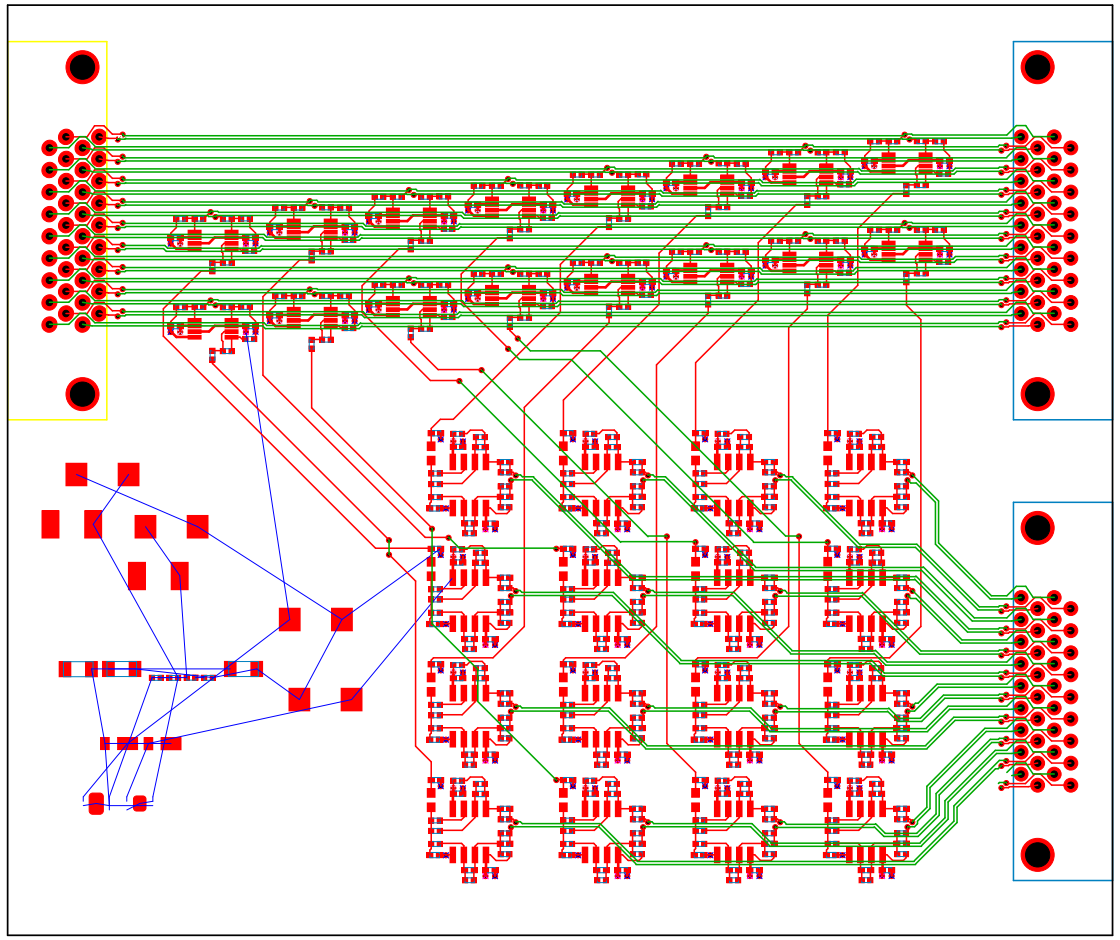
Splitter Requirements

- **Not to impair or significantly alter** the signals from EPD FEE to EPD readout
  - especially not to be sensitive to FCS running or not, DEP connections / power
  - inevitably, **splitter power does matter** though, so we have to be careful with that
    - take from EPD rack, under EPD group's control?
- Copy the signals from all west EPD channels to inputs to DEP for FCS trigger and readout
- Probably have to shape the signals little slower suitable for DEP sampling
  - otherwise no crisp hit threshold is possible, and efficiency may suffer
- 16 (or N×16) channels per board, same MDR connectors and pinout
  - note that FCS pinout is the same as EPD pinout which was based on FMS-POST pinout, so this is all sane actually by default
- and the usual: low cost, super reliable, easily serviceable, safety requirements, etc.

and

- For run 21 test installation only: Delay should be as small as possible! Since it adds skew between signals in same QT
  - Rosi informs us "We discussed this a bit in the EPD meeting today – we think that probably the 5 ns will be fine and that any changes that might result can be taken care of in the calibration of the data."

Current status



- Signal path schematic and layout 100% complete
- Power (and monitoring?) circuits to do still
- Board size defined (12.7 × 10.7 cm), mounting plan TBD
- 6 layer PCB (2 signal, 4 power/ground)
- Component values for gain & shaping are placeholders, TBD; some prototyping needed
- PCB's can be ordered in parallel with component value decisions

- Probably best to buy all (24 + 4 spare) PCB's, cost will be >50% higher to order 3 and 25 later
- We'll assemble 3 boards to install 2 in run 21 test
- **Two short (or extra-short) cables to be ordered asap**
- **Two long cables to be installed preferably before close-up for the run**