Vertexing and Tracking

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IR2@EIC workshop

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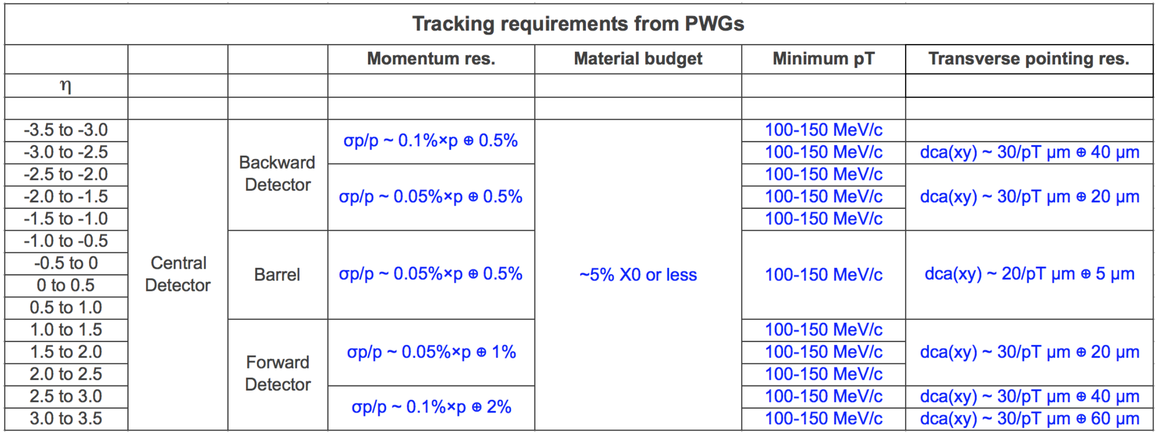
Vertex and tracking at EIC

- All proposed EIC detector concepts are equipped with a vertex and tracking detector as their innermost element

- A well integrated, large acceptance vertex and tracking detector designed with high granularity and low material budget is needed to enable high precision measurements that are key to the EIC science programme

- The tracking and vertexing systems under consideration are based on semiconductor detector technologies and gaseous tracking detector technologies, with concept combining both technologies
  - This talk focuses on the silicon vertex and tracking (SVT) technology for the central detector (barrel + backward/forward)

Tracking requirements from physics



Tracking requirements from PWGs

η			Momentum res.	Material budget	Minimum pT	Transverse pointing res.
-3.5 to -3.0	Central Detector	Backward Detector	σp/p ~ 0.1%×p ⊕ 0.5%	~5% X0 or less	100-150 MeV/c	
-3.0 to -2.5					100-150 MeV/c	dca(xy) ~ 30/pT µm ⊕ 40 µm
-2.5 to -2.0			σp/p ~ 0.05%×p ⊕ 0.5%		100-150 MeV/c	dca(xy) ~ 30/pT µm ⊕ 20 µm
-2.0 to -1.5					100-150 MeV/c	
-1.5 to -1.0					100-150 MeV/c	
-1.0 to -0.5		Barrel	σp/p ~ 0.05%×p ⊕ 0.5%		100-150 MeV/c	dca(xy) ~ 20/pT µm ⊕ 5 µm
-0.5 to 0						
0 to 0.5						
0.5 to 1.0						
1.0 to 1.5		Forward Detector	σp/p ~ 0.05%×p ⊕ 1%		100-150 MeV/c	dca(xy) ~ 30/pT µm ⊕ 20 µm
1.5 to 2.0					100-150 MeV/c	
2.0 to 2.5					100-150 MeV/c	
2.5 to 3.0			σp/p ~ 0.1%×p ⊕ 2%		100-150 MeV/c	dca(xy) ~ 30/pT µm ⊕ 40 µm
3.0 to 3.5					100-150 MeV/c	dca(xy) ~ 30/pT µm ⊕ 60 µm

From YR 11.2.2 at arXiv:2103.05419

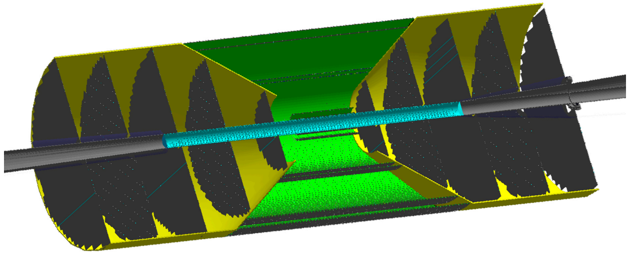
- Spatial resolution: ~5 μm (20 μm pixel pitch)
  - ~3 μm in the vertex layers (10 μm pixel pitch)
- Material budget: <0.3% X/X0 per layer
  - < 0.1% X/X0 per vertex layer
- Integration time ~2 μs
- Low power consumption
  - i.e. air cooling desirable for low material budget

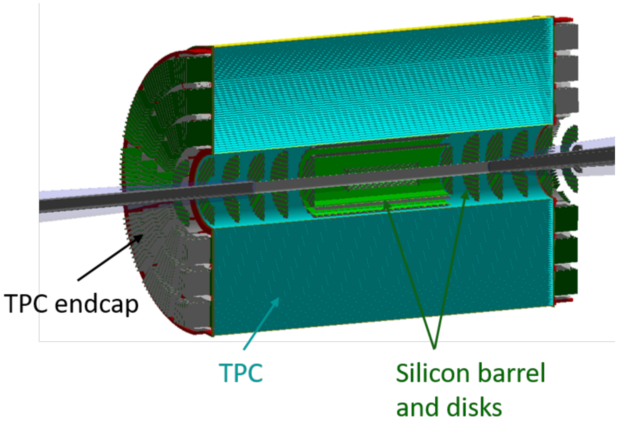
Requirements driven technology choice:
Monolithic Active Pixel Sensors (MAPS)

See L. Gonella, https://indico.bnl.gov/event/7449/contributions/35954/
1st EIC Yellow Report Workshop at Temple University (2020)

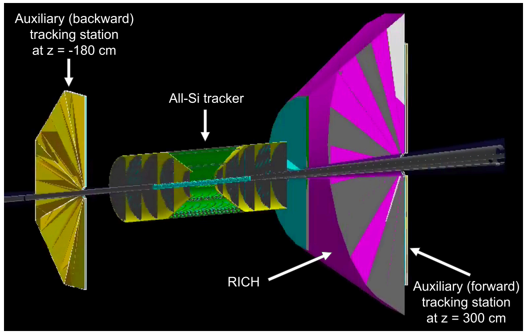
YR concepts based on MAPS SVT detector

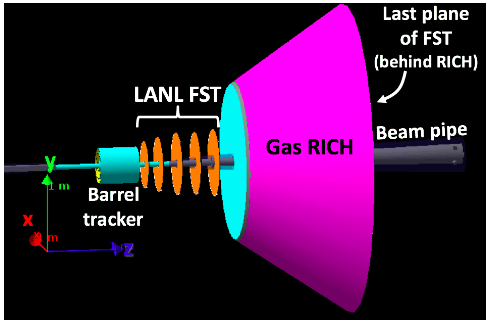
- YR baseline concepts
  - All-silicon and hybrid (MAPS + TPC)

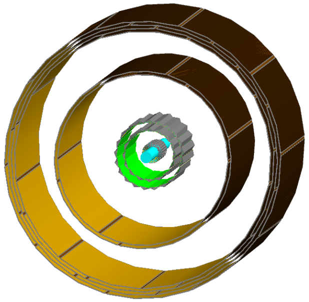




- Alternative tracking options exist in the backward and forward tracking regions, also MPGD based barrel







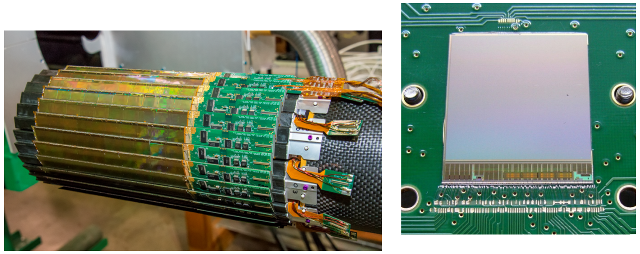
For more details see YR 11.2 at arXiv:2103.05419

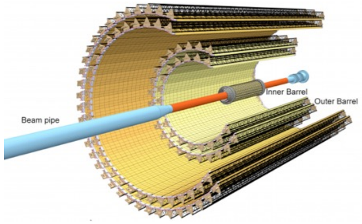
The MAPS technology to satisfy the requirements of the central detector can be the same for different EIC detector configurations

MAPS detectors

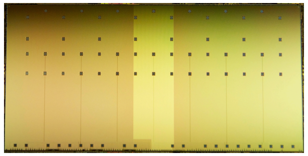
Experiment ready MAPS (i.e. production version exists)

MIMOSA 28 @ STAR HFT

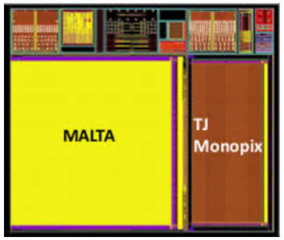




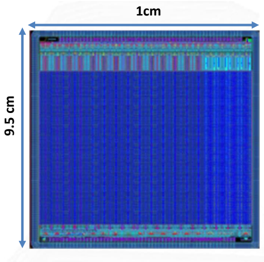
ALPIDE @ ALICE ITS



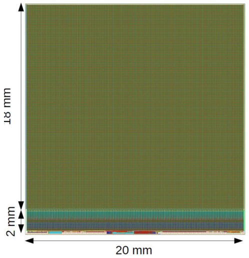
Depleted MAPS (i.e. HV/HR-CMOS) prototypes



MALTA and TJ-MONOPIX
180 nm TJ

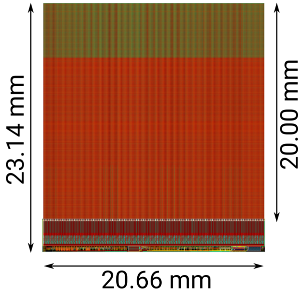


LF-MONOPIX
150 nm LFoundry



ATLASPix3
180 nm TSI

MuPix10
(soon @ Mu3e)



and more…

For a more detailed discussion see YR 11.2.3 at arXiv:2103.05419

None of the existing MAPS sensors meets all the requirements at once.
A dedicated EIC MAPS sensor is the desired solution.

New generation MAPS in 65 nm CMOS imaging technology

- A large effort is emerging to develop new generation MAPS in a commercial 65 nm CMOS imaging technology
- Large interest in the HEP community to develop this process for future experiments: CERN EP R&D programme and ALICE ITS3 project

- Improved performance in terms of granularity and power consumption that are key for precision measurements at the EIC
  - Demonstrated in simulation
- Process availability on the EIC project timescale
- Possibility to leverage on the ALICE ITS3 project
  - The ITS3 sensor specifications and development timescale are largely compatible with those of the EIC
  - EIC vertex layers could be a copy of the ITS3 detectors

Strategy:
Join the ALICE ITS3 collaboration to develop an EIC MAPS sensors in 65 nm CMOS imaging technology

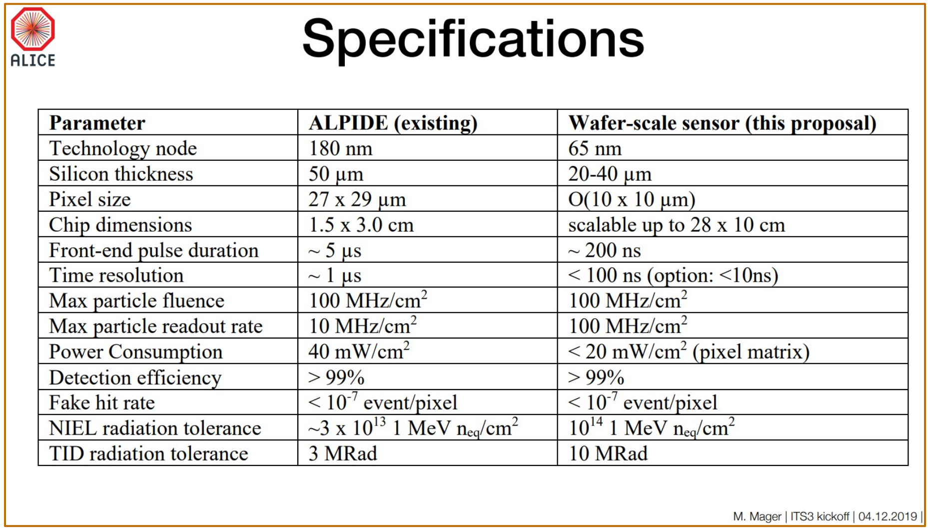
See L. Greiner, https://indico.jlab.org/event/348/sessions/1224/attachments/4665/5789/open-mic.pdf
EIC Yellow Report Kick-Off meeting (2019)

ALICE ITS3 sensor

- The ALICE ITS3 project aims at developing a new generation MAPS sensor at the 65 nm node with extremely low mass for the LHC Run4 (HL-LHC)

ITS3 sensor

- Specifications meet or even exceed the EIC requirements
- Higher granularity (10 µm pixel pitch) and lower power consumption (<20mW/cm^2) with respect to pre-CD0 simulation baseline (that was ITS2/ALPIDE derived)
- Also, integration time, fake hit rate and time resolution better than required at the EIC
- ITS3 fallback solution: new MAPS sensor in 180 nm CMOS imaging technology



Specifications

Parameter	**ALPIDE (existing)**	**Wafer-scale sensor (this proposal)**
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

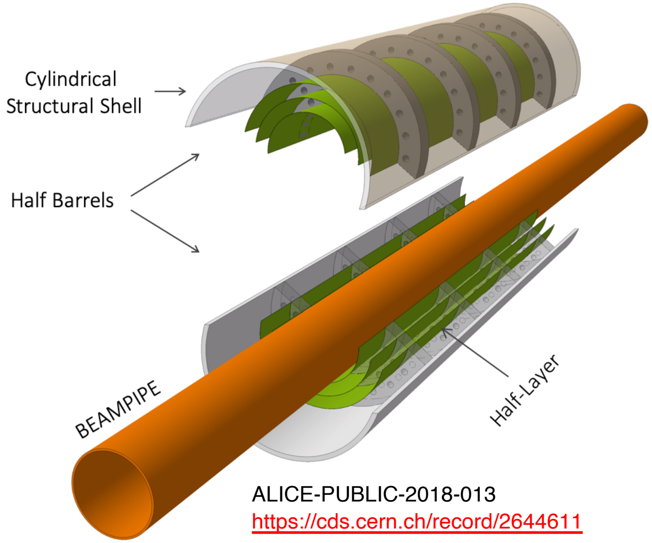
M. Mager | ITS3 kickoff | 04.12.2019 |

ALICE ITS3 detector concept

- In addition to the sensor, the ITS3 detector concept is very attractive for the vertex layers of an EIC SVT detector

<u>ITS3 detector concept</u>

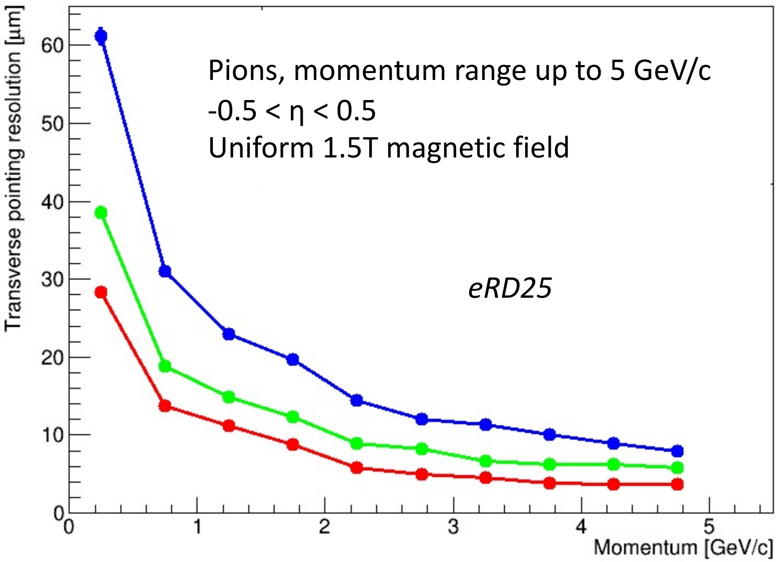
- Three layers vertex detector, 0.12 m^2
- Truly cylindrical layers
- Design and post-processing techniques to reach an extremely low material budget of 0.05% X/X0 per layer
- Low power, wafer-scale sensor, thinned to 20-40 μm, bent around the beam pipe = air-cooling, support and services outside active area



ALICE-PUBLIC-2018-013
https://cds.cern.ch/record/2644611

Simulation driven technology choice

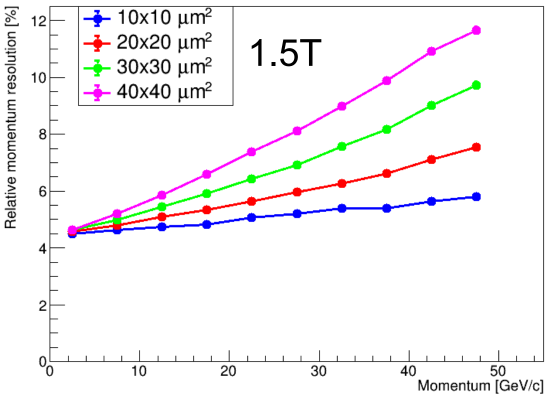
- Initial simulations showed
  - The need for ITS3 like spatial resolution and material budget to reach required vertex resolution

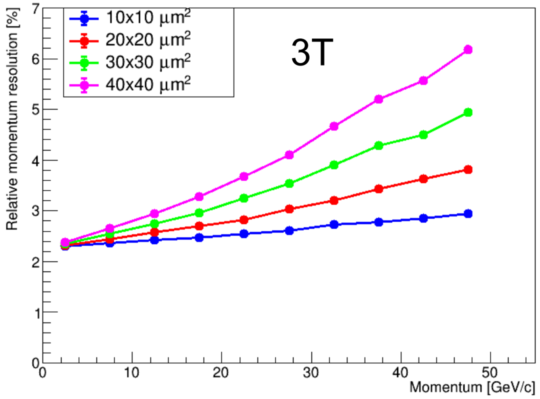


	Green	Blue	Red (ITS3 derived EIC SVT)
Beam pipe radius [mm]	18	**31**	**31**
x/X0 vertex	0.3%	0.3%	**0.05%**
x/X0 tracking layers	0.8%	0.8%	0.8%
Pixel pitch [um]	20	20	**10**

A beam pipe radius of 18 mm and a pixel pitch of 20 um were used in pre-CD0 simulations. Note that a pixel pitch of 20 um is not the ALPIDE, ALPIDE has ~28um pitch. Here binary readout is assumed so the spatial resolution is ~ 6 um (20 um pitch) and ~ 3 um (10 um pitch).

  - Momentum resolution at large eta also strongly affected by spatial resolution





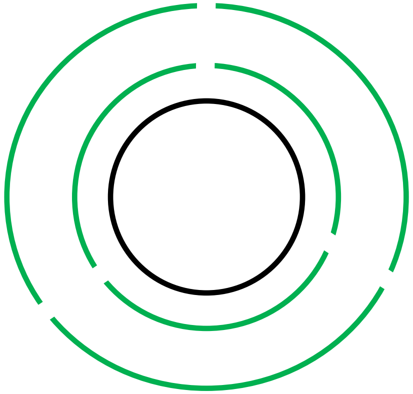
Forward region studied; η = 3
Single electrons fired from centre
Magnetic field: uniform 1.5 T and 3 T
Vertex layers and disks: 0.3% x/X0
Tracking layers: 0.8% x/X0
Beam pipe radius: 18 mm

See H. Wennlöf at https://indico.jlab.org/event/400/contributions/6529/ and http://cern.ch/go/xKk6

ITS3-derived EIC SVT

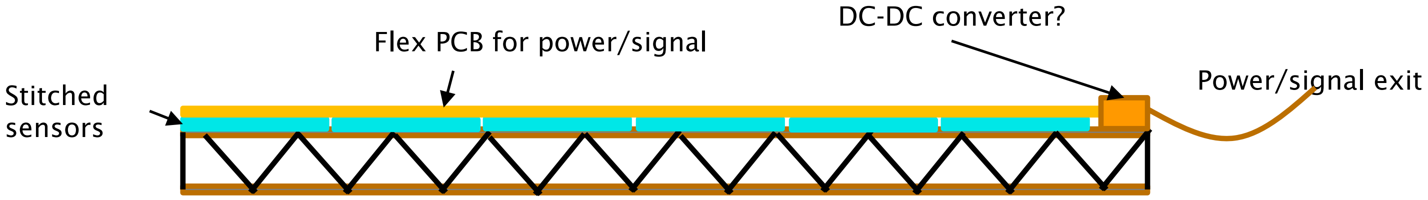
- Vertexing inner layers
  - Use ITS3 sensor
  - Adapt ITS3 detector concept to different length and radii of the EIC vertex layers

EIC strawman design (modification of ITS3)



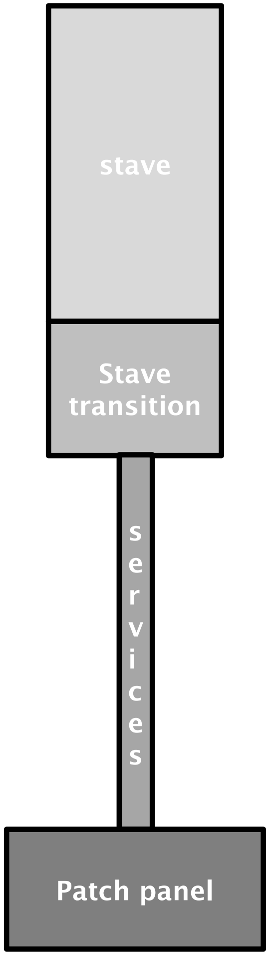
Reach larger radii by using 3 bent sections. Services exit from both sides of inner layers.

- Tracking layers and disks
  - Staves and discs will be based on a forked EIC specific sensor design based on the ITS3 sensor
    - The primary concern is yield for long rows of stitched sensors. The plan is to assess yield in the first engineering run and adjust the EIC sensors to optimize yield for the number of stitched sensors in a row.
  - Staves and disks will need to optimize the stitched sensor layout on the wafers to provide the right number of stitched sensor lengths to give the proper needed lengths for each stave/disc. This needs study and optimization.



Stave support structure

ITS3-derived EIC SVT – Material budget estimates



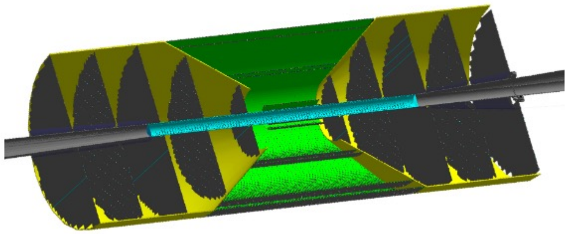
	Stave X/X0	Stave transition (per 100 cm^2 of Si surface)	Services (per 100 cm^2 of Si surface)	Patch panel (per 100 cm^2 of Si surface)
ITS3 like vertexing	~0.1%	6.66 cm^3 of material with X/X0 of 0.0684 per traversed cm	2.96 cm^2 cross section with X/X0 of 0.022 per traversed cm	4.32 cm x 1cm x 1 cm with 0.102 X/X0 per traversed cm
ITS3 like barrel (up to 1.5m length)	0.55 %	4.286 cm^3 of material with X/X0 of 0.0684 per traversed cm	1.905 cm^2 cross section with X/X0 of 0.022 per traversed cm	2.778cm x 1cm x 1 cm with 0.102 X/X0 per traversed cm
ITS3 like disc (up to 60 cm diameter)	0.24%	6.66 cm^3 of material with X/X0 of 0.0684 per traversed cm	2.96 cm^2 cross section with X/X0 of 0.022 per traversed cm	4.321 cm x 1cm x 1 cm with 0.102 X/X0 per traversed cm

Update on L. Greiner, https://indico.bnl.gov/event/8231/contributions/37955/
2nd EIC Yellow Report Workshop at Pavia University (2020)

YR baseline SVT concepts

- The YR baseline concepts are based on the ITS3-derived EIC SVT
  - Beam pipe for both is a beryllium cylinder of radius of 3.17 cm and thickness of 760 µm

- All-silicon concept



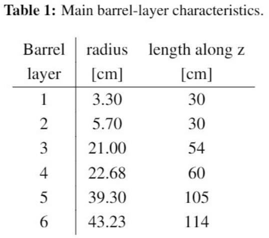


Table 1: Main barrel-layer characteristics.

Barrel layer	radius [cm]	length along z [cm]
1	3.30	30
2	5.70	30
3	21.00	54
4	22.68	60
5	39.30	105
6	43.23	114

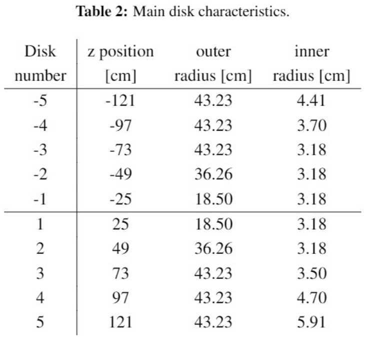
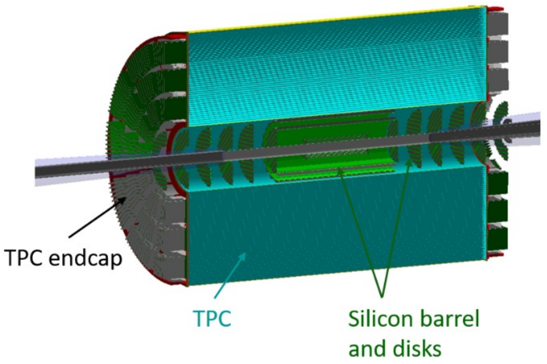


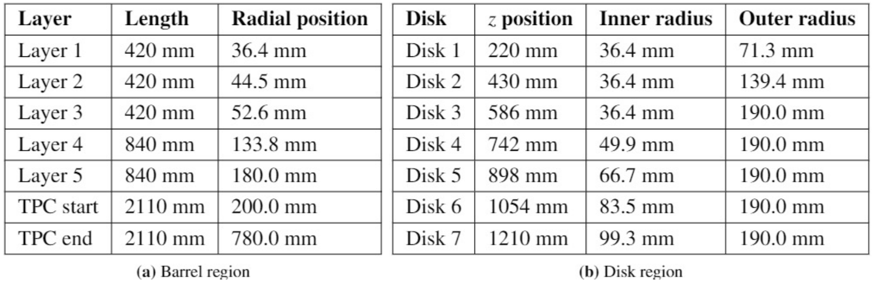
Table 2: Main disk characteristics.

Disk number	z position [cm]	outer radius [cm]	inner radius [cm]
-5	-121	43.23	4.41
-4	-97	43.23	3.70
-3	-73	43.23	3.18
-2	-49	36.26	3.18
-1	-25	18.50	3.18
1	25	18.50	3.18
2	49	36.26	3.18
3	73	43.23	3.50
4	97	43.23	4.70
5	121	43.23	5.91

x/X0 vertex	0.3%
x/X0 tracking layers	0.3%
x/X0 disks	0.3%
Pixel pitch [um]	10

- Hybrid: Silicon + gaseous detector tracking (TPC)





Layer	Length	Radial position
Layer 1	420 mm	36.4 mm
Layer 2	420 mm	44.5 mm
Layer 3	420 mm	52.6 mm
Layer 4	840 mm	133.8 mm
Layer 5	840 mm	180.0 mm
TPC start	2110 mm	200.0 mm
TPC end	2110 mm	780.0 mm

(a) Barrel region

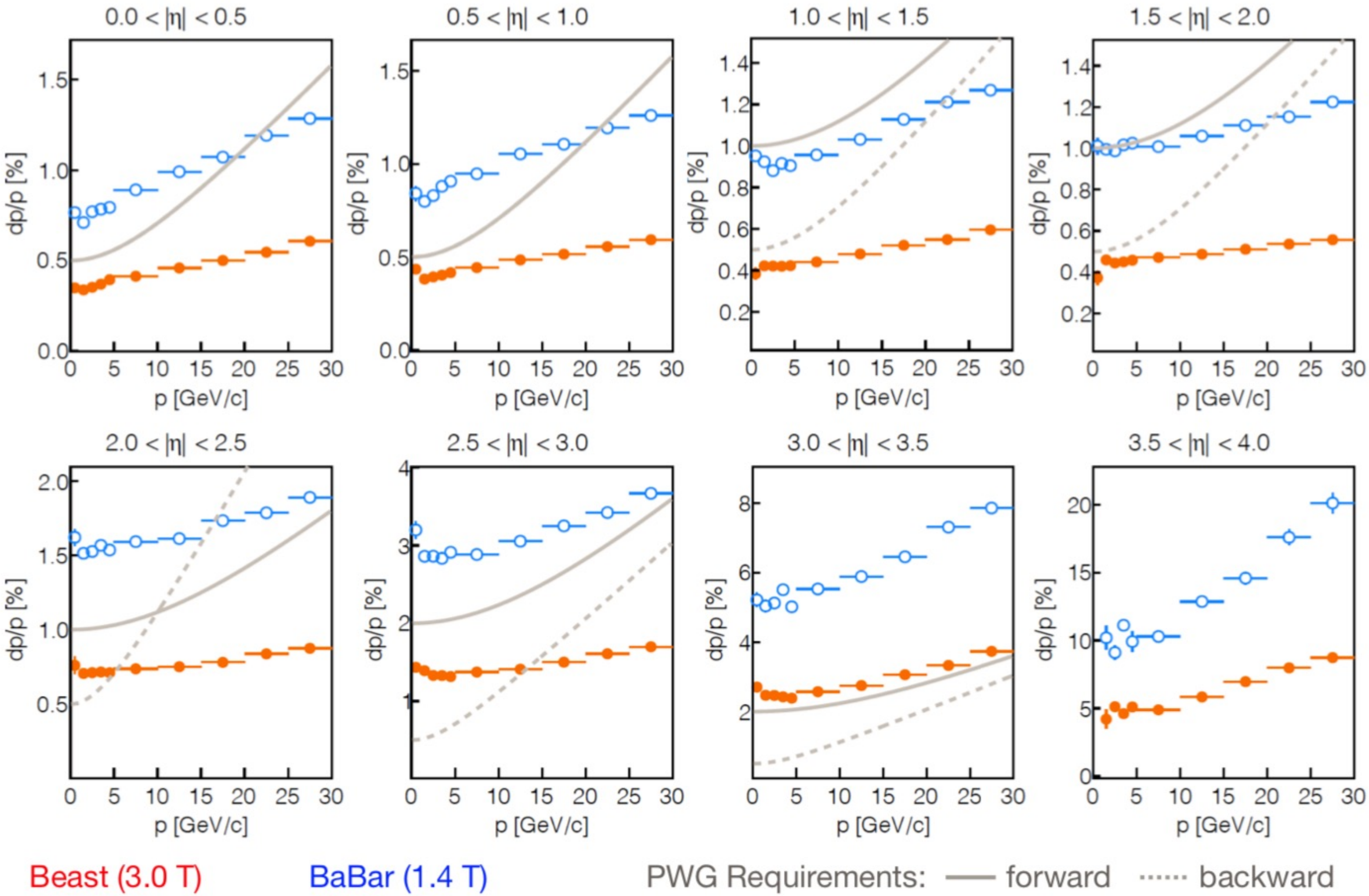
Disk	*z* position	Inner radius	Outer radius
Disk 1	220 mm	36.4 mm	71.3 mm
Disk 2	430 mm	36.4 mm	139.4 mm
Disk 3	586 mm	36.4 mm	190.0 mm
Disk 4	742 mm	49.9 mm	190.0 mm
Disk 5	898 mm	66.7 mm	190.0 mm
Disk 6	1054 mm	83.5 mm	190.0 mm
Disk 7	1210 mm	99.3 mm	190.0 mm

(b) Disk region

x/X0 vertex	0.05%
x/X0 tracking layers	0.55%
x/X0 disks	0.24%
Pixel pitch [um]	10

For more details see YR 11.2 at arXiv:2103.05419

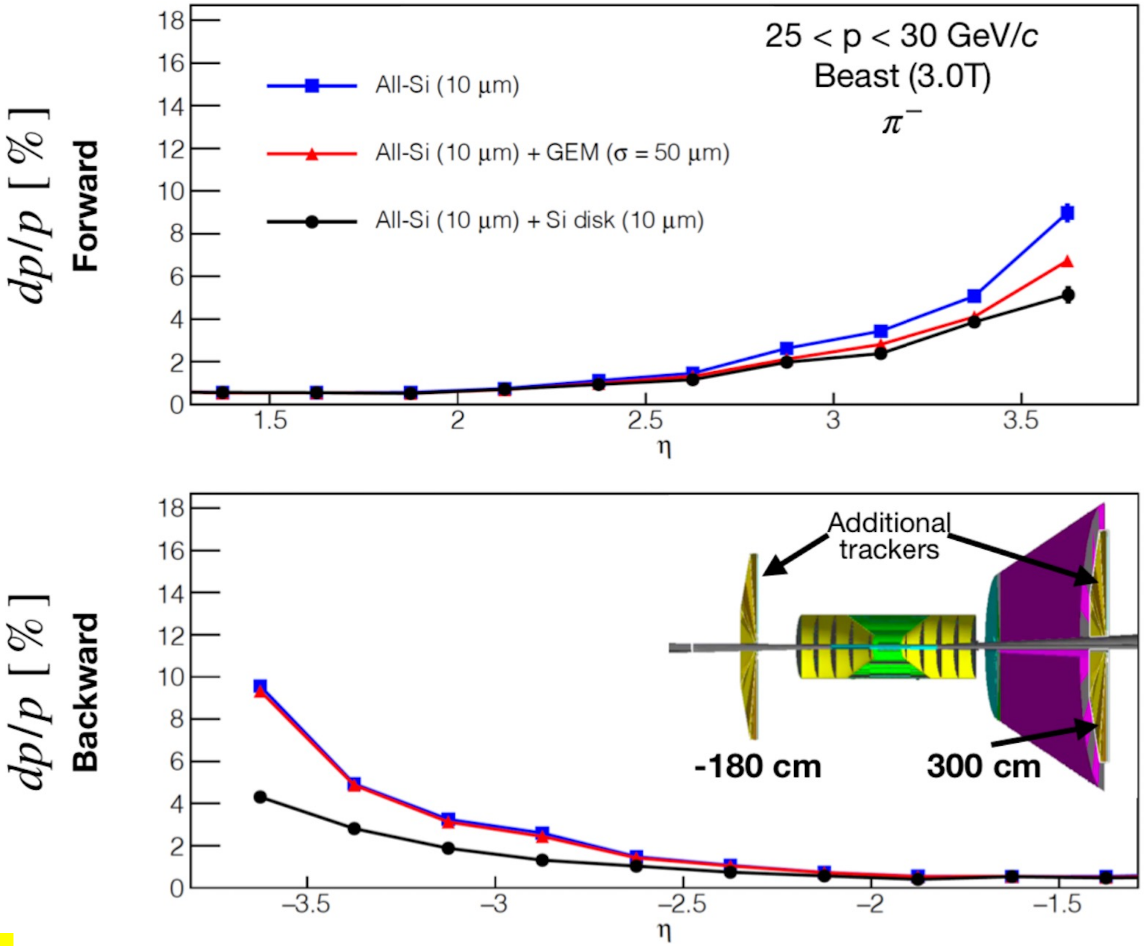
All-Silicon Concept - YR momentum resolution



R. Cruz-Torres

All-Silicon Concept - Additional trackers at large-*z*

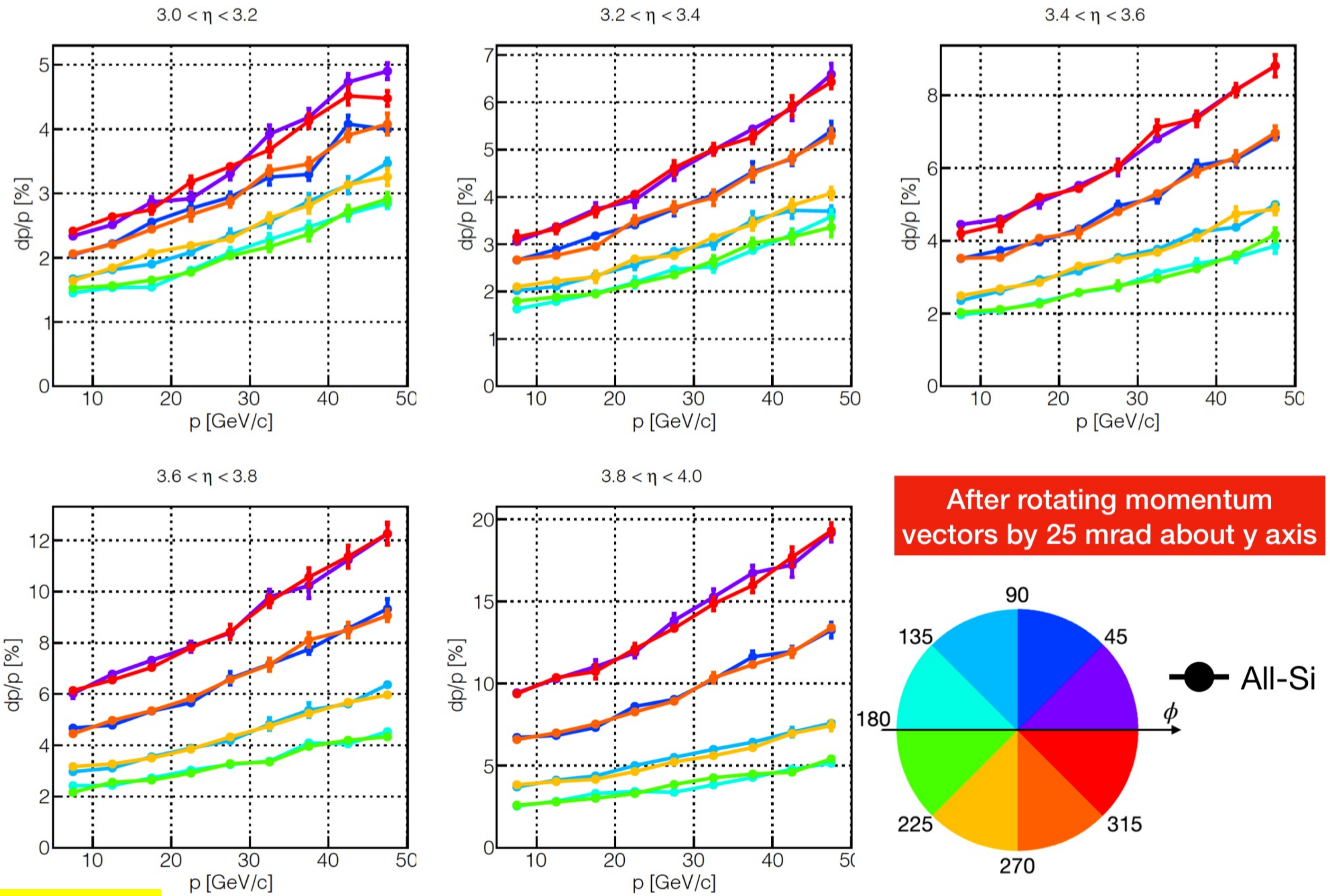
- Momentum resolutions can be enhanced by complementing detectors with additional tracking stations



R. Cruz-Torres

All-Silicon Concept - Effect of crossing Angle

Note, 20 μm pixel pitch in these simulations corresponding to ~ 6 μm point resolution



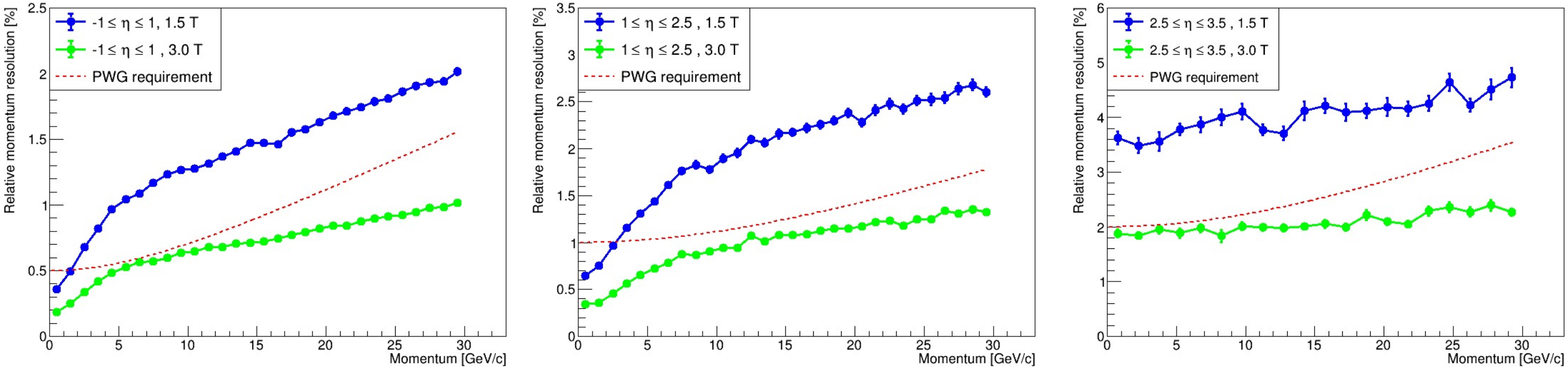
After rotating momentum vectors by 25 mrad about y axis

R. Cruz-Torres

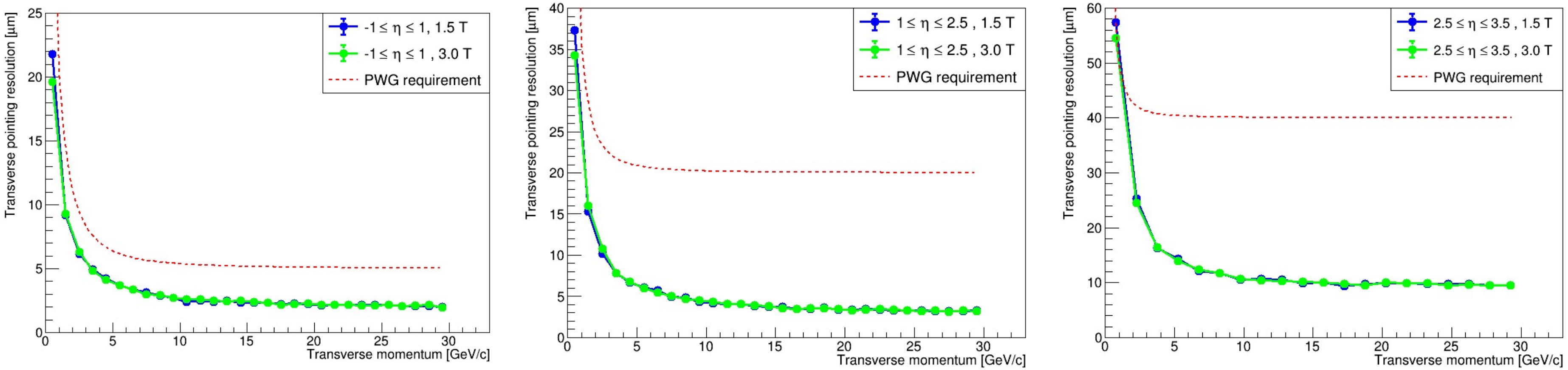
For more on all-silicon concept see arXiv:2102.08337

Hybrid Concept – YR momentum resolution

- Relative momentum resolution



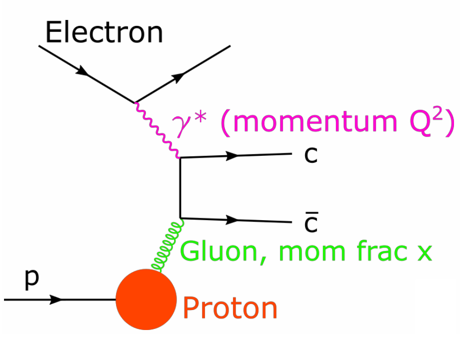
- Transverse pointing resolution

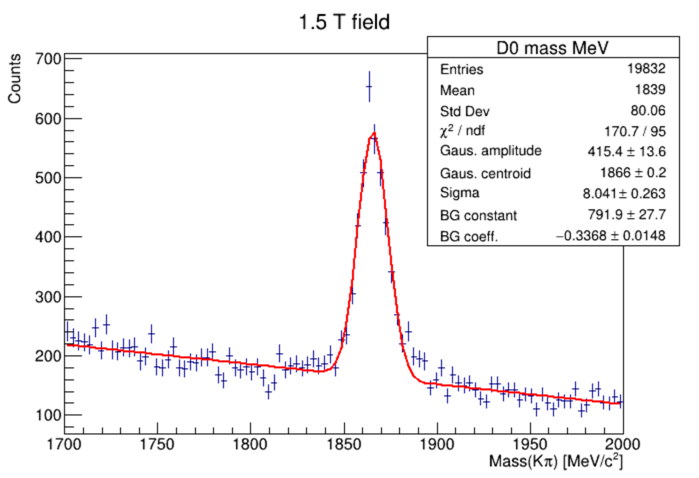


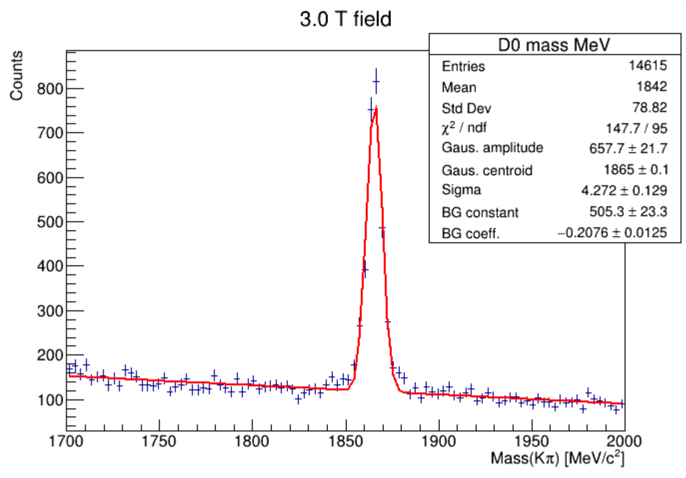
H. Wennlöf

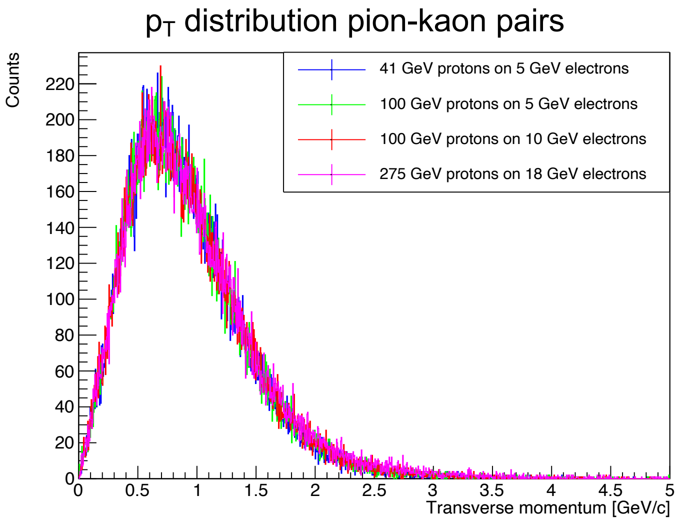
1.5T, 3.0T, PWG requirement

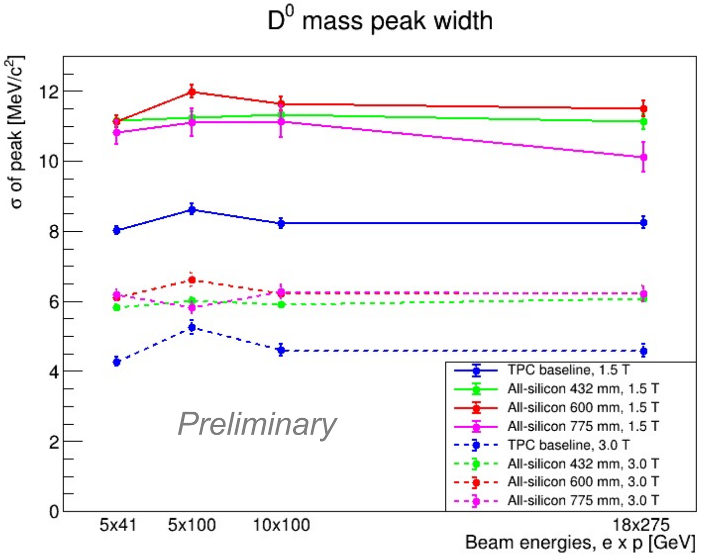
Hybrid Concept – Physics performance studies











Note: All-silicon options in this plot are not the YR baseline all-silicon, for that see arXiv:2102.08337

H. Wennlöf

EIC Silicon Consortium

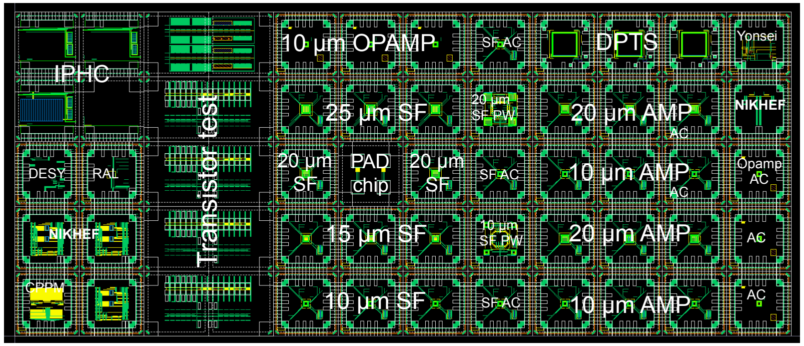
- The development of a ITS3 derived EIC vertex and tracking detector is carried out by the EIC Silicon Consortium
  - EOI: https://indico.bnl.gov/event/8552/contributions/43219/

- The EIC SC is open to institutes from different emerging collaborations interested to work on the proposed sensor solution for their specific EIC detector implementation
  - Similar concept to the CERN RD groups (such as RD50, RD53)
  - This will maximise the successful delivery of the technology with the lowest cost to the project

- The EIC SC is currently defining work packages with associated tasks assigned to groups based on interest and capabilities; regular meetings to start in a few weeks

EIC Silicon Consortium: status and plans

- Sensor development
  - RAL/Birmingham/LBNL already involved in first 65 nm submission with ITS3 Work Package 2
  - More groups signing NDA and collaboration agreement to join
  - ITS3 MLR2 submission planning starting now, including stitched matrix



- Services
  - Material estimates for services and supports available
  - Detailed review of powering options including possible configurations with DC-DC converter or serial powering, estimate of material budget and timescale for development carried out and summarised in a document

- Physics performance simulations
  - Simulation efforts continue in the context(s) of the imminent formation of detector collaborations and the corresponding specific detector designs

Conclusion

- MAPS is the technology of choice for a high granularity, low-mass silicon vertex and tracking detector at the EIC to meet the physics requirements

- The specific MAPS sensor implementation can be agnostic to one detector implementation or another, i.e. only one MAPS needs to developed

- An ITS3 derived EIC SVT based on a new generation 65 nm MAPS has been identified as the best way forward
  - Performance meets the requirements
  - EIC SVT development can leverage on a large effort at CERN for all aspects of the detector implementation beyond the sensor design
  - For the sensor design, the ITS3 provides both a main path forward (65 nm) and a fallback solution (180nm)

- The EIC SC is the framework in which this development will be carried forward, across collaborations