DUNE 35t Activity at BNL Status

B. Kirby- April 8, 2015 - BNL DUNE Local Meeting

BNL EDG and the DUNE 35t Detector

- **BNL EDG group tasked with testing DUNE 35t electronic production electronics**
  - Test board functionality, reliability at cryogenic temperature, measure performance
  - Work with instrumentation dept to debug board and firmware issues
  - Integrate frontend readout into 35t DAQ
  - Develop calibration and commissioning procedures
  - Contribute to electronics simulation
- **Current activity focused on board validation**
  - Significant delay in board production schedule
    - Originally anticipated production boards in Oct.
    - Received production boards end of Dec.
    - Cryogenic testing started end of January, ongoing...

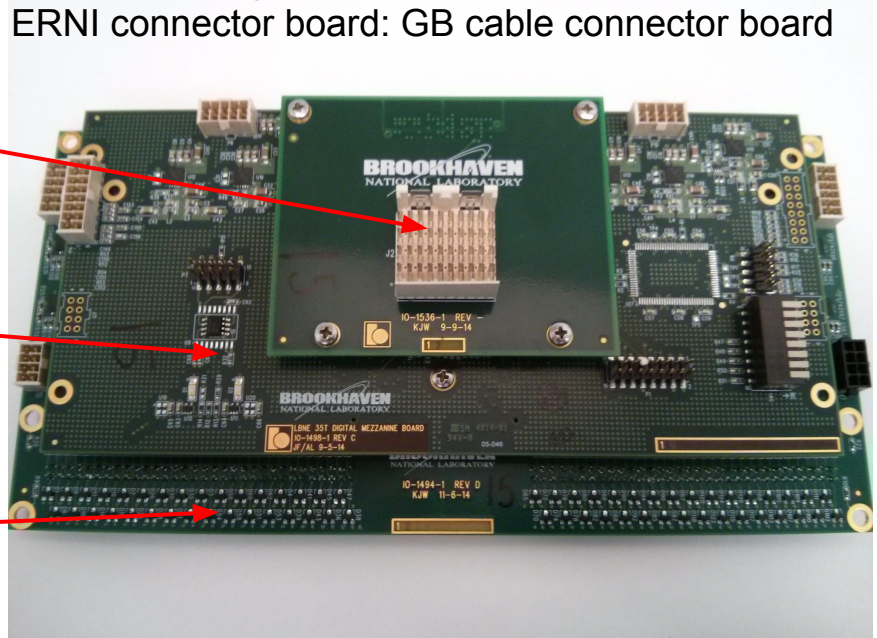
Reminder: 35t FEMBs

- 35t FrontEnd MotherBoards (FEMBs) contain analog board, FPGA board and ERNI interface board
  - Analog board: 8 pairs of shaping-amplifier ASICs and digitizing ADC ASICs, 128 channels
  - FPGA board: Programs and coordinates ASIC operation and readout, streams data to backend through GB transceivers and PGP interface
  - ERNI connector board: GB cable connector board

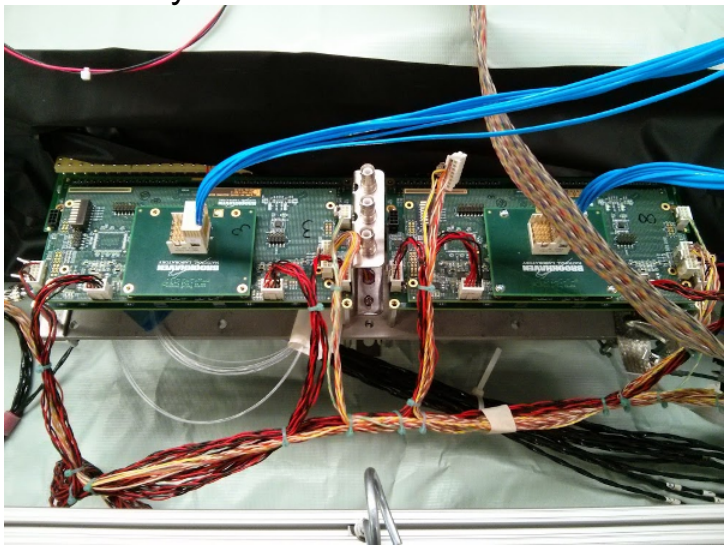
ERNI Board

FPGA Board

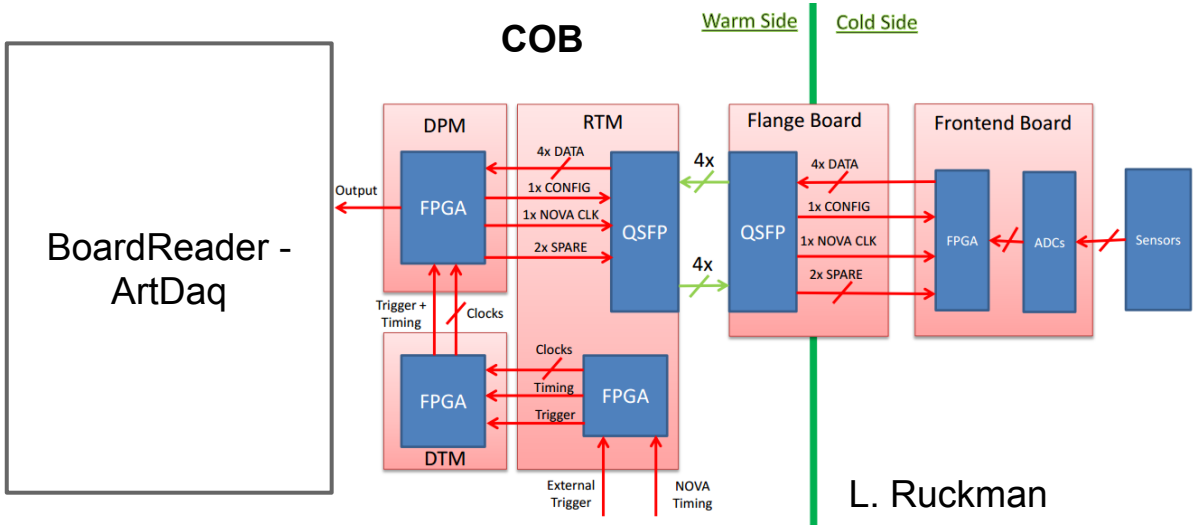
Analog Board



Fully Cabled Boards on APA



35t FEMBs in the DAQ

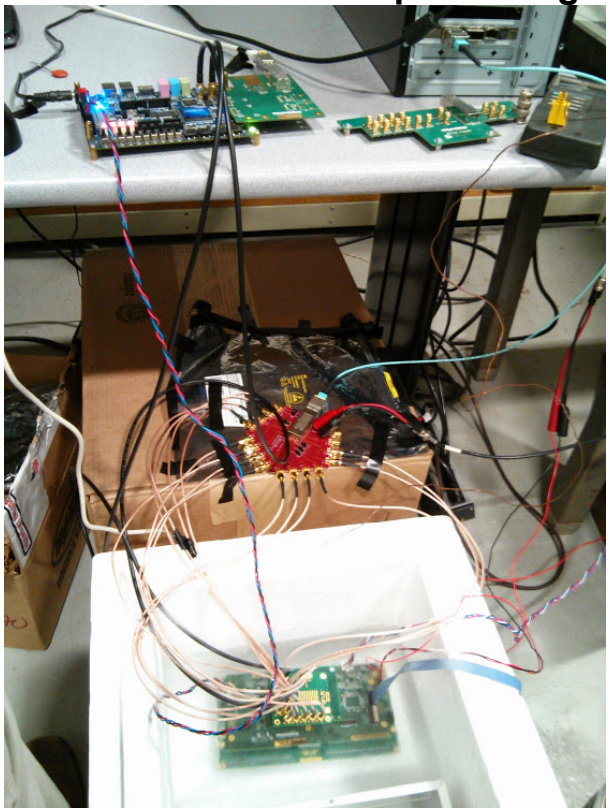


- ArtDAQ provides run control, initiates configuration of subdetectors
- BoardReader receives formatted data from Cluster-on-Board (COB)
- COB receives FEMB data, sends FEMB configuration through SLAC PGP interface
  - Also applies zero-suppresion (to be implemented!)
- FEMBs fully integrated into DAQ as of March 20:
  - FEMBs configured and ADC data streamed using artDAQ interface
- Have PGP-card readout working at BNL, emulates COB readout

35t Production Board Validation Procedure

- Boards validated in several steps:
  a. Basic functionality tests
     - Verify boards work, can be calibrated
  b. Cryogenic testing:
     - Verify boards continue to work in liquid nitrogen, can be programmed, take data etc.
  c. Final validation data-taking
     - Determine if boards still work after cryo testing

35t FEMB Tested in Liquid Nitrogen



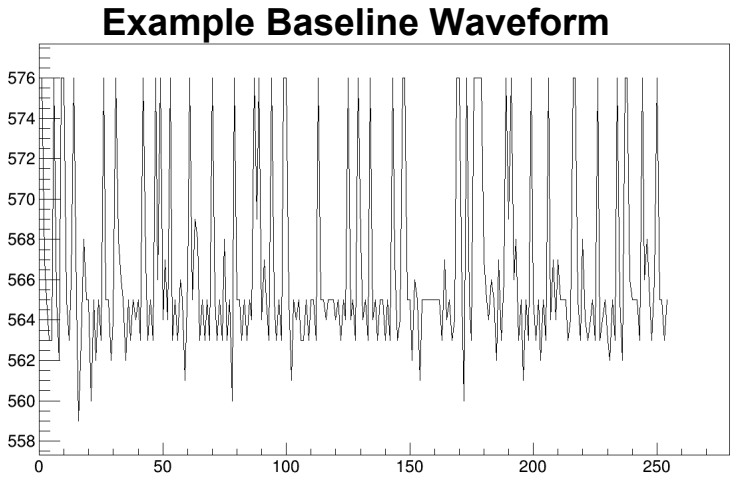
Board Validation Status

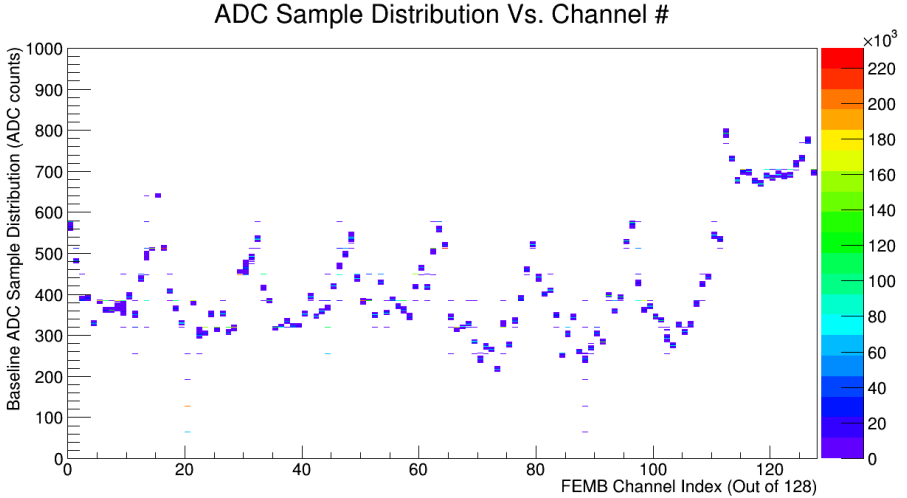
Overall FEMB Testing Summary									
FEMB#	Identifier	Current Location	Basic Test	Cryogenic Test	Final Modifications?	Validation Data Runs	Validation Data Analyzed?	Cleaned?	Shipped?
			Test Log	Cryo Test Log		Run Log			
1	F1A1E1	Instrumentation	PASS	FAIL	-				
2	F2A2E2	Instrumentation	PASS	FAIL	-				
3	F3A?E3???	FNAL	MISSING	PASS	-				
4	F4A4E4	lab 233	PASS	PASS	PASS	433-469		PASS	
5	F5A5E5	Instrumentation	PASS	FAIL	-				
6	F6A6E6	lab 233	PASS	PASS	IN PROGRESS				
7	F7A7E7	Instrumentation	PASS	FAIL	-				
8	F8A8E8	FNAL	PASS	PASS	-				
9	F9A9E9	lab 233	PASS	PASS	PASS	356-393	PASS	PASS	
10	F10A10E10	lab 233	PASS	PASS	PASS	318-355	PASS	PASS	
11	F11A11E11	lab 233	PASS	PASS	REDO - needs P5 connector	168-207	PASS	PASS	
12	F12A12E12	Instrumentation	PASS	FAIL	-				
13	F13A13E13	lab 233	PASS	PASS	PASS	-		PASS	
14	F14A14E14	high-bay	PASS	FAIL	-				
15	F15A15E15	lab 233	PASS	PASS	IN PROGRESS				
16	F16A16E16	Instrumentation	PASS	FAIL	-				
17	F17A17E17	lab 233	PASS	PASS	PASS	394-430	PASS	PASS	
18	F18A18E18	Instrumentation	PASS	MODIFIED-UNUSABLE					
19	F19A0E19	high-bay	PASS	FAIL					

Summary of Current Board Failures

- 3 boards not programmable by JTAG in liquid nitrogen
  - Cause is not clear, swapping FPGA boards
- 3 boards have ASICs not getting programmed by SPI
  - Usually single pin issue
- 1 boards not streaming data from all ASICs
  - ADC link or FPGA board connector problem
- 1 ASIC not getting calibration signal
  - ASIC replaced April 7

“Stuck Code” Issue with FEMB Data





- Still observe “stuck ADC codes” in FEMB digitized data
  - Fairly rare at room temperature, ~3% of channels
  - Issue becomes worse in liquid nitrogen, see significant variation between boards
  - Electronic noise or variation in ADC ASIC power supply possibly causes
    - Under study by us and instrumentation dept engineer + student
- Baseline distribution obtained from entire FEMB shows interesting features
  - Offsets possibly FE ASIC feature, does not affect pulse shapes
  - Used low-threshold setting to make this plot, induction channels will be OK

Summary

- Nearly finished validating 35t production boards
  - 8 boards being debugged
- Trying to understand ADC code issue in liquid nitrogen
  - Running out of time to fix it in hardware
  - Looking at firmware fixes (staggering ADC sampling clocks)
  - Considering software fixes (spurious sample filter?)
- Critical that physicists help BNL engineers with next revision of cold electronic boards:
  - Boards/ASICs redesign underway, informed from 35t issues
  - Engineers have significant time constraints, need help analyzing large amount of data and boards
  - Test setup in place for room temperature and cryogenic board testing going forward