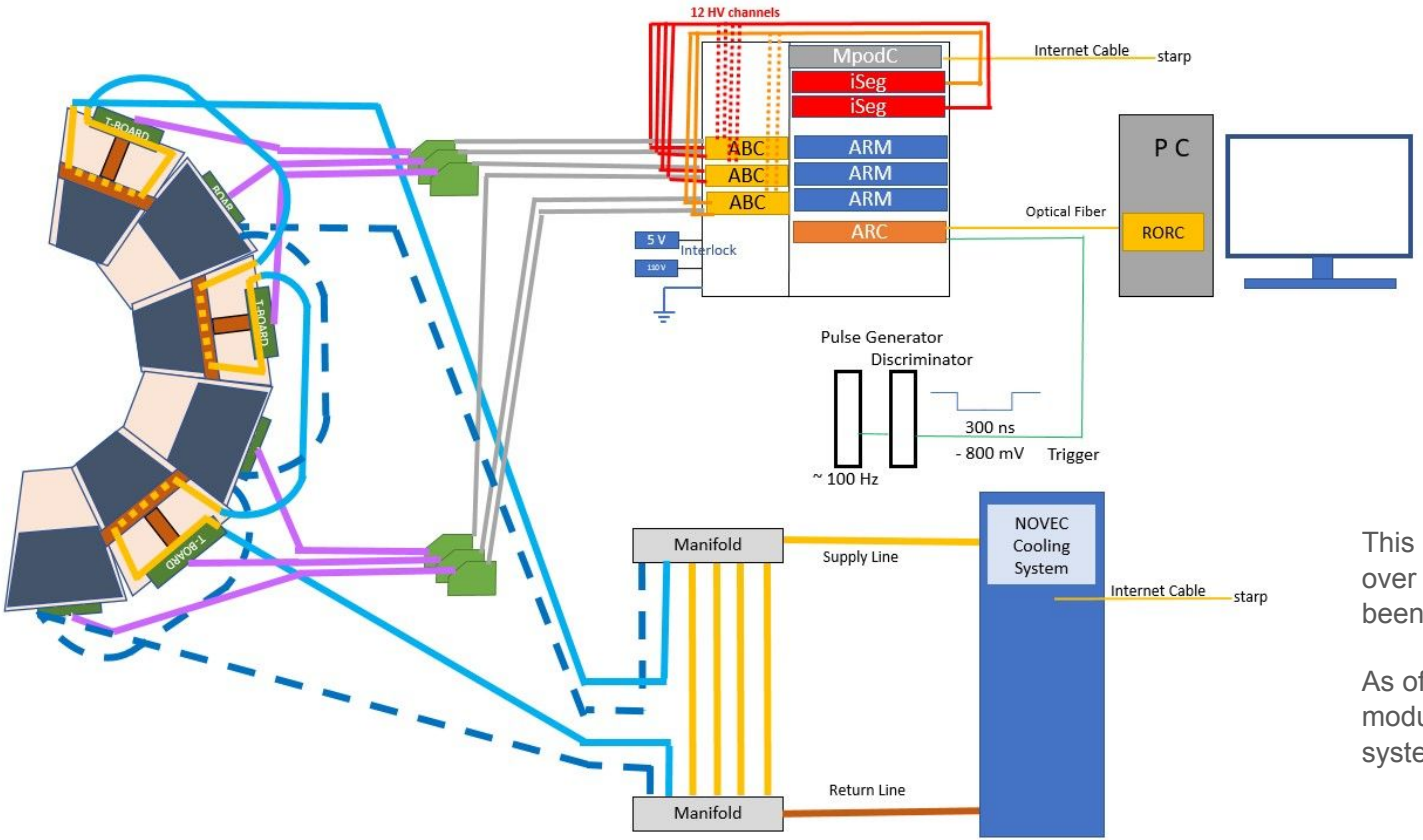
BNL test stand status for pre-installation testing

Yu Hu, Xu Sun, Prithwish Tribedy

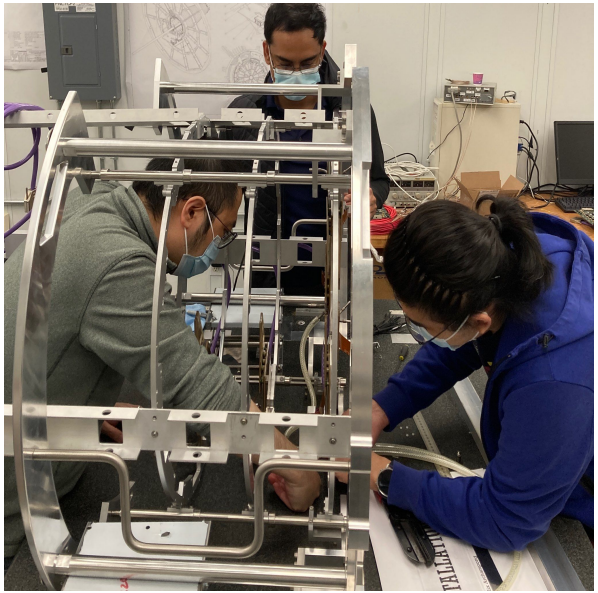


This is the schematic of our setup -- over the last week this is what we've been trying to assemble.

As of now we're aiming to bias 6 modules (12 sensors) with cooling systems, slow control and DAQ

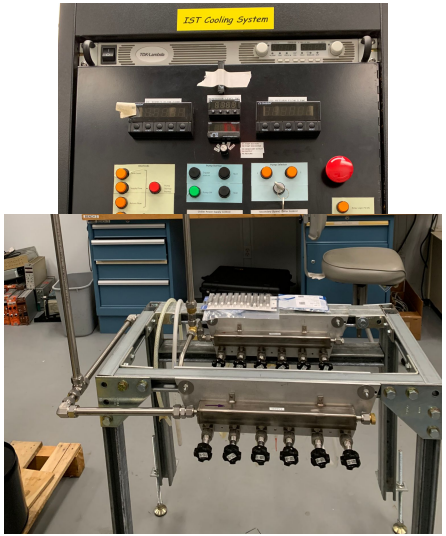
Team, items and lab set up for pre-installation testing

We will have the same team as integration test (Yu, Xu and Prithwish) last year before others from UIC join the team.



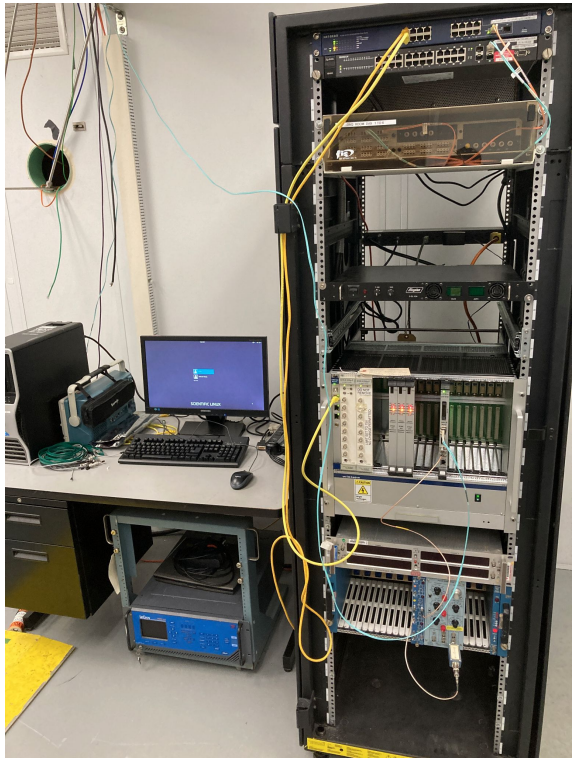
Over the last week we have been trying to measure the length of cables, getting trained to setup the module

We moved everything from 510 on Monday with help from Mike to set-up testing setup in the cleanroom.



Rahul and Bill moved the cooling system to clean room -- will be online soon

Team, items and lab set up for pre-installation testing



With help from Mike, the DAQ stand is fully setup and connected to server

ITEMS	In CR	We need	Source
MPOD Create	1	1	510
ARC	1	1	510
ARM	1+2	3	510 + Platform
iSEG	1+2	3	510
Grey cable	1	6	510
Purple cable	2	6	510
PC + D-RORC	1	1	510
Optical cable	1	1	510
ABC board	3	3	510

ITEMS	In CR	We need	Source
Ethernet Cables + USB	2	2	510
PPB	1	6	510
NIM Pulse Generator	1	1	510
NIM Discriminator	1	1	510
Interlock cheater	1	1	510
Lemo Connectors + capacitor	2	2	510
HV cable	2	6+6	510

Software update and readiness

```
[huyu@fsttesting2 pre-test]$ ../../../../tonko/fst_sl7/fgt_run_daq -R 1 -L -c fst_rdo_conf.txt -n 10
INFO: fgt_run_daq.C [line 112]: Hello FST!
INFO: fgt_run_daq.C [line 216]: Using new physmem at 0x7f64f4f86000
Tonko: fgt_run_daq.C [line 230]: Physmem is 536870912 bytes [512 MB], need 64 MB
INFO: ars_lib.C [line 94]: Reading configuration parameters from fst_rdo_conf.txt
INFO: ars_lib.C [line 1090]: [1] Configuring with ARM mask 0x02
INFO: ars_lib.C [line 843]: [1] Doing ARC-II reboot
INFO: ars_lib.C [line 877]: [1] ARC-II firmware rev 63
INFO: ars_lib.C [line 882]: [1] ARC-II PLL output RHIC strobe frequency 0.0000 MHz; trigdclk input frequency 5*0.0000 MHz
INFO: ars_lib.C [line 894]: [1] ARM address setup completed, detected ARM flags 0x07
WARNING: ars_lib.C [line 898]: [1] Setting ARC-II clock/trigger source to LOCAL
INFO: ars_lib.C [line 1129]: [1] doing FEE power control...
INFO: ars_lib.C [line 1144]: [1] doing I2C...
WARNING: ars_lib.C [line 1167]: [1] Gerrit's special (July 2013 style) long reset
INFO: ars_lib.C [line 1423]: [1] RDO 1 is configured
WARNING: ars_lib.C [line 919]: Setting ARC-I clock source selector to INTERNAL (no effect on ARC-II)
INFO: ars_lib.C [line 929]: [1] Doing software tcmd2 reset
INFO: ars_lib.C [line 946]: [1] ARC-II PLL output RHIC strobe frequency 9.3937 MHz; trigdclk input frequency 5*0.0000 MHz
INFO: fgt_run_daq.C [line 290]: Doing RDYRX
INFO: fgt_run_daq.C [line 340]: Event 1/10: words 5313, status 0x014C1082
INFO: ars_lib.C [line 1487]: [1] Detected ARC firmware rev 63
INFO: fgt_run_daq.C [line 340]: Event 2/10: words 21, status 0x00015082
INFO: fgt_run_daq.C [line 340]: Event 3/10: words 5313, status 0x014C1082
INFO: fgt_run_daq.C [line 340]: Event 4/10: words 21, status 0x00015082
INFO: fgt_run_daq.C [line 340]: Event 5/10: words 5313, status 0x014C1082
INFO: fgt_run_daq.C [line 340]: Event 6/10: words 21, status 0x00015082
INFO: fgt_run_daq.C [line 340]: Event 7/10: words 5313, status 0x014C1082
INFO: ars_lib.C [line 1504]: [1] Detected ARM serial 0x0000,0000,0000, firmware rev 106, temperature 0.0 on ARM # 1
INFO: fgt_run_daq.C [line 340]: Event 8/10: words 21, status 0x00015082
INFO: fgt_run_daq.C [line 340]: Event 9/10: words 5313, status 0x014C1082
INFO: fgt_run_daq.C [line 340]: Event 10/10: words 21, status 0x00015082
INFO: fgt_run_daq.C [line 470]: Received 10 events in 1 seconds (avg 10.00 Hz), after 0 seconds start delay
[huyu@fsttesting2 pre-test]$
```

fsttesting2.starp.bnl.gov updated to SL7, D-RORC driver update with help of Mike,Tonko

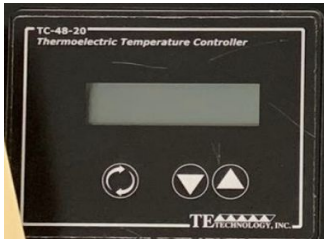
```
#cd ${MODULE_TOP}
#dbLoadRecords("db/asynRecord.db","P=IST:,R=asyn,PORT=HX86PA,ADDR=0,IMAX=100,OMAX=100")


# Configure ASYN port drivers
drvAsynIPPortConfigure("ADAM-6017","130.199.60.115:502 TCP",0,0,1)
drvAsynIPPortConfigure("ADAM-6052","130.199.60.80:502 TCP",0,0,1)
drvAsynIPPortConfigure("TC-48","130.199.60.121:2000 TCP",0,0,0)
drvAsynIPPortConfigure("HX86PA","130.199.60.127:2000 TCP",0,0,0)
```

lstcooling.cmd, requires 4 ip addresses

New ip addresses obtained with help from Wayne, cooling system will be available soon.

ADAM 6052 (controller)
ADAM 6017 (controller)
TC-48 (thermoelectric temp. controller)
HX86PA (humidity sensor)



Cooling package is compiled in softioc4: /star/u/sysuser/iocTop/FST/ISTCOOLING

We will first test the package on softioc4 and then move to sc5 test with SC for DAQ and alarm system.

More details about pre-installation activities: Xu's presentation