FCS Electronics, Trigger & DAQ
at the Apr 2021
F2F Meeting

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for
Akio, Bob, Christian, Mike, Tim

FCS DEP/ADC Status

- working fine
- started adding cooling fins to the FPGAs (½ complete, during access times) [Christian]
- 1 bad board moved to the Preshower section so it doesn't interfere with DAQ

FCS Trigger Status

- stage_0/1 modified to include a simple peakfinder [TL]
  - debugged, looks good
- stage_2 has problems with the “High Tower” component
  - problem found, waiting for the fix [Christian]
- stage_3 finished but with only 8 bits
  - we would like to have all 16 bits which we can at least read from the data for debugging
    - not the highest priority [Christian, TL]
- all software bitcheckers checked [Akio] and working correctly
  - need to provide a comprehensive testing suite to Akio et al. Soon. (TL)
- Trigger Group provided us with all 16 bits [new!]
  - verified and looks fine!
  - the new path should be slightly faster ⇒ need to check

DAQ Status

- included in all STAR runs for last ~2 months
  - included from noon to midnight to allow us to continue debugging the firmware during the morning
- running smoothly, no issues at all
- FCS is readout for all STAR triggers (e.g. with the TPC)
- a few debugging triggers from the FCS (High Tower mostly) are included for scaling/counting purposes, not for readout
  - plan is to include (and correctly name) the 8 triggers we have now available as soon as the stage_3 firmware gets completed
    - in preparation for the OO-200 data taking

OO-200 Run Status

- assumed to start 2nd week of May and last for ~1 week
- we expect to be ready with a set of 16 triggers
- running mode
  - 1) FCS present in every “STAR triggered” event (~2 kHz)
    - same as now
  - 2) FCS triggered events [new]
    - note that those events will/might have the wrong bunch xing relative to all other STAR detectors -- TBD
    - prescaled/adjusted to <2 kHz so we don’t go over the ~4 kHz total STAR Trigger upper limit

Near Term Future

1. fix the stage_2 HT bug [Christian]
2. add 8 more bits to stage_3 [Christian, Akio, TL]
3. re-check timing to Trigger [TL]
4. run bitcheckers for verification [TL]
5. start adding FCS triggers into the Run Control [Jeff, Jack, Akio, TL]