INFN TRIESTE

ALICE

ALICE ITS3 Project progress report

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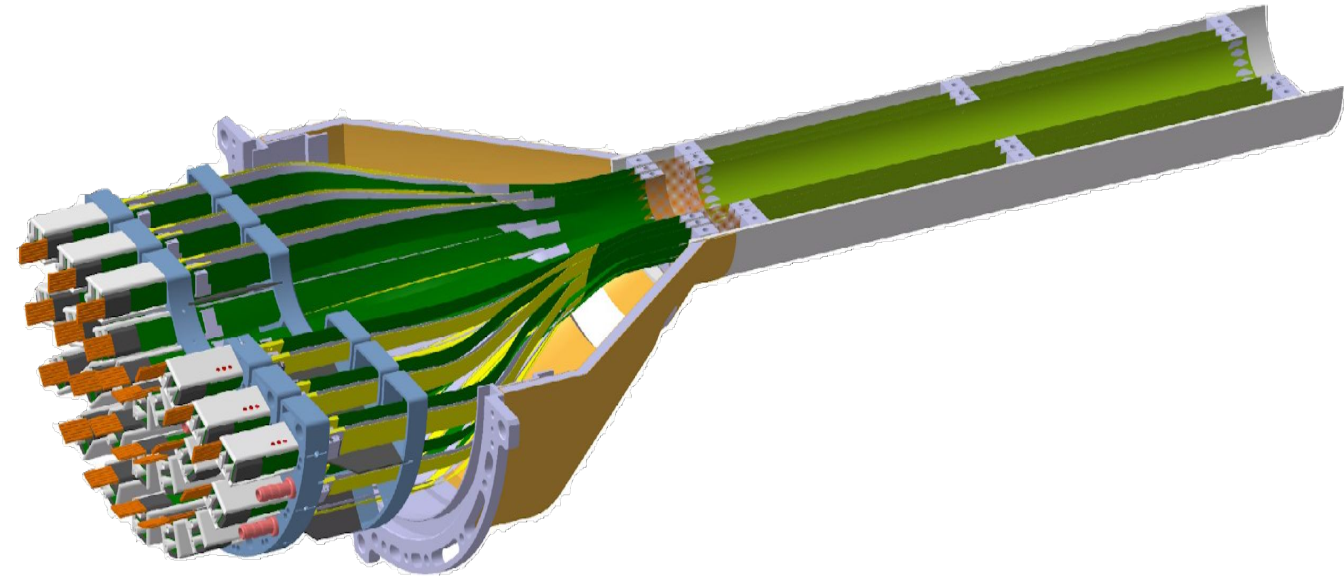
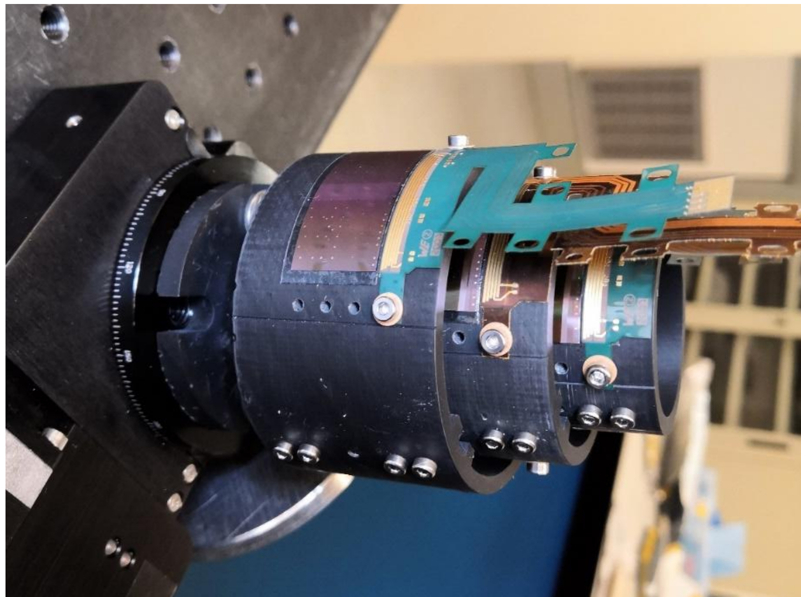
EIC Silicon Consortium meeting – Feb 4 2021



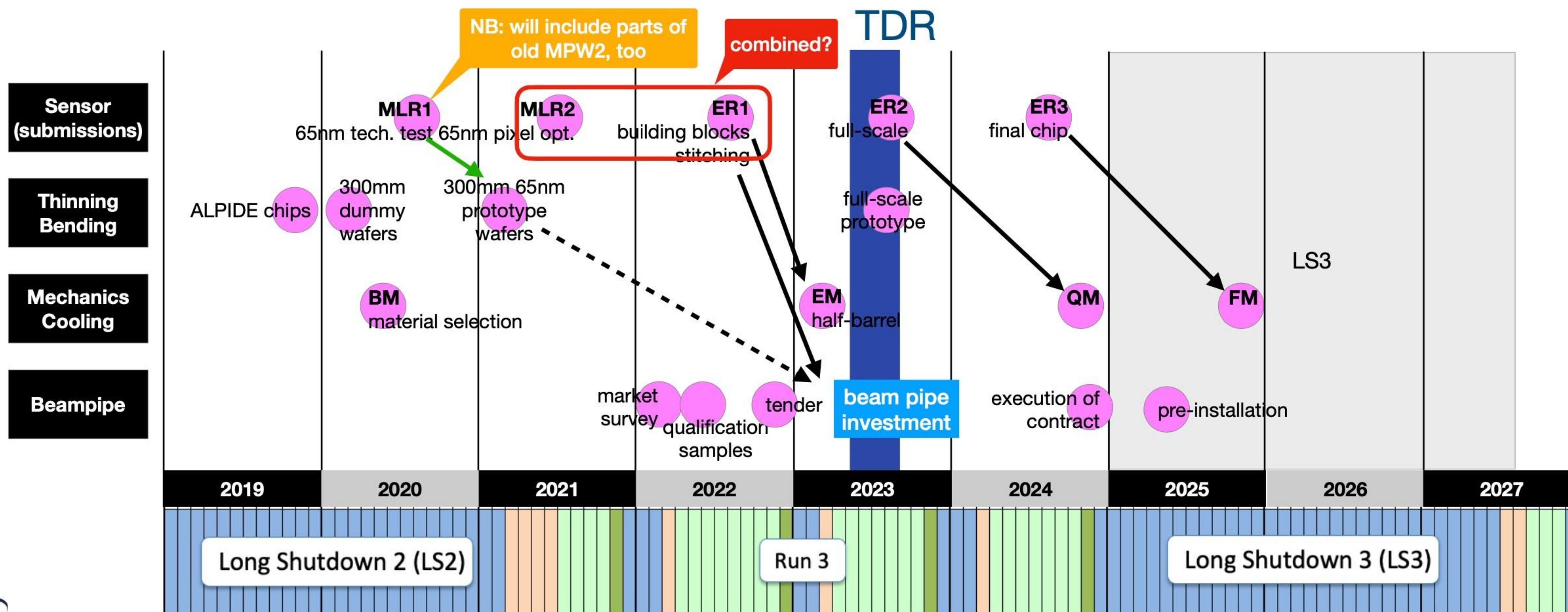


Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

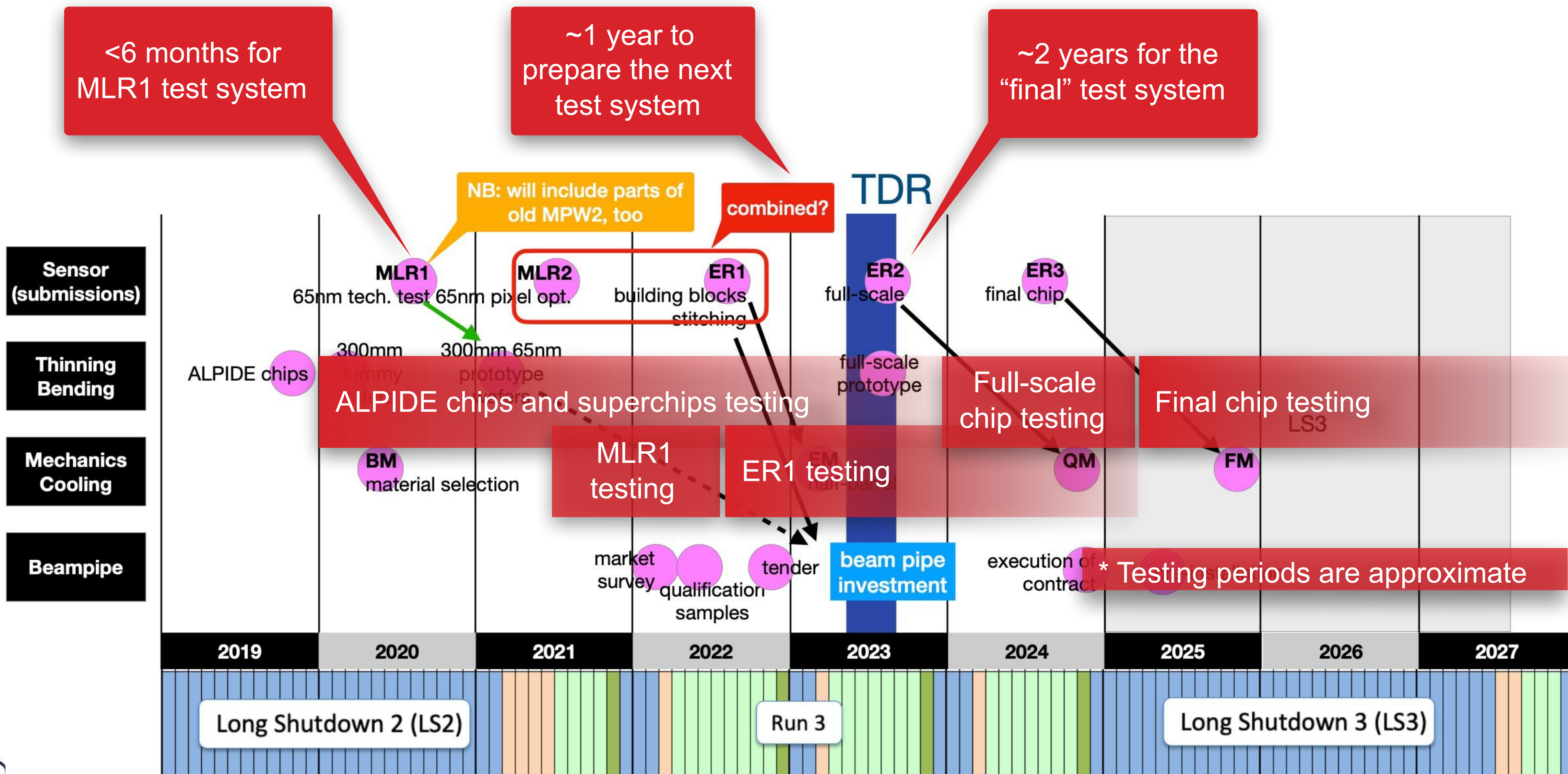
Outline

- ITS3 Project timeline
- MLR1 Testing plans
- Thinning and Bending
- Interconnections
- Mechanics

ITS3 project timeline



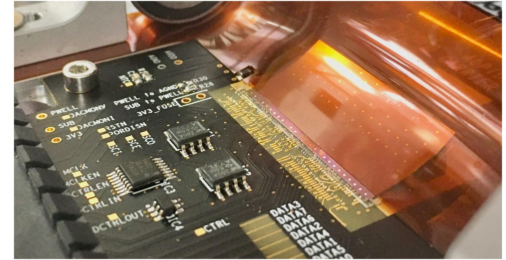
ITS3 project timeline: testing

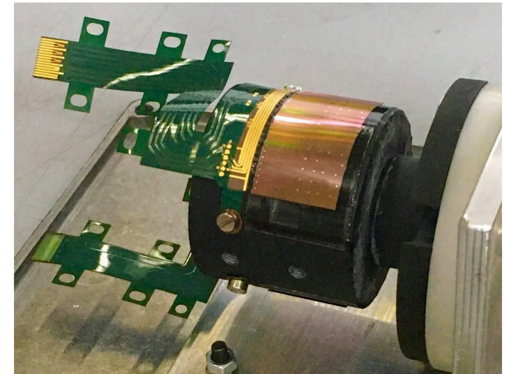


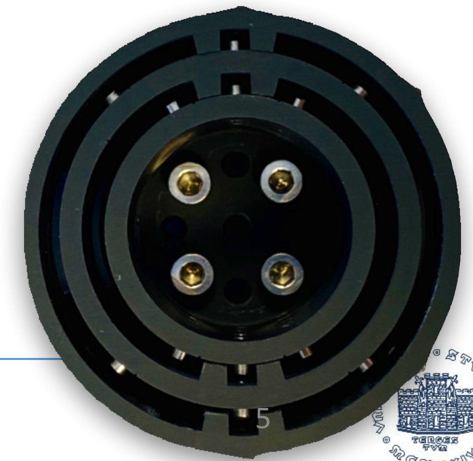
Bent ALPIDE testing

From now to ~next year

- Feasibility tests - **Done**
  - First tests in spring last year, beam test in June
- Test of chips bent in various directions - **Mostly done**
  - Lab and beam tests with wire bonded chips - done
  - SpTab bonded chips bent in lab - to be tested in beam
  - µITS3 (6 bent chips, various radii) - to be tested in beam
- Test bent superchips - **To do**
  - Diced portions of wafers containing many ALPIDE reticles







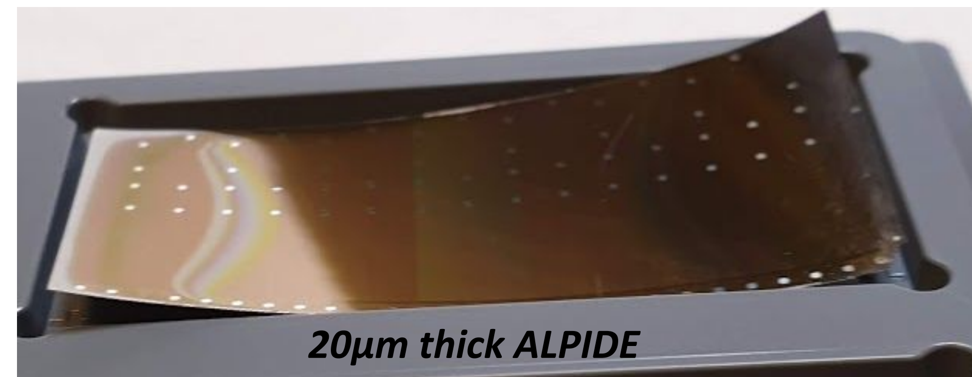
Testing of MLR1 pixel matrices

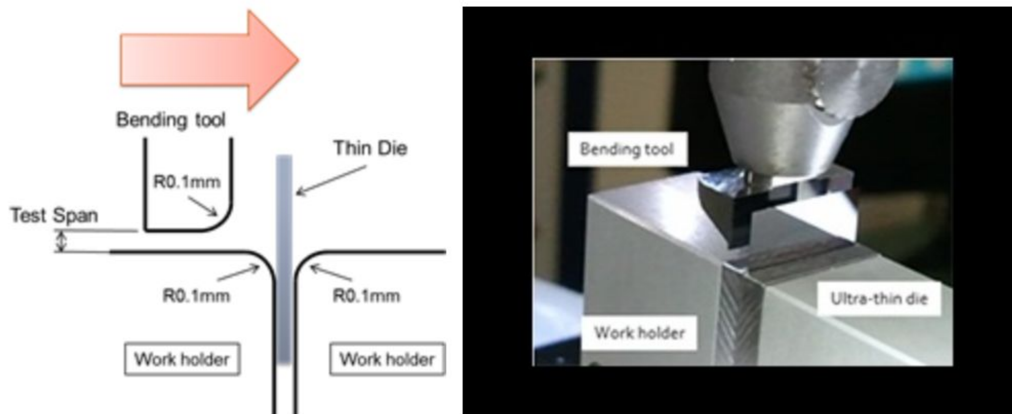
In 6 months for ~1 year

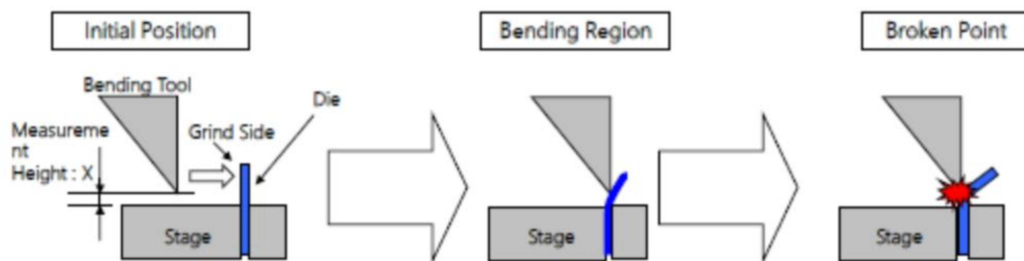
- Short time to prepare the test system and short usage time → avoid custom solutions
- Provide feedback for ER1 quickly → distribute the characterisation workload
- **Solutions**: a "proximity board" (+ potentially "carrier card") +
  - Existing test system, or
  - General purpose components (oscilloscopes, dev boards…)
- **To keep in mind:**
  - Testbeams, bending tests, irradiation, yield…
  - >100 chips on "carrier card"/"proximity boards" & ~20 test systems

Thinning and bending of single ALPIDEs

- Silicon Deep Reactive Ion Etching (DRIE) of ALPIDE
  - Thinned down to 20-30-50-56 μm
  - Cantilever bending test to breakage
    - 3&4 points test hard to apply on thin small area chips



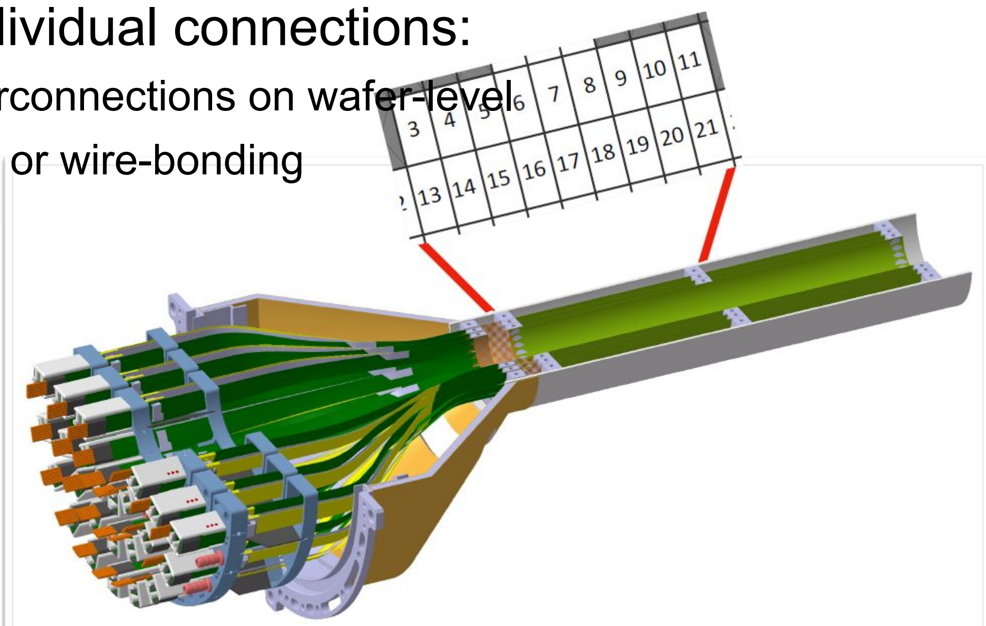


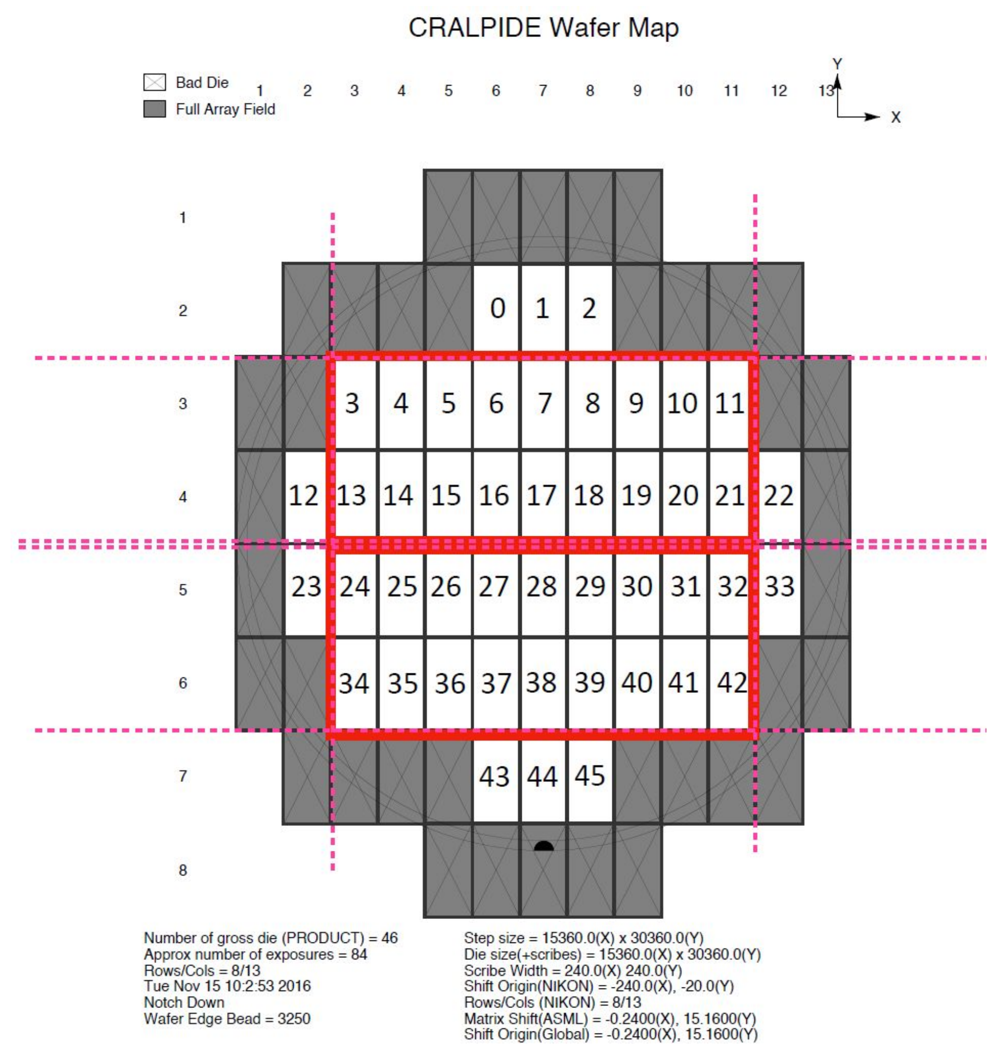


Thickness	Force at break [cN]		
20um	14.8	11.45	16.92
30um	35.95	29.25	35.07
50um	56.04	65.03	124.24
56um	110.5	129.35	

Moving to larger size: ALPIDE Super-chip

- Idea: cut out large “super chips” from a wafer
- about the area of 1/2 ITS3 half-layer 0
  - ~140 x 60 mm
- 9 x 2 chips
  - 9 interconnection areas in z-direction
- need individual connections:
  - no interconnections on wafer-level
  - SpTAB or wire-bonding

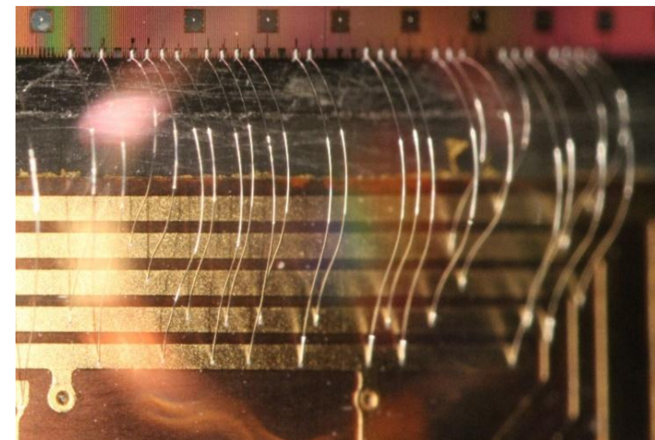




Interconnections for bent chips

- Wire-bonding on curved chip
  - Directly to pads on test carrier board, if possible
  - To bendable FPC extension to reach test carrier board

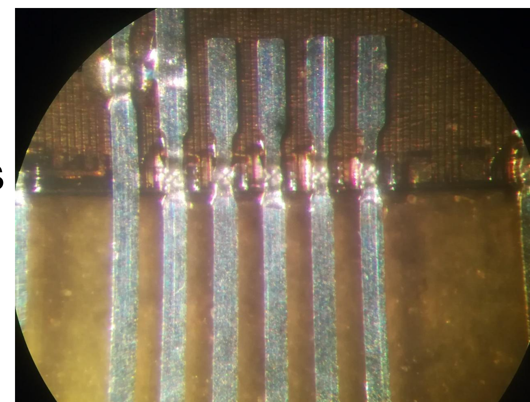
Bent ALPIDE, wire-bonded to bendable FPC, connected to interface card

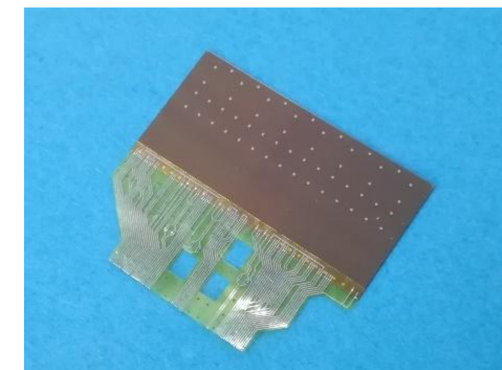


Bent ALPIDE, wire-bonded

- SpTAB bonding chip to flexible chipcables
  - Would easily allow for bending in different directions
  - Chipcable matching the pad floorplan to be developed in advance
  - Needs connector on test carrier board

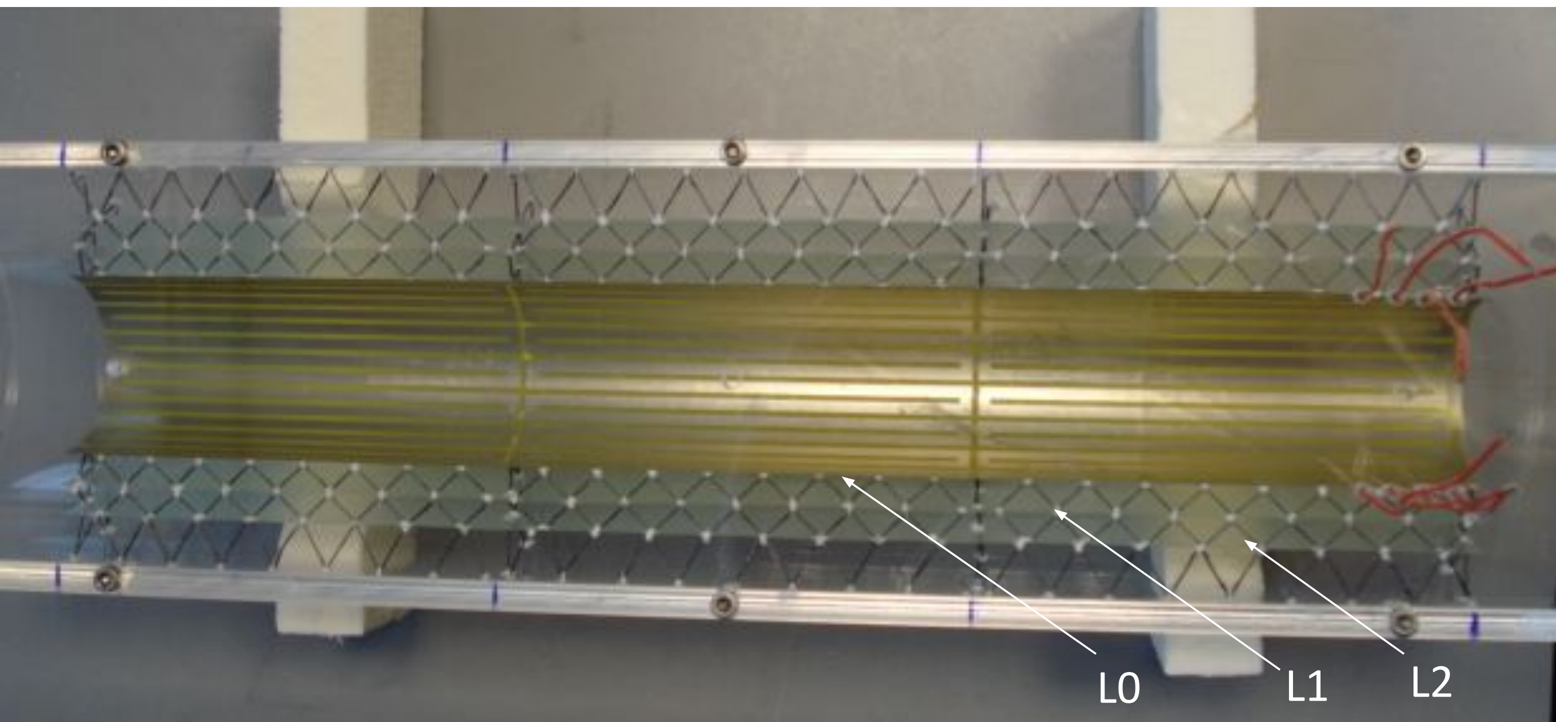
ALPIDE, SpTAB bonded to microcable

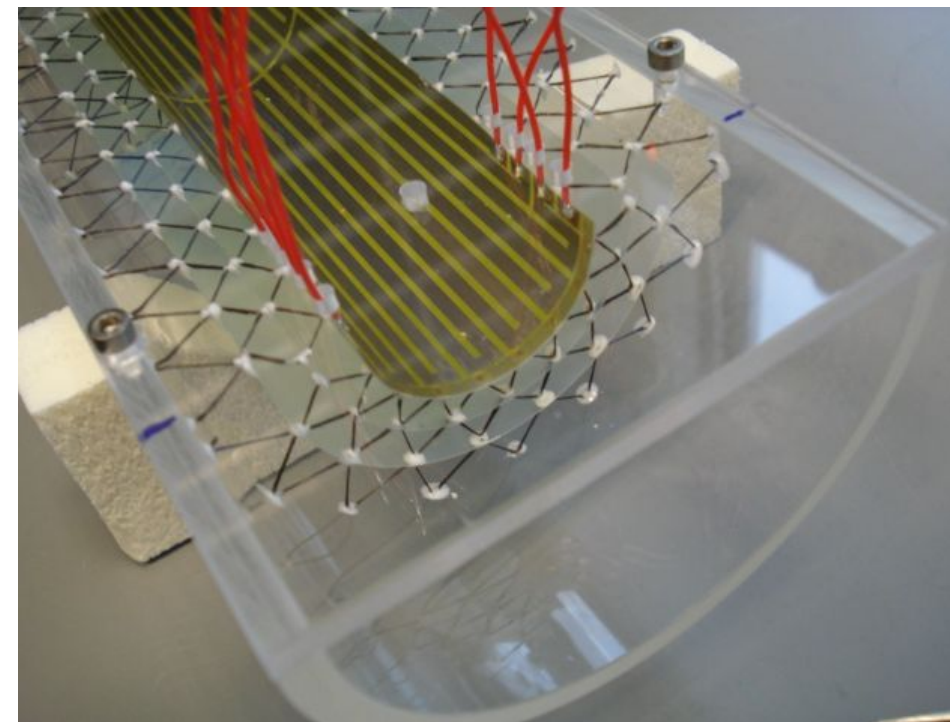




Breadboard Model: dummy HLS with glued heaters

How we simulate the heat dissipated by the Half Layer Sensor during the characterization phase with HLS mock-up

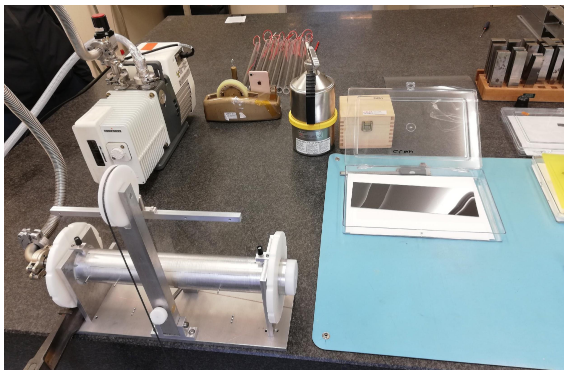
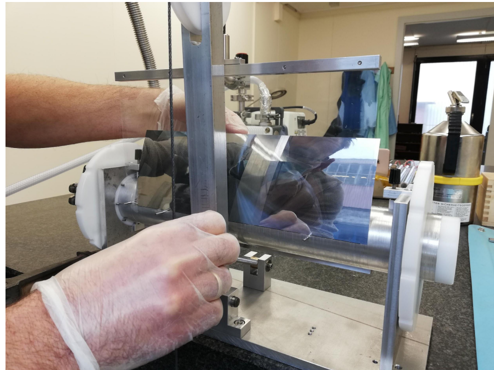


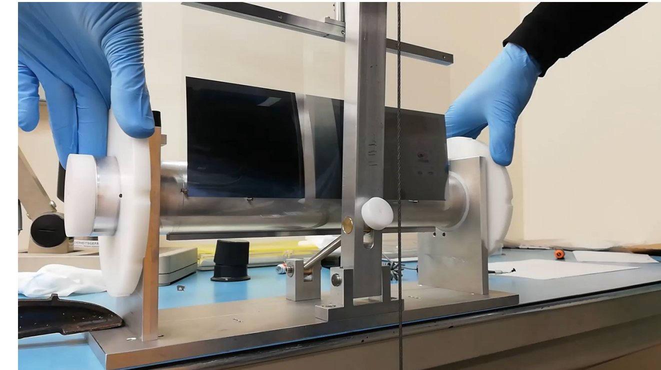


BBM1 assembled.
G10 glass fibers HLS mock-up
HLS-0 equipped with Foil Heater for thermal test

EM: Half Layer Sensor kept bent with vacuum

We are not yet able to keep bended, on a vacuum chuck, a full size HLS in a repeatable and reliable way



Once the chip is bended, vacuum is opened in the mandrel that hold the HLS in position, allowing for the removal of the mylar.

Slots to hold Half layer under vacuum caused failure in some of the bended HLS

under study

- vacuum chuck surface deep inspection and cleaning
- alternative holes pattern for vacuum chuck
- alternative porous material for vacuum chuck
  - ✔ AIR permeable Aluminum Metapor BF 100 AL
  - ✔ AIR permeable Ceramic Metapor CE 100

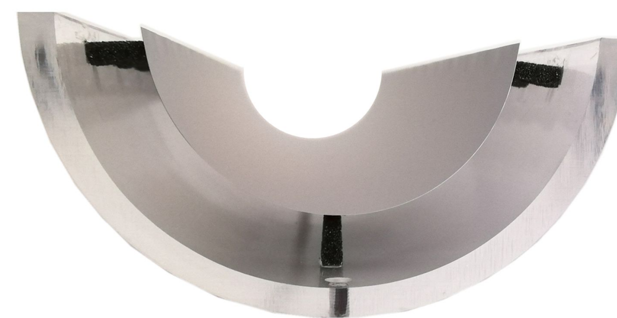
EM: Engineering Model 1 EXS+HLS2

EM1, preliminary steps towards feasibility of keeping the Silicon Half Layer Sensor in position. Several support layouts under study, thermal and structural requirements drive the design; lightest carbon foam used for this first model

Dummy Silicon Half Layer Sensor
280mmx93.2mmx40 µm

Carbon foam wedge: ERG Duocel
[0.06 kg/dm^3]
Carbon fleece
[8g/m^2]

Araldite 2011



Development paths and scalability

- Test setup development:
  5-month development for MLR1 forward compatibility with ER1
- Thinning:
  50 µm 40 µm 30 µm 20 µm (single ALPIDEs, full 8” 180 nm wafers and full 12” 65 nm wafers)
- Bending:
  180 nm: ALPIDEs ALPIDE super-chips & wafer-scale dice
  65 nm: MLR1 reticles (~1x1cm) ITS3-size mock-up chips
  Engineering Modules: full-scale bending system
- Interconnections
  - Wire-bonding technology on ITS3 curvature radii
    - Validated for bonding-after-bending – systematic qualification ongoing
    - Under investigation for bending-after-bonding
  - SpTAB bonding technology for bending-after-bonding (reversible)
    - Validated for ALPIDEs
    - In preparation for 65 nm structures
- Mechanics: carbon foam qualification, heat dissipation simulation