HDI Status and Thruhole Evaluation Procedure

RIKEN/RBRC

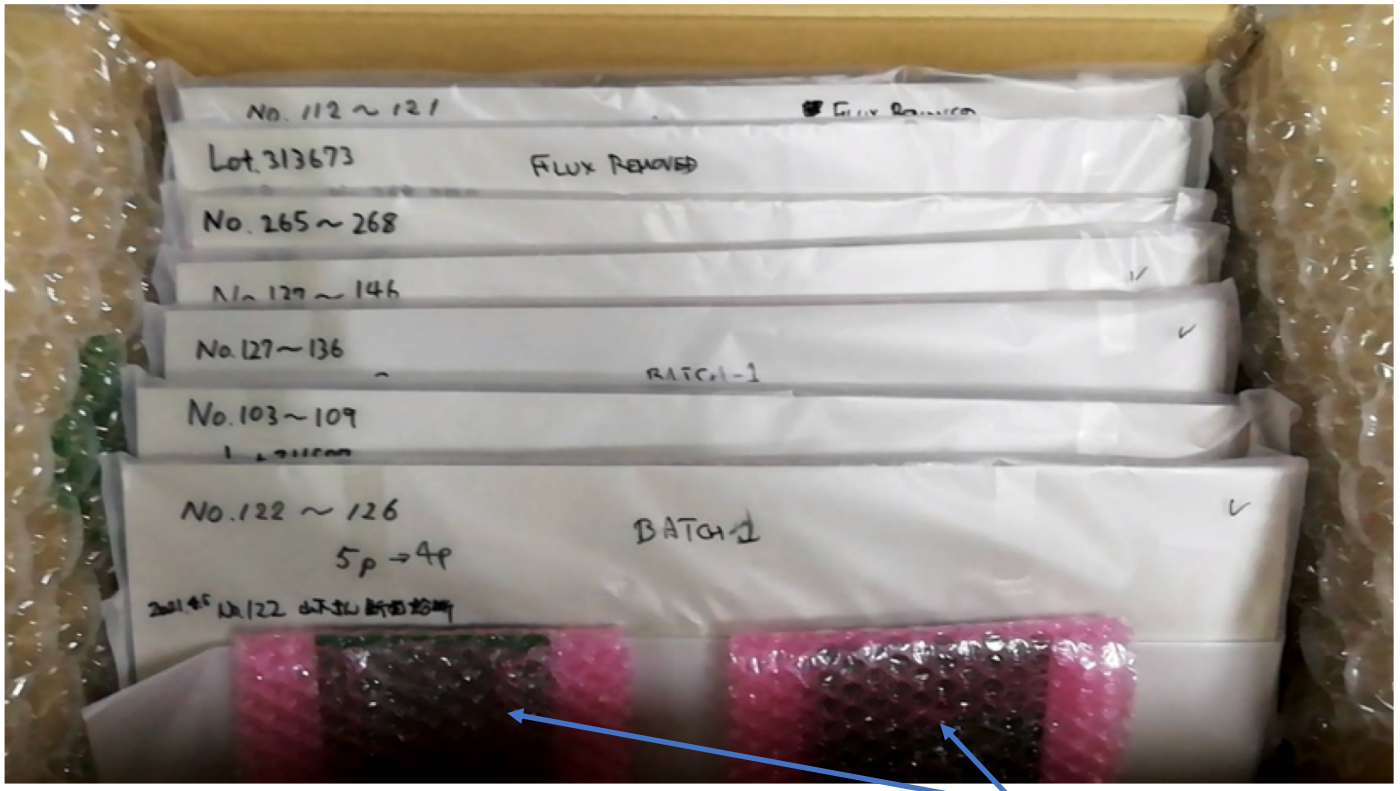
Itaru Nakagawa

Reproduce HDI Plan

- Itaru, Hideto, and Yasuyuki will visit Yamashita co. on May 13th to express our complaints and discuss about the 3rd batch production of HDIs.
- Since the thruhole inspection of sampled HDIs from each LOT has been taking longer time than expected, we have to move on to 3rd batch rather than waiting for their report.
- The primary purpose of this meeting is to determine how many HDIs to be reproduced within their compensation. The quantity is a complicated function of the delivery time and results of their ongoing thruhole inspection by then.
- They reported module-50 inspection result on April 28th.

HDI shipping to Taiwan

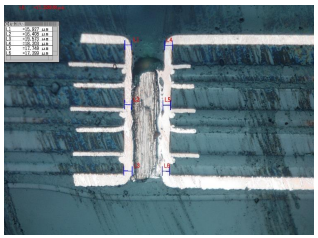
46 HDIs were picked up on April 30th.

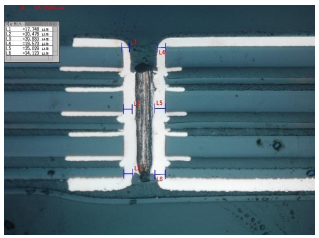


Inspection boards (sorry no connection jig)

Delivery Day	Batch	Order #	LOT #	Quantity	HDI Serial No.		Incremented Quantity	Inspection	Result	Shipped to Taiwan
2019/1/23	Preproduction	349670	302382	6						
2019/2/6		349670	302725	4						
2019/9/11		350963	306716	20						
2019/11/20		Exchanged	307469	1						
2020/4/2	Batch-1A	352075	310184	9	1	9	9			
2020/4/2		352075	310185_1	7	10	16	16			
2020/4/2		352075	310185_2	13	17	29	29			
2020/4/2		352075	310186	30	30	59	59	50	Good?	
2020/4/28	Batch-1B	**352075**	**310188**	**17**	**60**	**76**	**76**	**70**	**bad**	
2020/4/28		**352075**	**310189**	**24**	**77**	**100**	**100**	**80, 94**	**bad**	
2020/6/8		352075	311139	2	101	102	102			
2020/6/8		352075	311587_1	7	103	109	109	105		6
2020/6/17		352075	311587_2	2	110	111	111			
2020/6/17		352075	311614	15	112	126	126	122		14
2020/6/24		352075	311615	21	127	147	147	127		20
2020/7/9		352075	312095	20	148	167	167	(160)		
2020/7/9		352075	312096_1	6	168	173	173			
2020/7/21		352075	312096_2_1	7	174	180	180			
2020/7/28	Batch-1A	Exchanged	312096_2_2	1	24	24	180			
2020/9/28	Batch-2	353110	312532	20	181	200	200			
2020/9/28		353110	312533	16	201	216	216			
2020/9/29		353110	312534	7	217	223	223	(220)		
2020/9/29		353110	312535	14	224	237	237			
2020/9/29		**353110**	**312536**	**7**	238	244	**244**			
2020/10/27		**353110**	**313304**	**24**	245	268	**268**	**265**		**3**
2020/11/27		353110	313673	2	269	270	270			2

Serial Number 50 Thruhole Inspection


U1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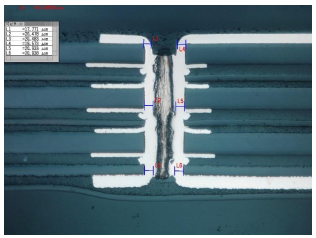
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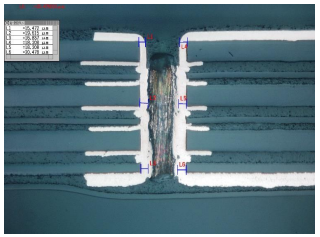
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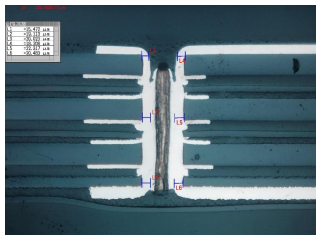
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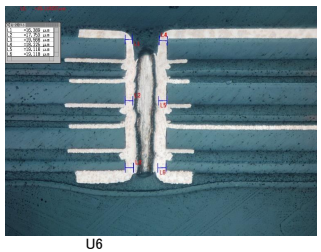
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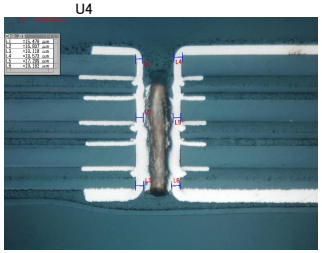
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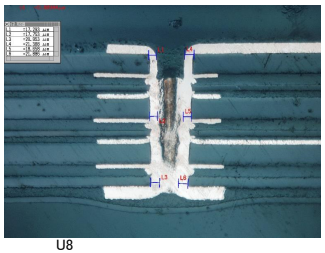
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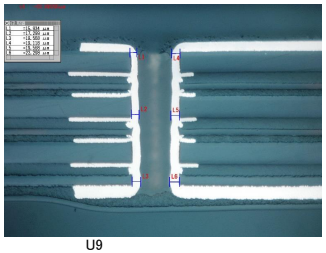

U9

Report from Yamashita on April 29, 2021. They arbitrary selected one thruhole per chip and inspected them. They claim constant thickness of copper plating. For now, we classify this LOT 310186 as good. However, I am worried this observation is somewhat inconsistent with the rest of assembled modules. See next page.

Proposed Strategy

Module 041	S14629-01, 1134	G		4	84.86/89.53	-11.40/-27.38	4.19E-4/2.91E-4	All	
Module 042	S14629-01, 1135	G		4	44.17/12.76	-0.72/-9.63	8.9E-5/2.16E-4	All	
Module 043		B, U20 U16 empty U15 half entries	U20 : slow control in r : 0.58M ohm U16 : slow control in U15 : all good serial out 1/1b 2/2b : good	1					
Module 044	S14629-01, 1136	G		4	77.91/32.73	-21.87/-11.73	6.77E-4/8.6E-4	All	
Module 045		B, U14 empty	U14 Outclockb disconnected	1					◘U10 resetb open and U18, U24 outclkb open, fixed by patches to connect opening lines to neighbor chips
Module 046	S14629-01, 1270 (d	B, U5 U7 U15 empty	U5 : resetb U7 : BCO clockb U15 : reset	2	20	5			U15 is operational if LVDS is set to 255. Module has been assembled one type A sensor for bonding test. (only assemble type A)
Module 047		B, U17 empty, U24 half entries ---------- U17 18 6 empty. U19 half (2021/01/26)	all pads are good For U17 and U24 "all" pads are checked -> all good ----------20210126---------- U6 : bcoclkb U18: outclk U17 all good	1					re-bond chip U17 with new bonding parameter -> didn't help
		B	U1 : resetb, outclk						

- There are certainly open lines in other HDIs in this LOT though, no bad thruhole was detected by Yamashita's inspection of serial No.50.
- This is indicating the limit of sampling inspection method currently ongoing. The fraction of bad thruhole varies from one HDI to another even they are produced in the same LOT.
- Although the inspection is currently ongoing, we shouldn't rely on it too much. As Itaru proposed in the last meeting, we should continue assembly on HDIs except for known bad LOT (and can be found more bad LOT in near future).
- We will judge whether an assemble HDIs are good or bad by testing it after the assembly.

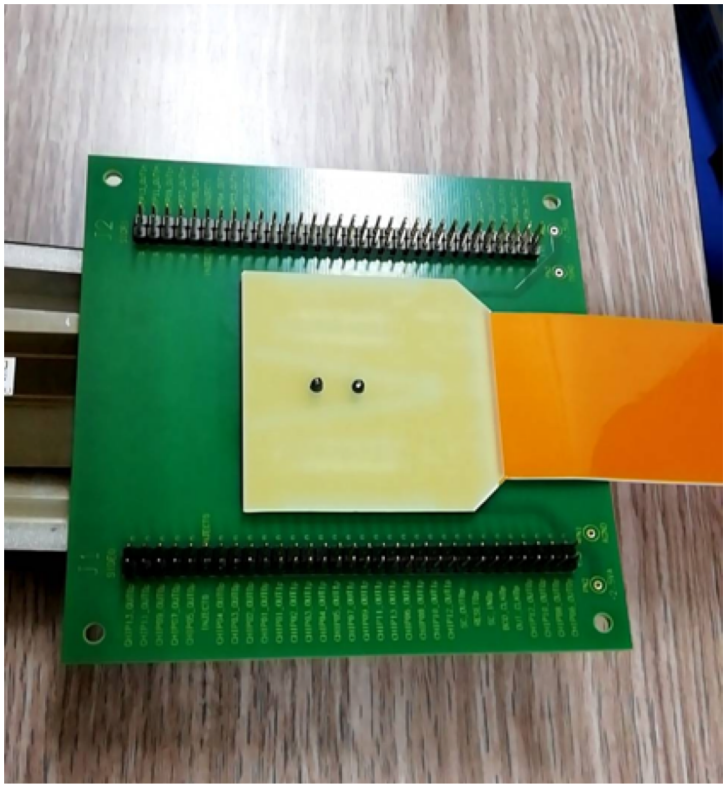
Procedure

1. Calibration as usual
2. The calibration, solo is not sufficient to judge the quality of HDI. As pointed out by Taiwan group in the past, even there is an open line in the data transfer LVDS line, there is still a chance to observe “perfect” calibration result because a single LVDS line still be able to transmit the signal which satisfy the LVDS receiver requirement, if the circumstance is good. Thus we shouldn’t assume that an open line always appears in the calibration result. To be certain, we should at least confirm the conductivities of each LVDS lines using the interception board.

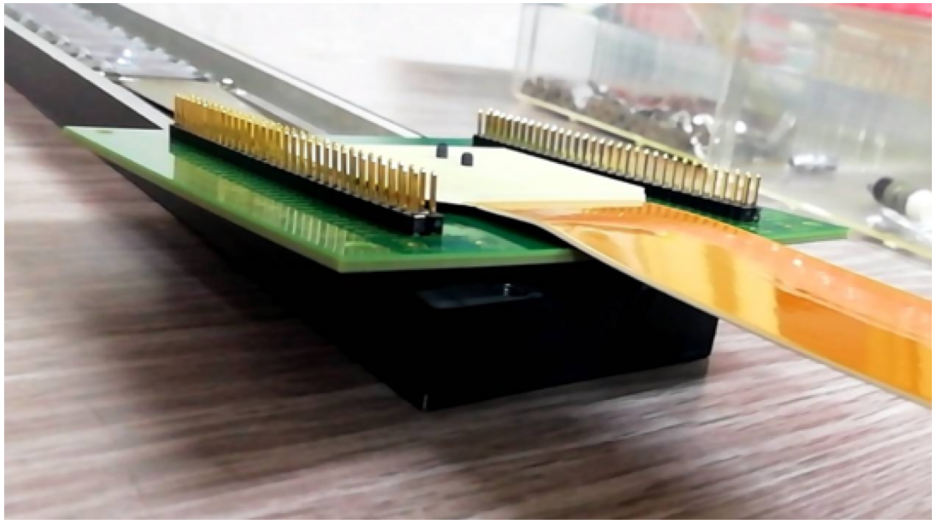
Proposed Procedure

Conductivity check of HDI-LVDS lines using the interception board

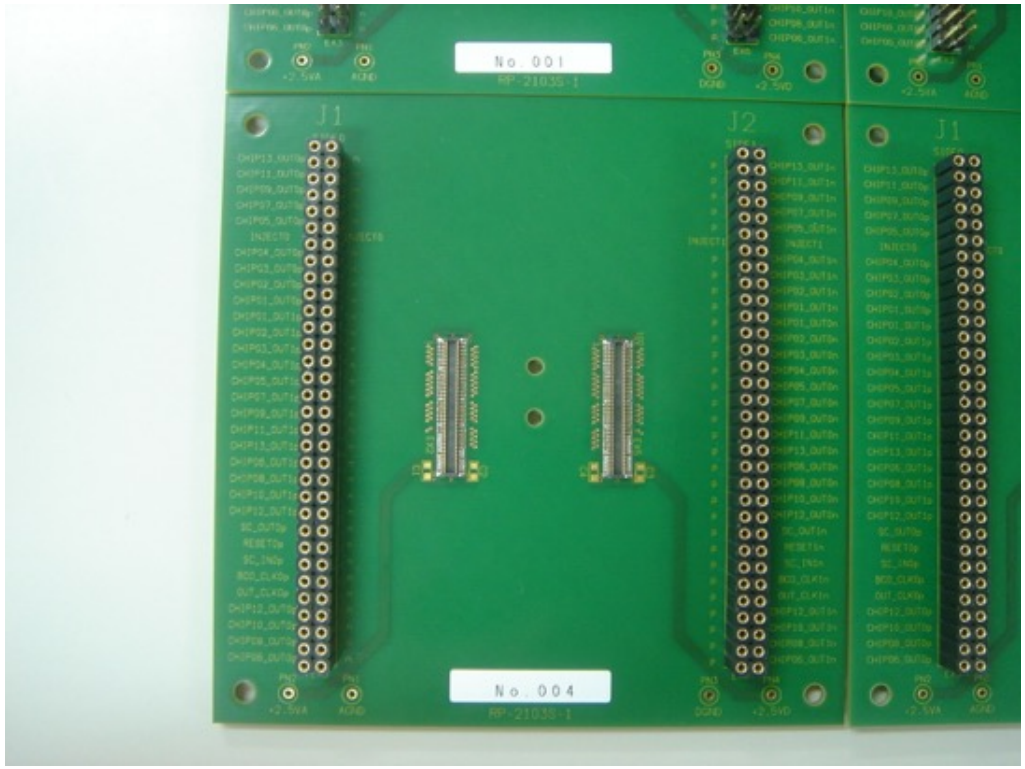
Take data with the interception board



Insert the interception board between a HDI and a conversion cable. Since this is the check if there is any open signal lines, the bus extender is not necessary.



Interception Boards

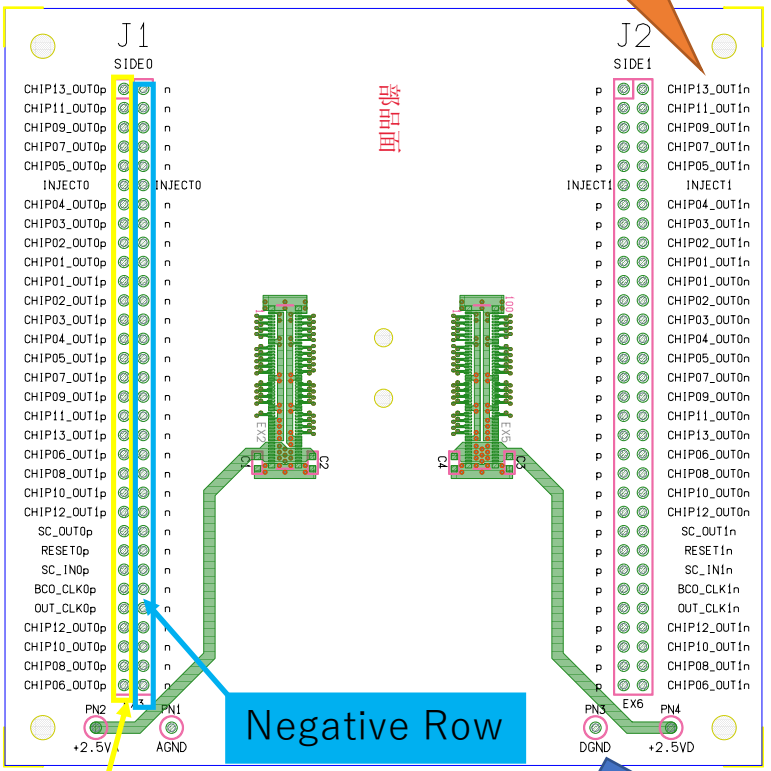


Front Side

Chip-1~13

Chip-14~26

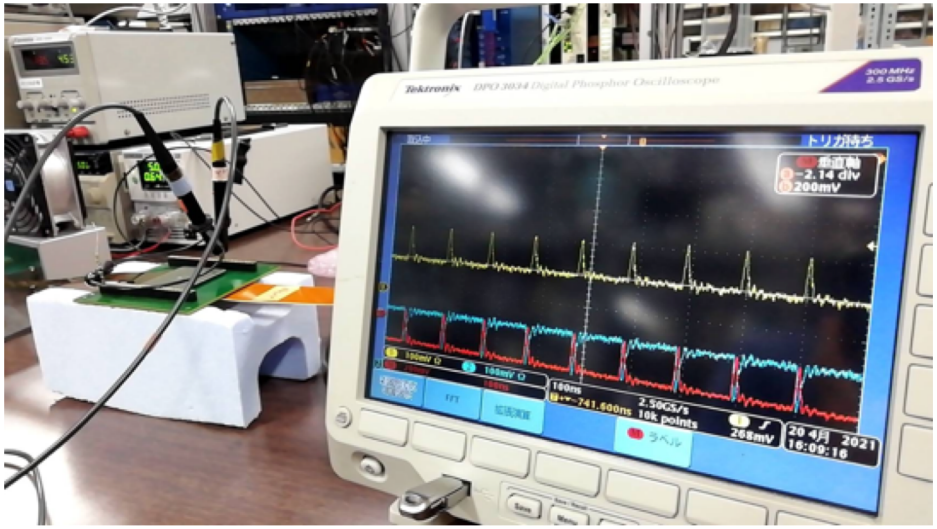
Add +13 to translate to chip-ID

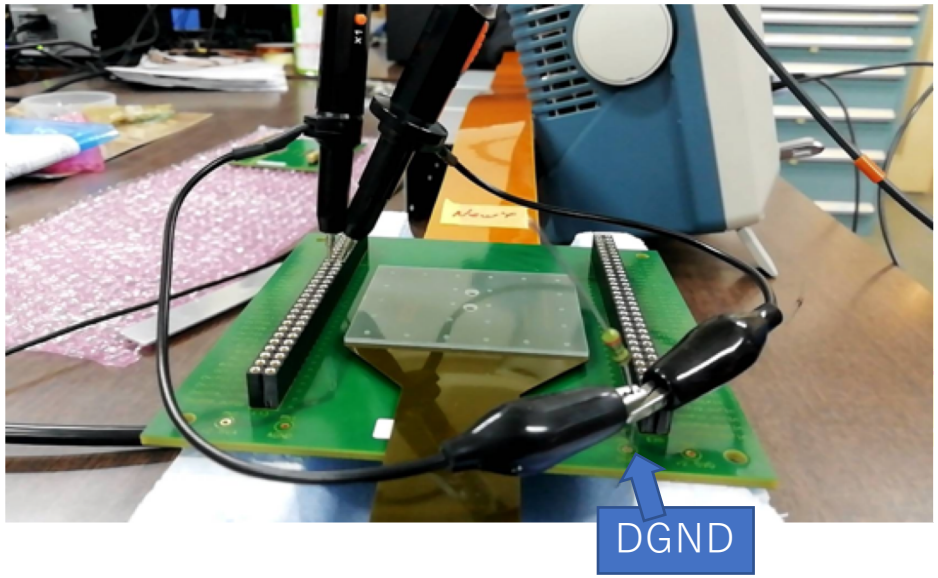


Positive Row

Oscillroscope Setup

One probe plug into positive side and another one is to be plugged into negative side. The ground can be connected to DGND. Simultaneous probing is not mandatory. If you find it is quicker to pursue check with a single probe, go ahead.





How the data stream look like

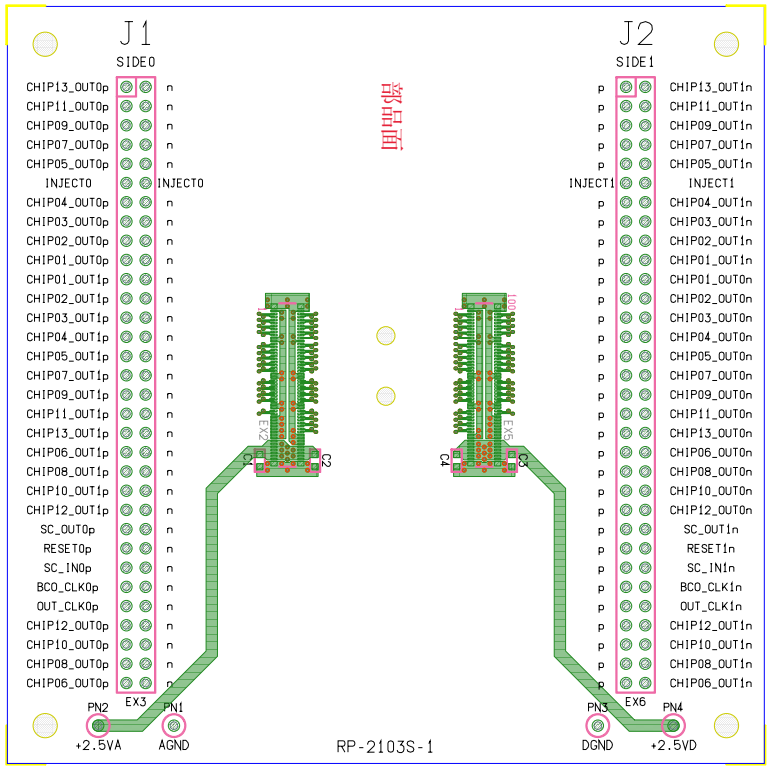
Impedance setting better be 1MΩ

Once you press the FFR button (this button initializes FPHX chip), all FPHX chips should start issuing this default pattern. If you observe this pattern, the line is alive.

If you find an open line, the module suppose to be ranked lower. Please keep recording in the database.

Can we probe all signal lines?

The short answer is ”NO”

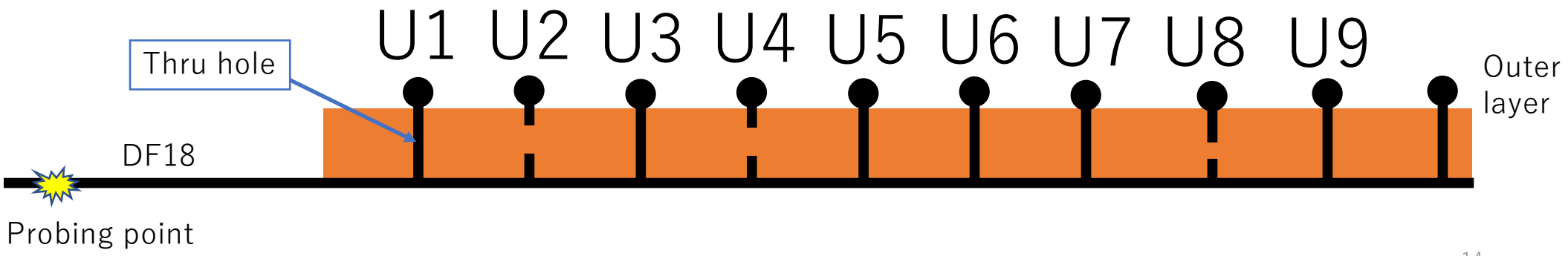


- You should see BCLK signal in BCO lines. (perhaps OUT_CLK as well).
- INJECT won’t see signal unless you run the calibration.
- You will see one shot data transmission in SC_** when you change any parameter like DAC threshold, LVDS amplitude, etc.
- There is a trick to get signal out from SC_OUT. Leave it for now.

The procedure will be updated accordingly as further investigation proceeds in NWU.

What to do with SC lines?

- SC lines are important not to mention. Here is the idea how to probe SC thruholes.
- Since SC lines are shared by 13 chips through daisy chain as illustrated below. We can probe each thruholes by proving the ”readback” response from each FPHX chip.
- This process better be somewhat automated, so a macro will be developed in NWU.



Interception Board Shipping to BNL

- Paper works is ready.
- Pick up date is arranged to be May 12th.
- No connection jig neighther, sorry.