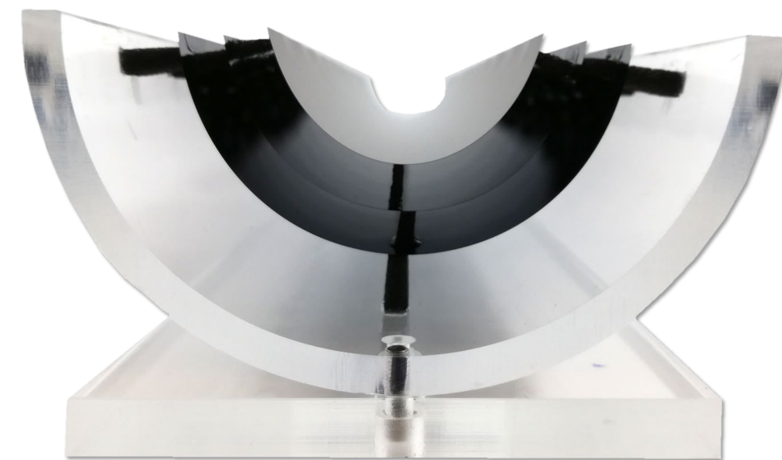
ALICE ITS3 WP3-4-5
Progress report



Giacomo Contin
Università di Trieste and INFN Sezione di Trieste

EIC Silicon Consortium meeting – May 17th 2021

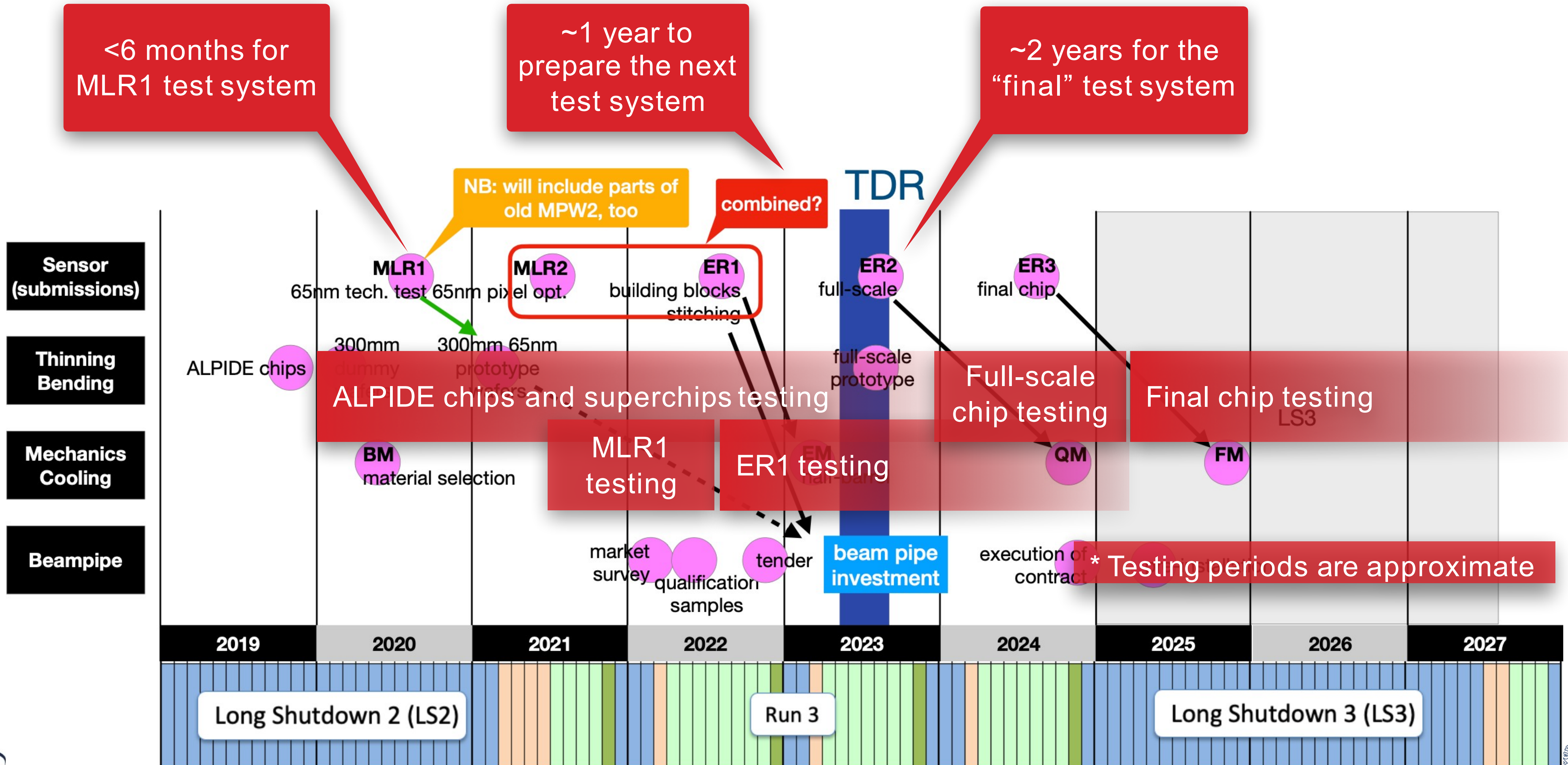
ALICE

INFN TRIESTE

Summary

- MLR1 Testing campaign plans
- ALPIDE-based DUT Testbeams
- Larger-size chip Thinning, Bending and Interconnections
- Mechanics development

ITS3 project timeline: testing



Testing of MLR1 pixel matrices

From June and for ~1 year

- Short time to prepare the test system and short usage time → avoid custom solutions
- Provide feedback for ER1 quickly → distribute the characterisation workload
- **Solutions**: several “carrier cards” + “proximity board”
  - Existing test system, or
  - General purpose components (oscilloscopes, dev boards…)
- **To keep in mind:**
  - Testbeams, bending tests, irradiation, yield…
  - >100 chips on “carrier card”/“proximity boards” & ~20 test systems

X 4 (APTS, DPTS, CE65, CA)

Testing plan & timeline summary

Miko Suljic @ ITS3 Plenary 23.04.2021

- T_0 (June) = delivery of first batch of chips on carriers to testing sites participating in carrier design, software or firmware development
- T_0 + 3 weeks (early July) = decision on the next batch of chips to be bonded and distributed to all testing sites
- T_0 + 7 weeks (early August) = decision on the chip variants to be bonded and irradiated (TID) or bonded after irradiation (NIEL), bonded for further exploration of parameter phase space (APTS)

Testbeam slots:

- mid-Jul @ SPS
- end-Oct @ PS
- beg-Nov @ SPS

Chip testing phase space

Miko Suljic @ ITS3 Plenary 23.04.2021

APTS

#	Pitch (um)	Buffer	Coupling	Process
1	10	SF	DC	std
2	10	SF	DC	mod
3	10	SF	DC	gap
4	15	SF	DC	std
5	15	SF	DC	mod
6	15	SF	DC	gap
7	20	SF	DC	std
8	20	SF	DC	mod
9	20	SF	DC	gap
10	25	SF	DC	std
11	25	SF	DC	mod
12	25	SF	DC	gap
13	10	SF	AC	std
14	10	SF	AC	mod
15	10	SF	AC	gap
16	20	SF	AC	std
17	20	SF	AC	mod
18	20	SF	AC	gap

#	Pitch (um)	Buffer	Coupling	Process
19	10	SF+amp	DC	std
20	10	SF+amp	DC	mod
21	10	SF+amp	DC	gap
22	20	SF+amp	DC	std
23	20	SF+amp	DC	mod
24	20	SF+amp	DC	gap
25	10	SF+amp	AC	std
26	10	SF+amp	AC	mod
27	10	SF+amp	AC	gap
28	20	SF+amp	AC	std
29	20	SF+amp	AC	mod
30	20	SF+amp	AC	gap
31	10	OPAMP	DC	std
32	10	OPAMP	DC	mod
33	10	OPAMP	DC	gap
34	10	OPAMP	AC	std
35	10	OPAMP	AC	mod
36	10	OPAMP	AC	gap
37	10	SF mux	DC	gap
38	20	SF mux	DC	gap

CE65

#	Pitch (um)	Buffer [coupling]	Process
A	15	Amp [AC], Amp [DC], SF [DC]	std
B	15	Amp [AC], Amp [DC], SF [DC]	gap
C	15	Amp [AC], Amp [DC], SF [DC]	Mod
D	25	Amp [AC], Amp [DC], SF [DC]	std

DPTS

#	Pitch (um)	Variant
1	15	Base
2	15	Column cross connect
3	15	column cross connect, shorted DVSS AVSS

To test on splits 1 & 4

To test on split 4

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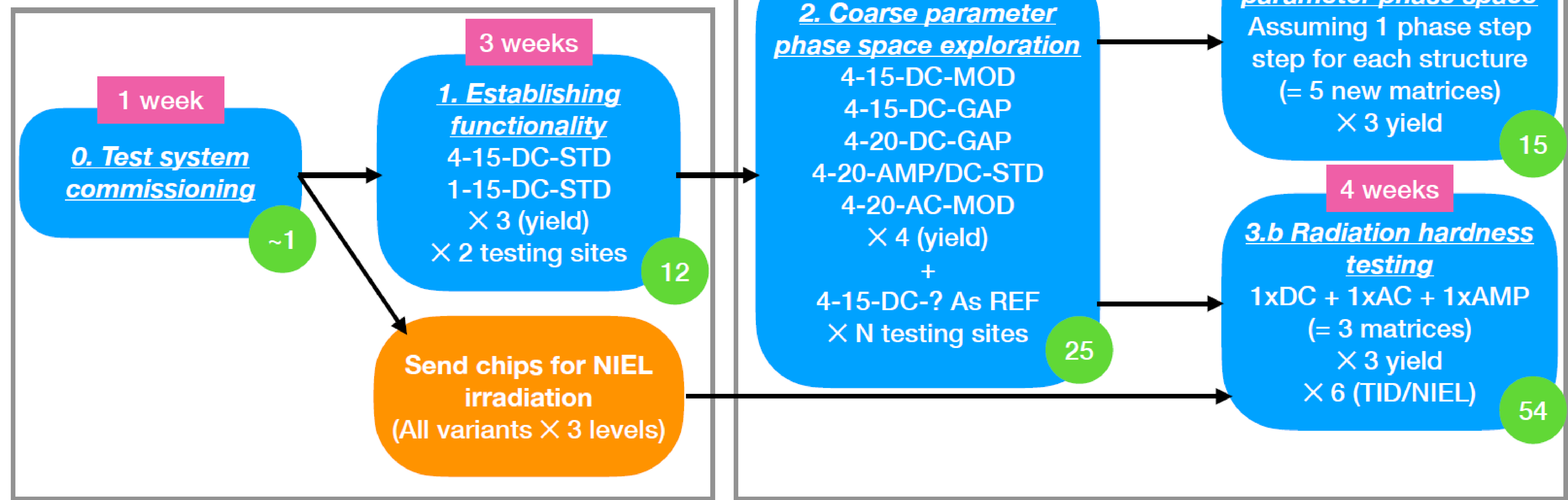
APTS SF (Low sampling rate)



1st carrier production (~15)

2nd carrier production (~100)

1st bonding (~12)

2nd bonding (~25)

3rd bonding (~70)

N carrier + spares!

Time to provide first feedback

TBD: # testing sites

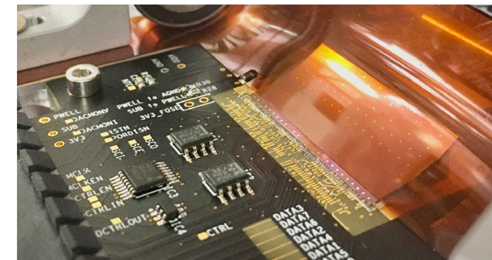
Miko Suljic @ ITS3 Plenary 23.04.2021

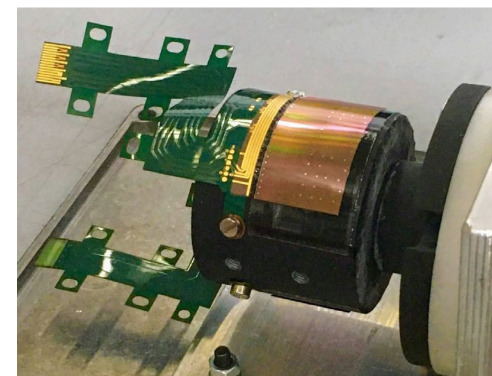
Naming: split-pitch-coupling-process

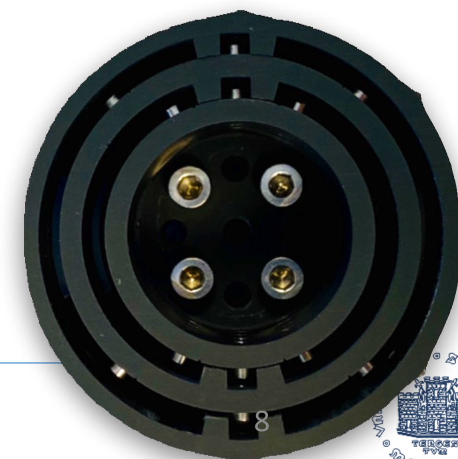
Bent ALPIDE testing

From now to ~next year

- Feasibility tests - **Done**
  - First tests in spring last year, next beam tests in July @SPS
- Test of chips bent in various directions - **Mostly done**
  - Lab and beam tests with wire bonded chips - done
  - SpTab bonded chips bent in lab - ongoing
  - μITS3 (6 bent chips, various radii) – partially done
- Test bent ALPIDE-Superchips - **ongoing**
  - Diced portions of wafers containing many ALPIDE reticles
  - Connection to existing test system & powering scheme being produced

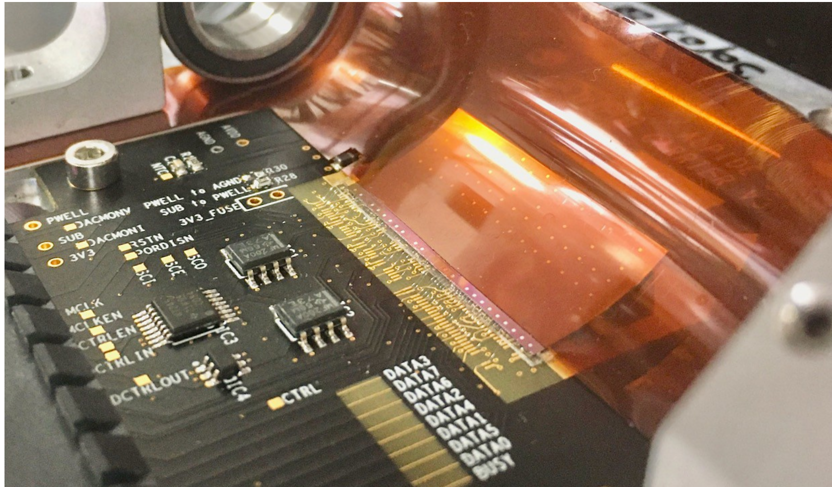




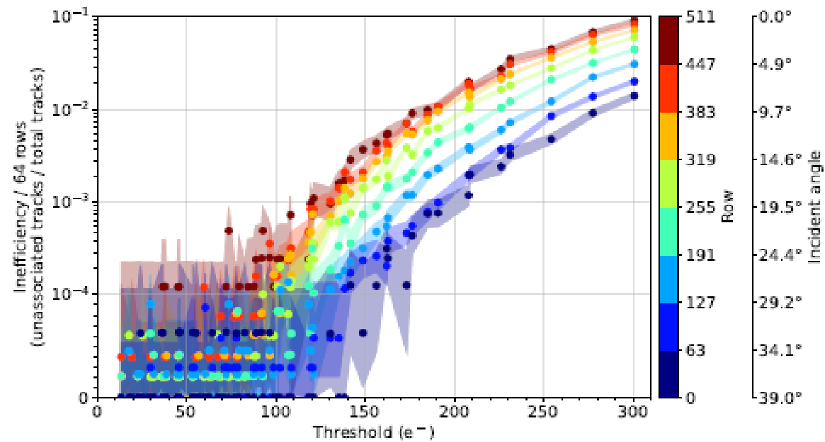


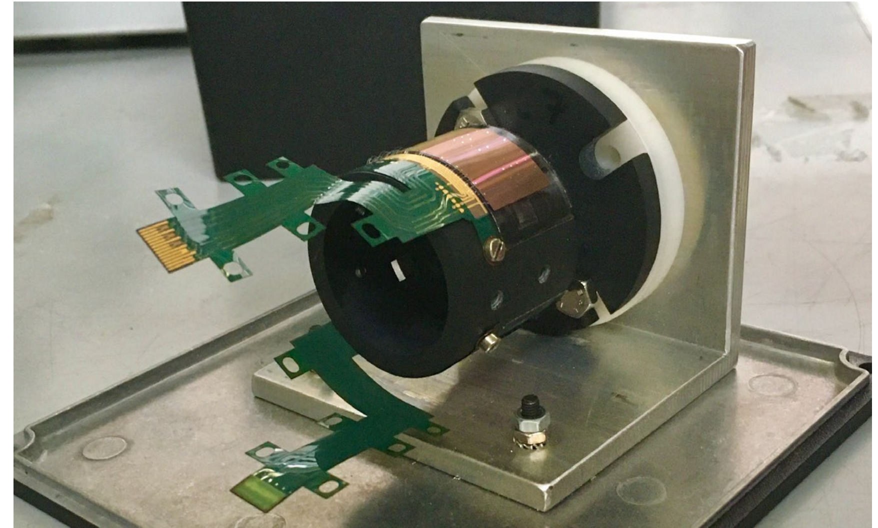
2020 Testbeams

Bent ALPIDE
(short side)
18-22 mm radius

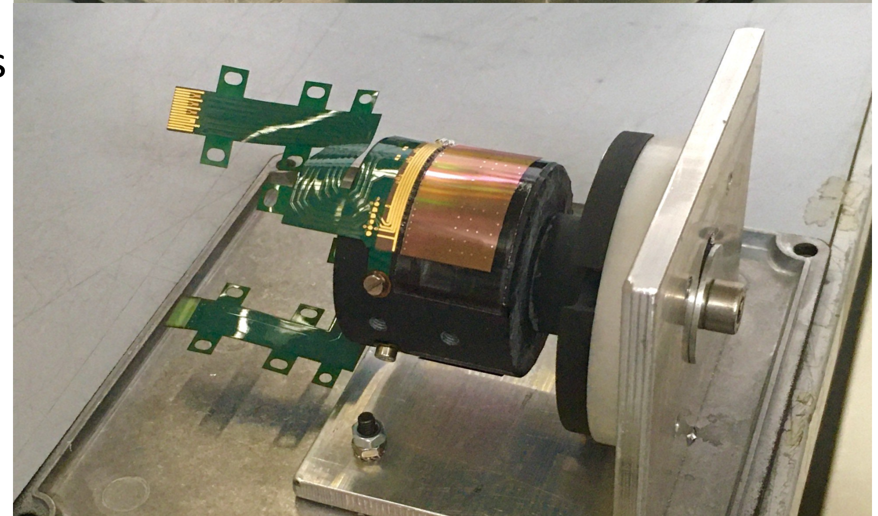


Measured inefficiency Vs Threshold (and Row)





Bent ALPIDE
(long side)
18 mm radius



Single-crossing configuration

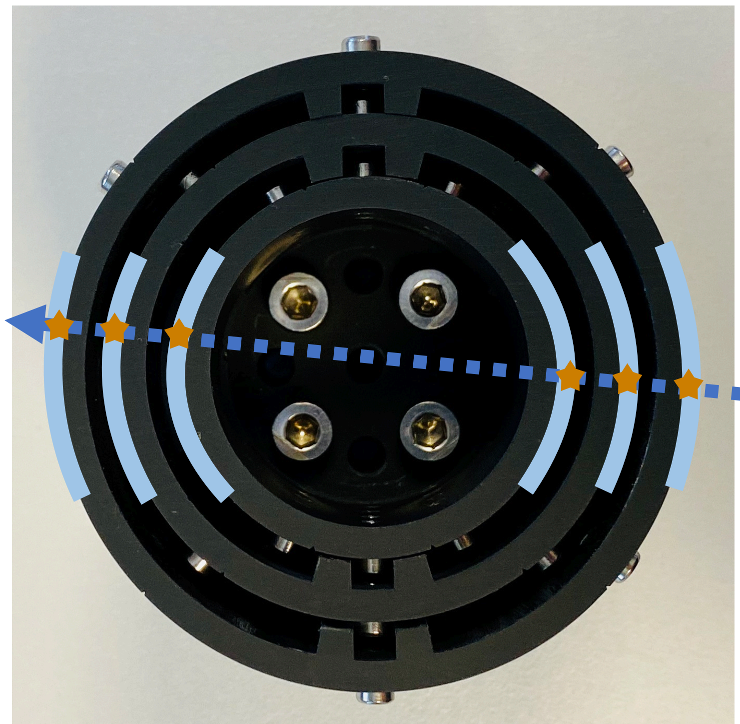
Standard setup

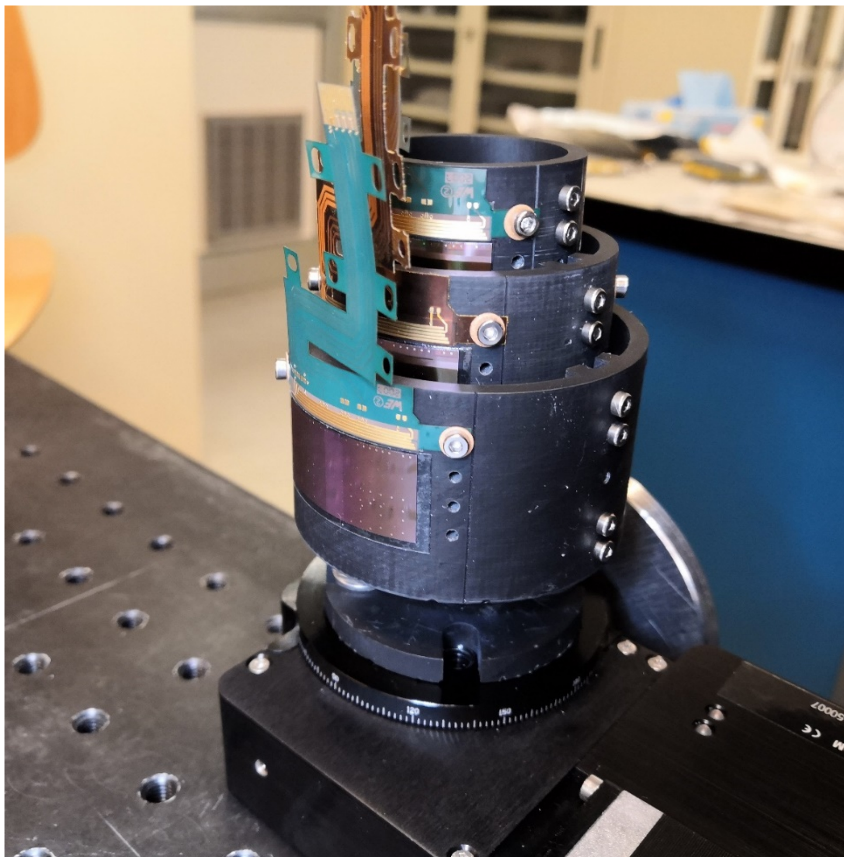
Beam

Double-crossing configuration

April 2021 Testbeam: 3-layer micro-ITS3

- Chips exposed for visibility

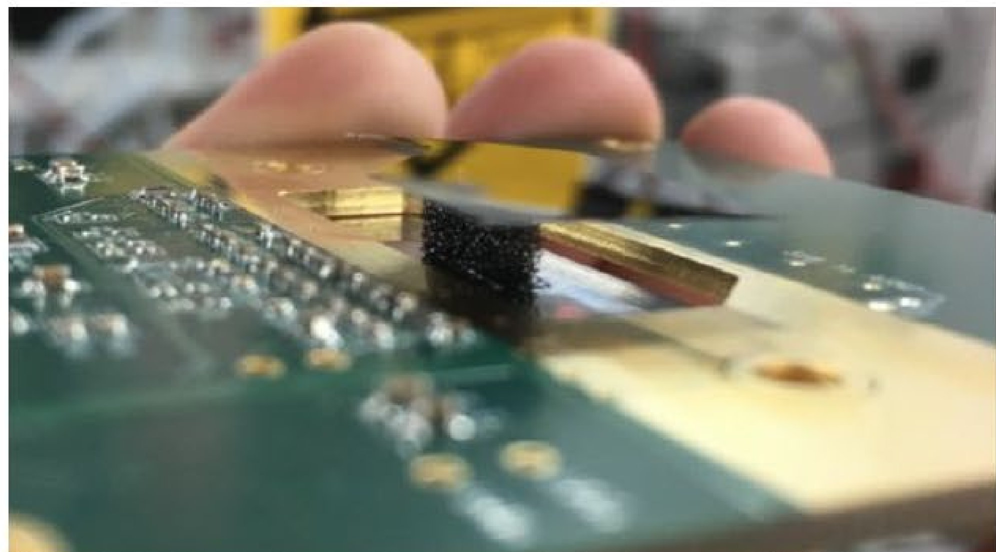


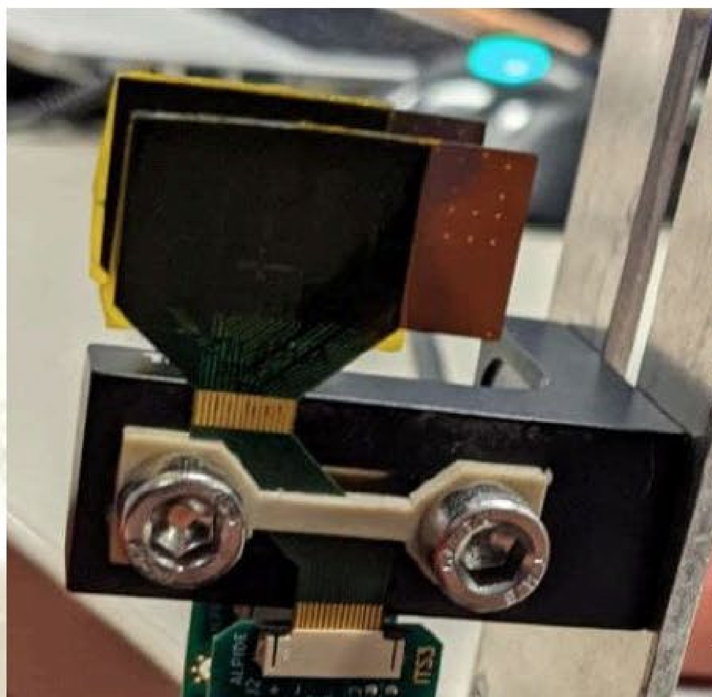


Goals

Lukas Lautner @ ITS3 WP3 04.05.2021

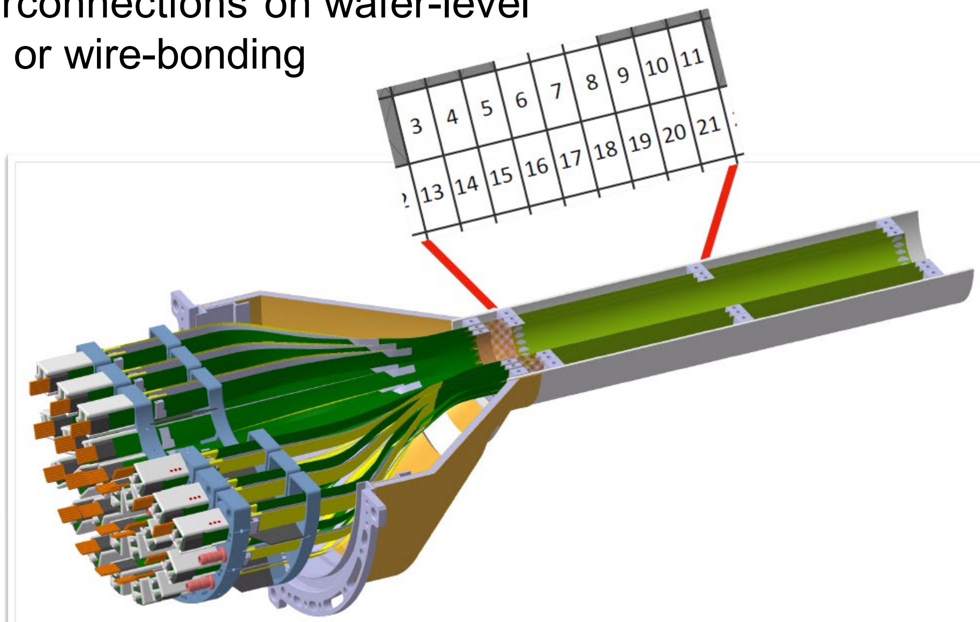
- 3 ALPIDE telescope
  → µITS3 (4 layers: L0B, L0T, L1T, L2T)
  → carbon foam
  → normal bent setup / parallel ALPIDE / ACF

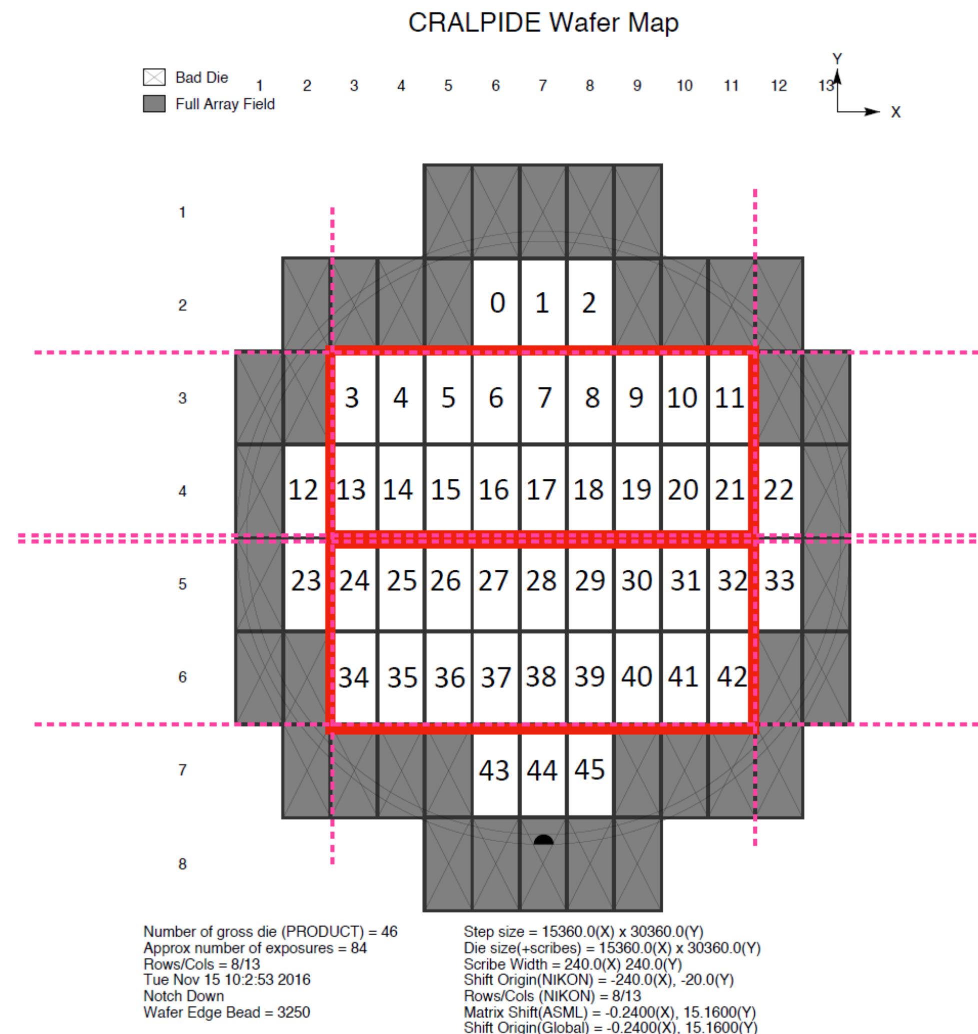




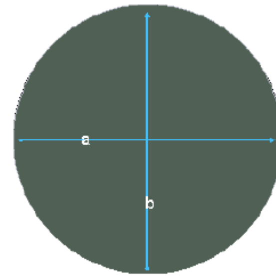
Moving to larger size: ALPIDE Super-chip

- Idea: cut out large “super chips” from a wafer
- about the area of 1/2 ITS3 half-layer 0
  - ~140 x 60 mm
- 9 x 2 chips
  - 9 interconnection areas in z-direction
- need individual connections:
  - no interconnections on wafer-level
  - SpTAB or wire-bonding



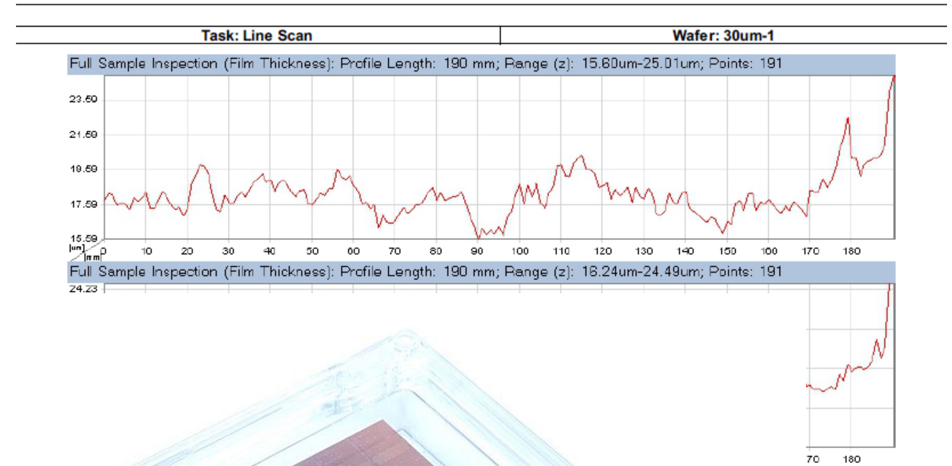


Super-ALPIDE project

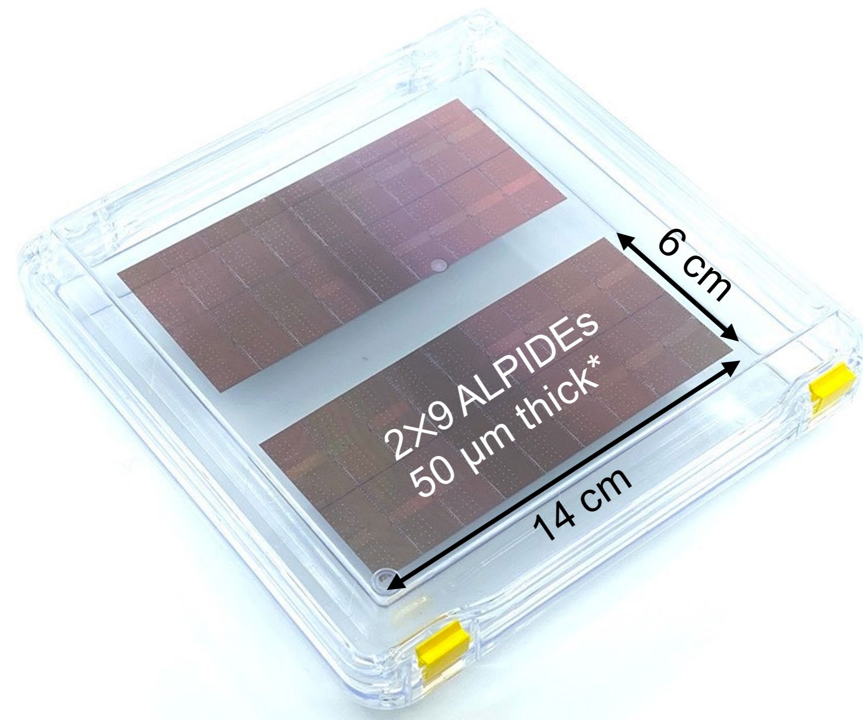


M. Mager @ ITS3 WP4

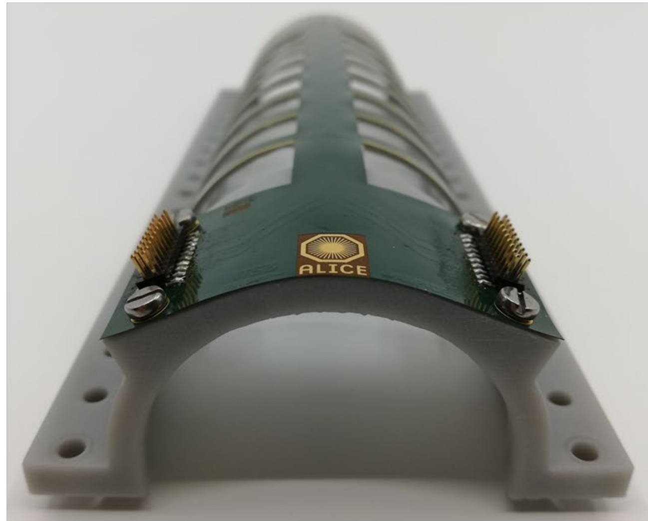
- Thinning and dicing
  - 30 – 40 – 50 µm / 9*2 ALPIDE matrix
  - 30 µm example, as measured by the thinning company through optical scan
    - 18.6 µm average with 1.4 µm st. dev
    - Does not include ~11 µm thick metal stack

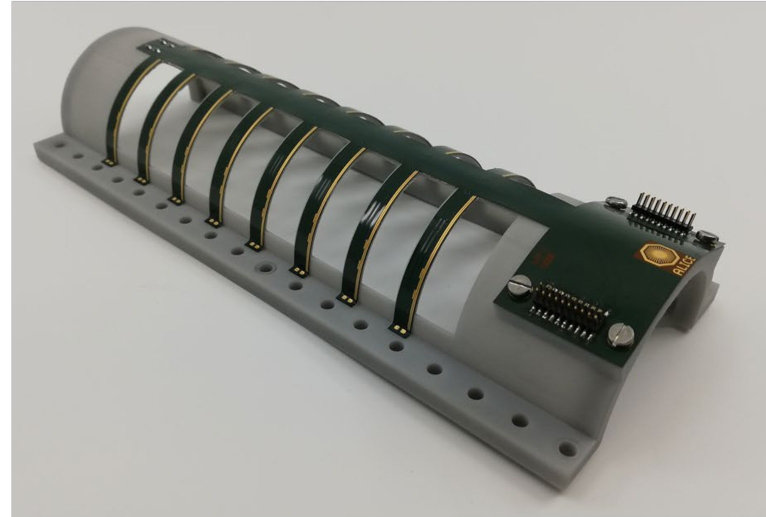


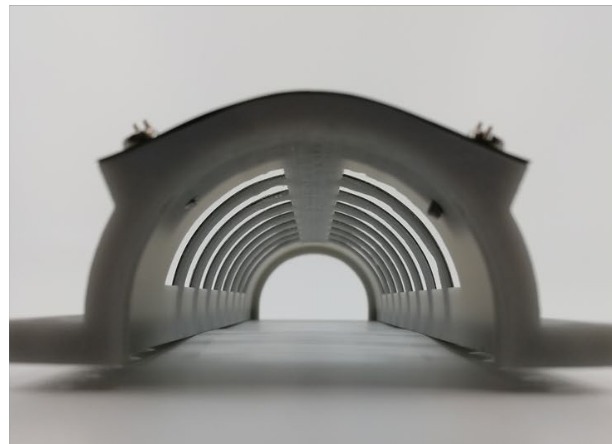
- Shipping membrane box for large size dice
  - Larger size needed for final size
  - To be optimized and validated

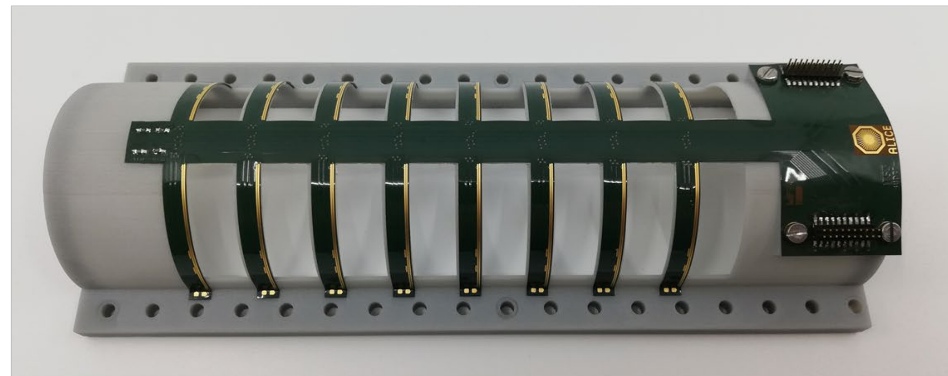


Super-ALPIDE project: FPC + Exoskeleton







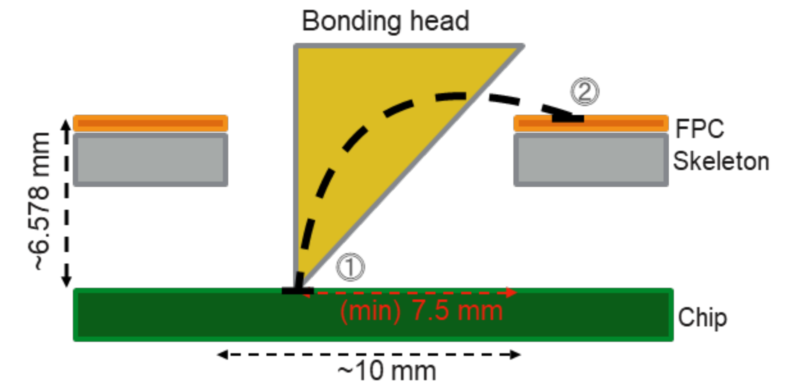


Dimensions, tolerance, details being optimized

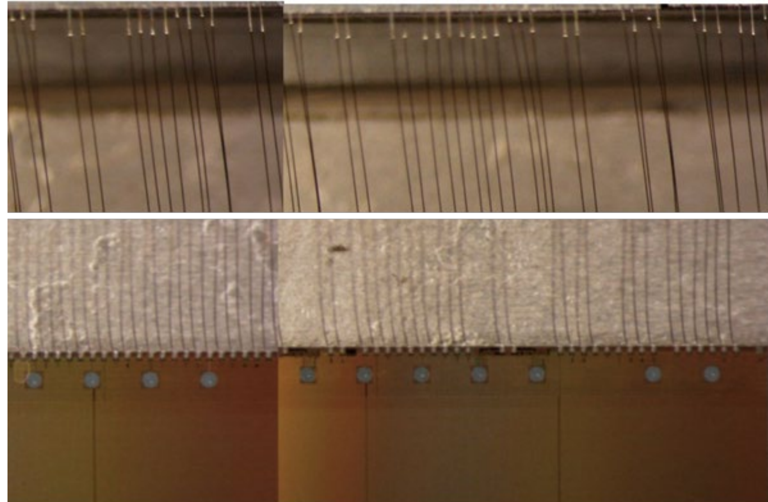
Super-ALPIDE: wire-bonding @ Bari

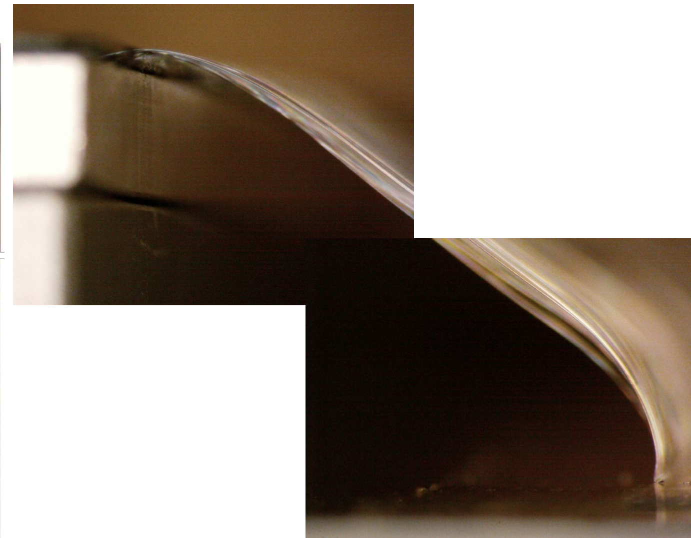
D. Colella @ ITS3 WP4

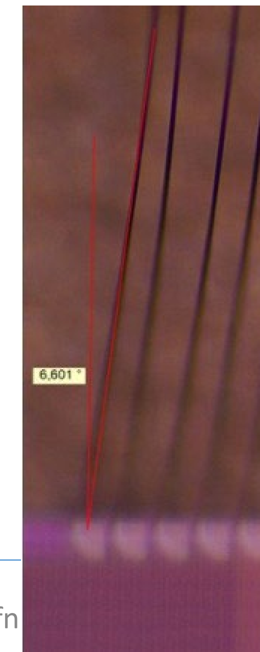
- Preliminary wire-bonding test on real ALPIDE, avoiding conflict between bonding head and FPC
  - Loop height: 6.6mm (target: ~ 8mm)
  - Distance between pads along z: 8.7mm
  - First soldering on chip (down), second on FPC (up)
  - Inter-pad bondable distance 220 μm = two consecutive small pads
  - 6 degrees angle between bonding pads direction and wire
  - Interference with previously soldered wires due to clamp dimensions
    → reduced by rotating the foot at chip pads by 15 degrees

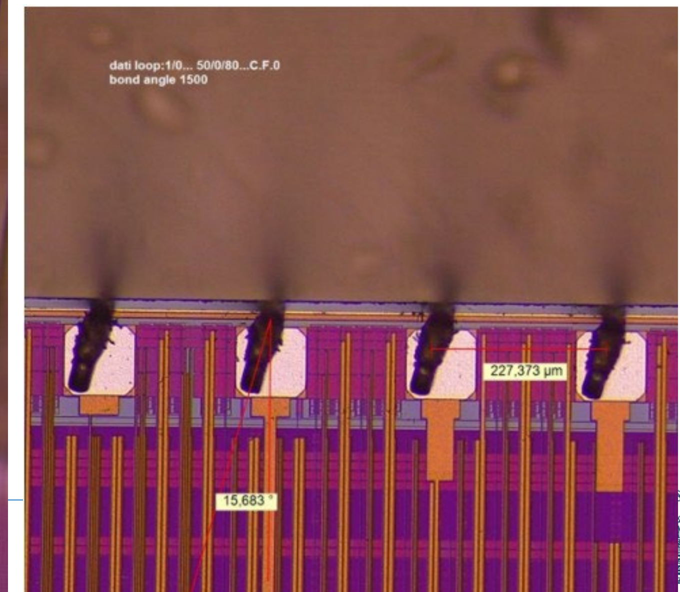


Domenico Colella - Bari







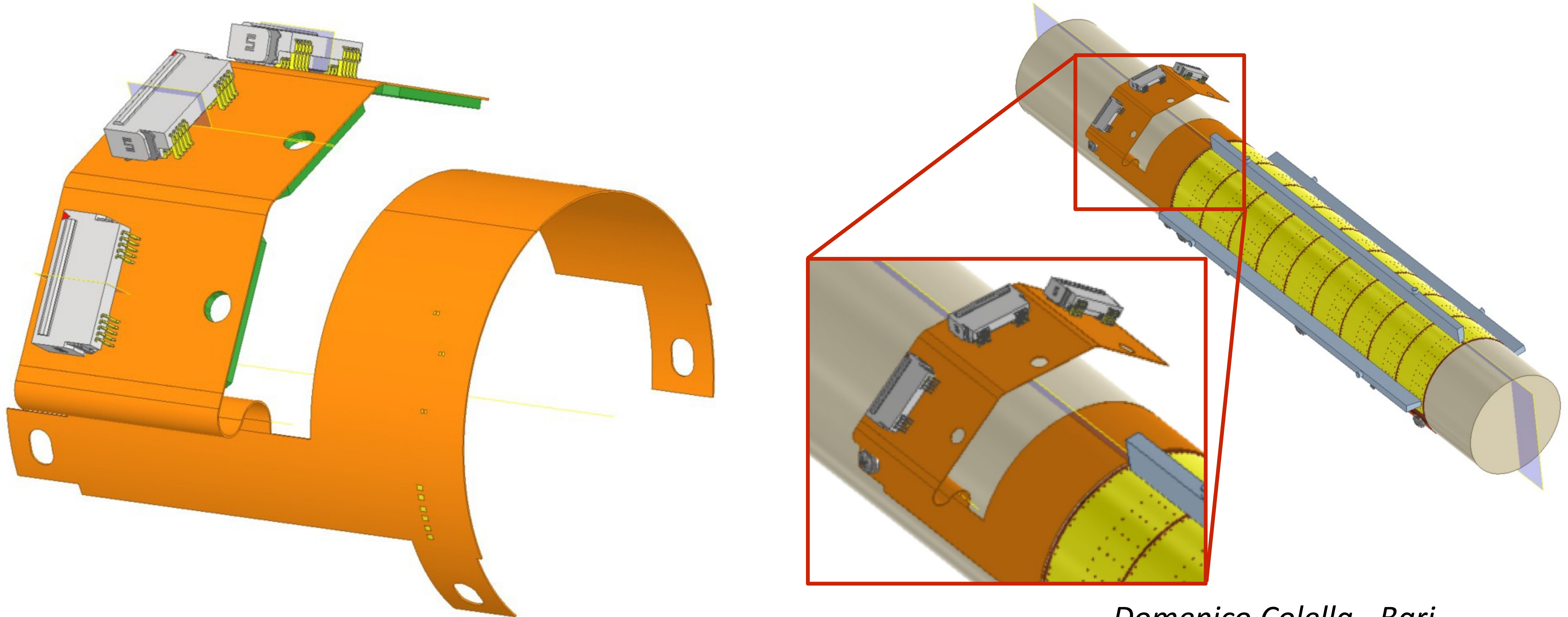


Super-ALPIDE Edge-FPC @ Bari

D. Colella @ ITS3 WP4

ALICE

- First prototype of the final front-edge ITS3 interconnections

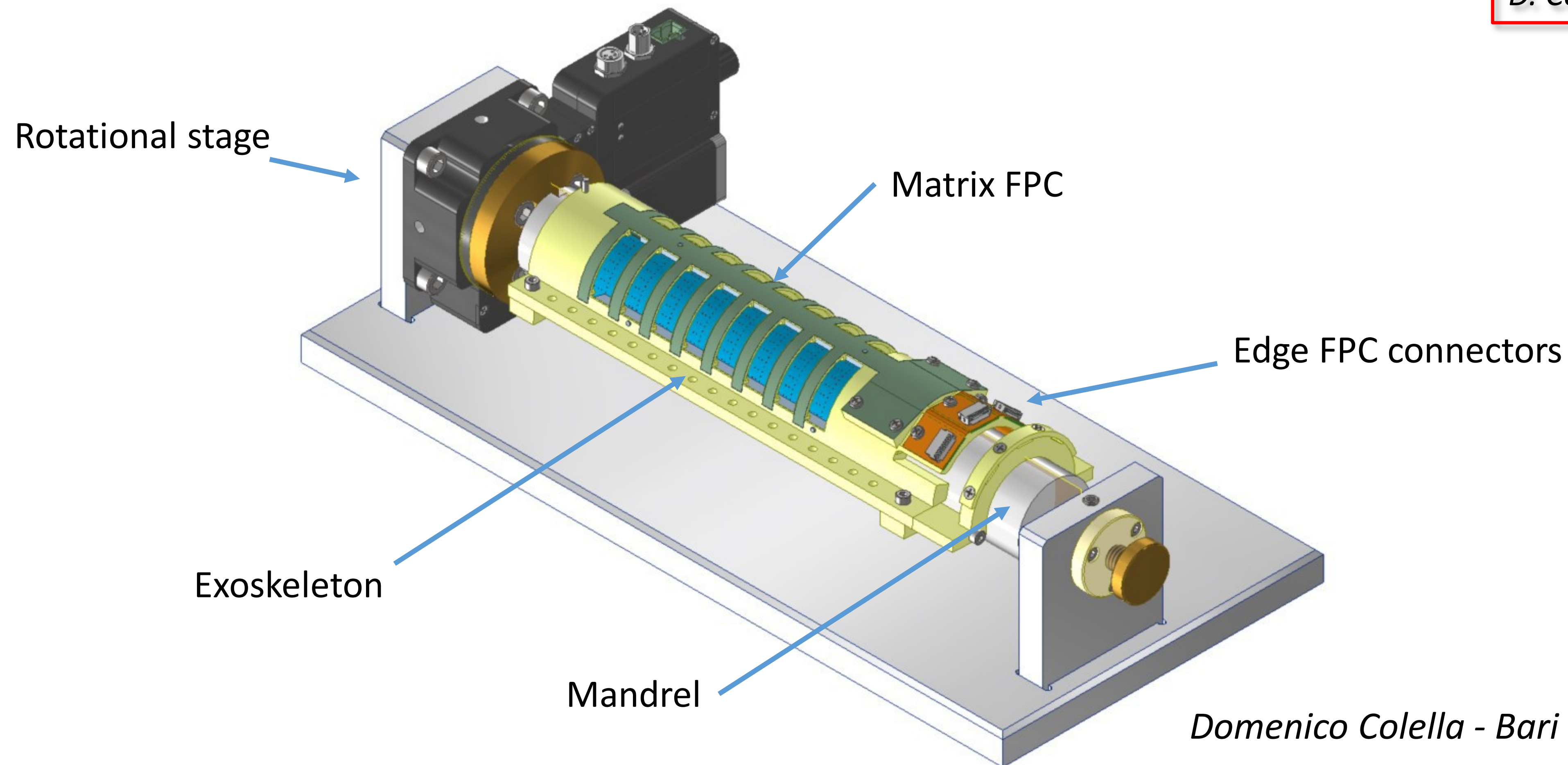


Domenico Colella - Bari

Super-ALPIDE wire-bonding setup @ Bari

- Component design being finalized or already in production

D. Colella @ ITS3 WP4



Domenico Colella - Bari

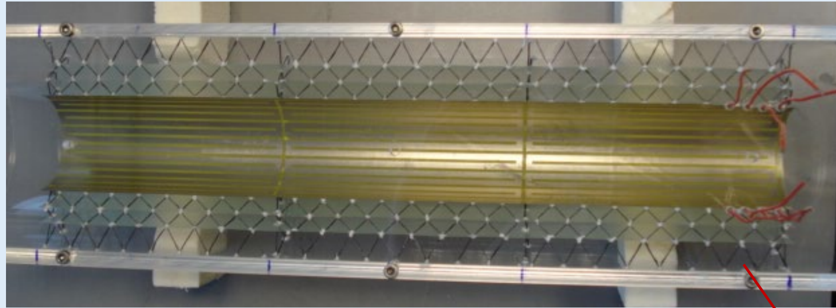
BBM: BBM1 and BBM2

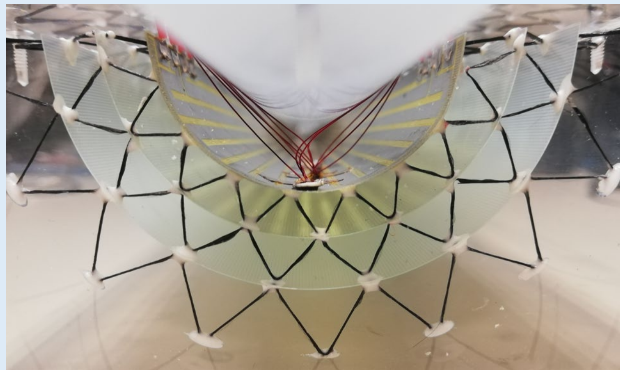
C. Gargiulo / M. Angeletti @ ITS3 Plenary 23.04.2021

BBM1 DONE

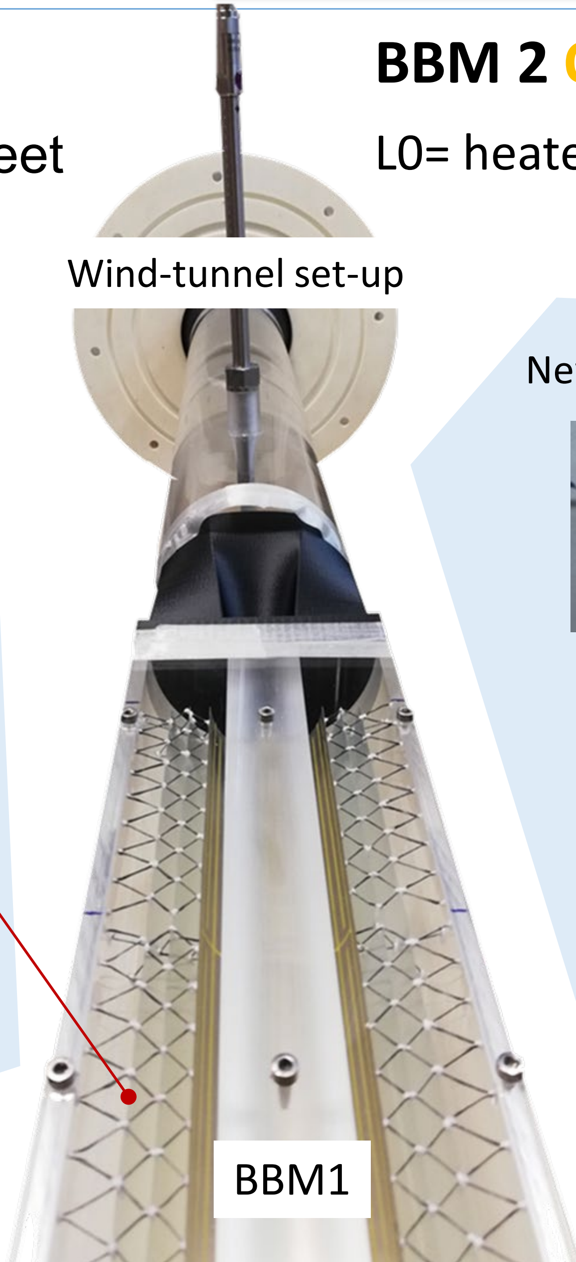
L0= heater; L1= G10 sheet; L2=G10 sheet

3 dummy layers (fiberglass), first equipped with kapton heaters





Wind-tunnel set-up

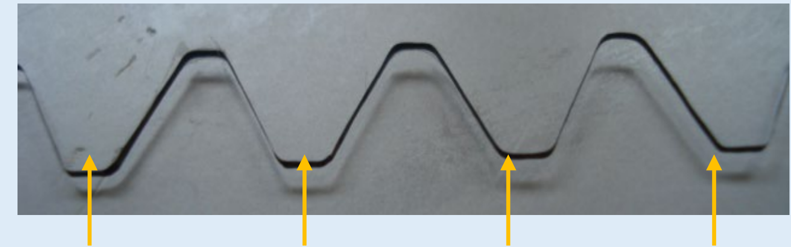


BBM1

BBM 2 ONGOING

L0= heater; L1= heater; L2= heater

New CFRP support design for BBM2 (Plan B for EM)



- Flat edges to minimize glue but have a reasonable gluing area.
- Cross section 1x0.05 mm2

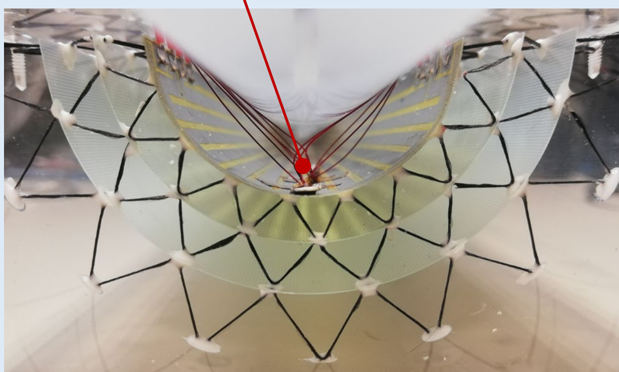
@NIKHEF

BBM: wind tunnel test

C. Gargiulo / M. Angeletti @ ITS3 Plenary 23.04.2021

BBM1 Ready for preliminary Test in wind tunnel

L0 equipped with 3 PT1000 temperature sensors.

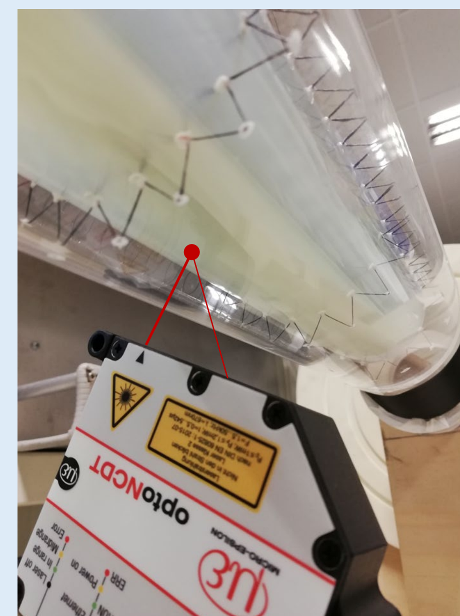


Wind-tunnel set-up

BBM1

Next implementation of ..

Laser displacement sensor
Micro-Epsilon ILD2300-20LL
Resolution 0.3micron



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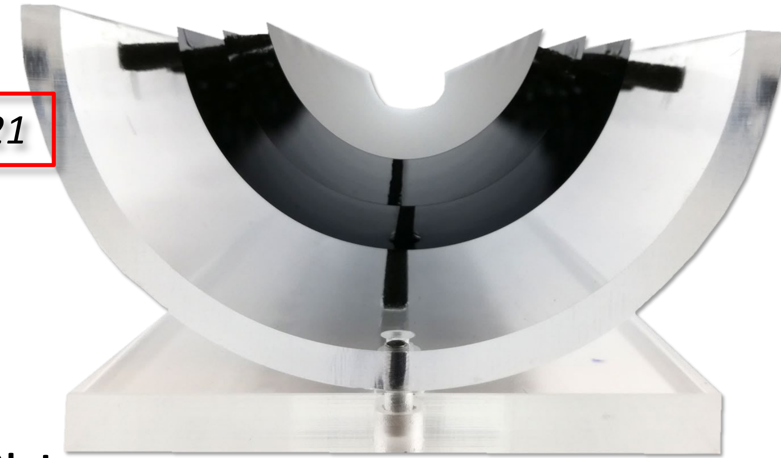
Highlights: Engineering model 1 --> Fully assembled

The first half barrel model with dummy silicon HLS at nominal radius has been completed.

Items	Th. [um]	L [mm]	Circ. [mm]
L0	50	280	56.5
L1	40	280	74.4
L2	40	280	93.2

C. Gargiulo / M. Angeletti @ ITS3 Plenary 23.04.2021



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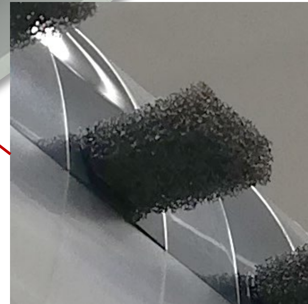
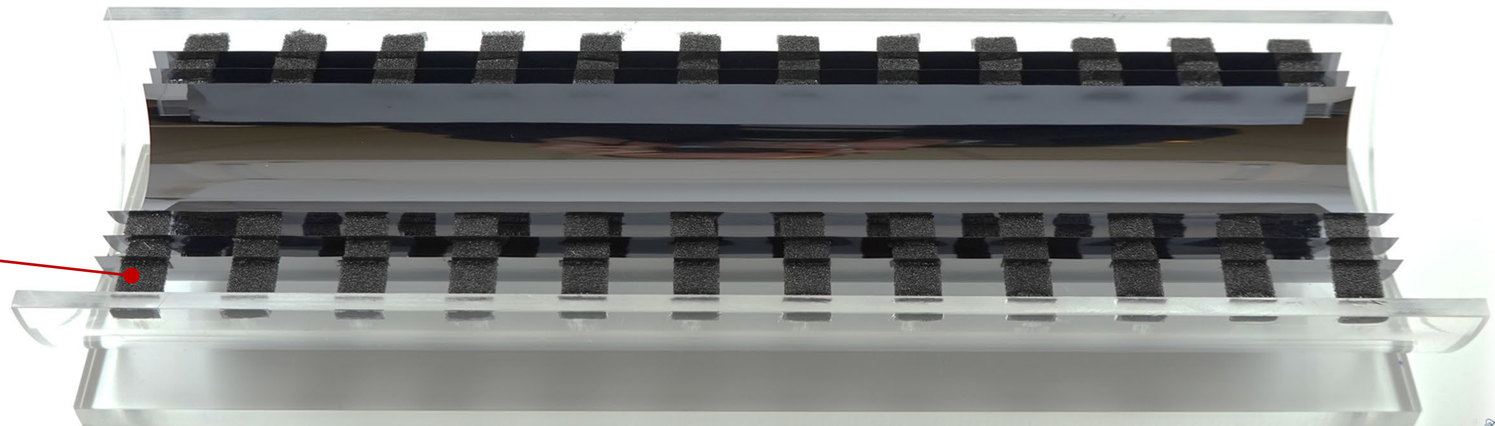


@Duocell ERG wedge



Notes:

- Layers' position guaranteed by small foam wedges only;
- 50µm thick L0 has been used to demonstrate bendability (min radius)

EM1: Improvement of sensor interface to support

Across wedges

Bending

Below wedges

footprint

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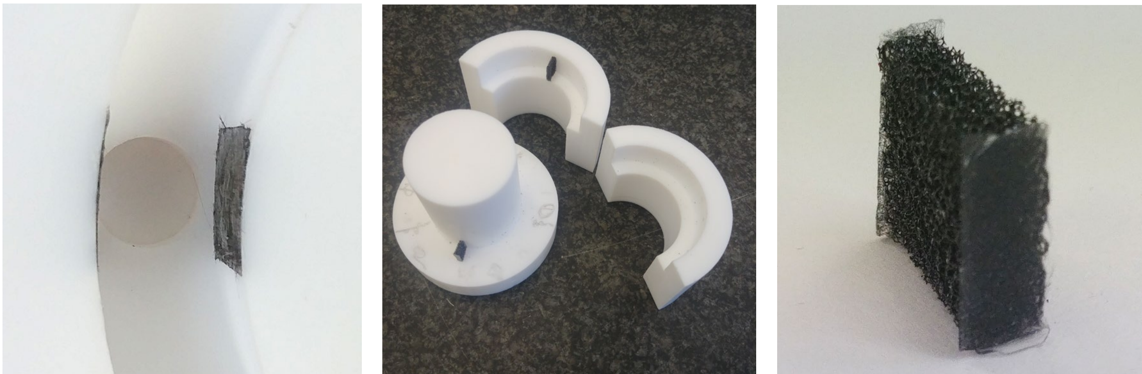

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ongoing

MINIMIZE footprint→ special preparation of carbon foam/fleece (also to reduce glue)

MINIMIZE bending → enlarge contact surface i.e. increase number of wedges; continuous wedge (requires vacuum chuck).

Hybrid solution with Al porus vacuum chuck and thin FINGER-maylar foil under investigation

Possible engagements in ITS3 WPs towards EIC dev.

- MLR1 test structure and small matrix characterization
  - ➢ Test setup development and sensor characterization for EIC
- Large sensor thinning/bending/interconnections
  - ➢ Development for EIC vertex radii/dimensions
- Mechanics and cooling development
  - ➢ Development for EIC vertex radii/dimensions
  - ➢ Integration with EIC services