ALICE ITS3 WP3-4-5 Progress report

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Università di Trieste and INFN Sezione di Trieste

EIC Silicon Consortium meeting – May 17th 2021
Summary

- MLR1 Testing campaign plans
- ALPIDE-based DUT Testbeams
- Larger-size chip Thinning, Bending and Interconnections
- Mechanics development
ALPIDE chips and superchips testing

<6 months for MLR1 test system

~1 year to prepare the next test system

~2 years for the “final” test system

Testing periods are approximate

ITS3 project timeline: testing
Testing of MLR1 pixel matrices

- Short time to prepare the test system and short usage time → avoid custom solutions
- Provide feedback for ER1 quickly → distribute the characterisation workload

- **Solutions**: several “carrier cards” + “proximity board”
  - Existing test system, or
  - General purpose components (oscilloscopes, dev boards…)

- **To keep in mind**:
  - Testbeams, bending tests, irradiation, yield…
  - >100 chips on “carrier card”/“proximity boards” & ~20 test systems

X 4 (APTS, DPTS, CE65, CA)
Testing plan & timeline summary

- $T_0$ (June) = delivery of first batch of chips on carriers to testing sites participating in carrier design, software or firmware development

- $T_0 + 3$ weeks (early July) = decision on the next batch of chips to be bonded and distributed to all testing sites

- $T_0 + 7$ weeks (early August) = decision on the chip variants to be bonded and irradiated (TID) or bonded after irradiation (NIEL), bonded for further exploration of parameter phase space (APTS)

Testbeam slots:
- mid-Jul @ SPS
- end-Oct @ PS
- beg-Nov @ SPS
# Chip testing phase space

## APTS

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## DPTS

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To test on splits 1 & 4

To test on split 4
APTSD SF
(Low sampling rate)

1. Establishing functionality
   - 4-15-DC-STD
   - 1-15-DC-STD
   × 3 (yield)
   × 2 testing sites

2. Coarse parameter phase space exploration
   - 4-15-DC-MOD
   - 4-15-DC-GAP
   - 4-20-DC-GAP
   - 4-20-AMP/DC-STD
   × 4 (yield)
   + 4-15-DC-? As REF
   × N testing sites

3.a Fine tuning of parameter phase space
   - Assuming 1 phase step step for each structure
     (= 5 new matrices)
     × 3 yield

3.b Radiation hardness testing
   - 1xDC + 1xAC + 1xAMP
     (= 3 matrices)
     × 3 yield
     × 6 (TID/NIEL)

1st carrier production (~15)
1st bonding (~12)
2nd carrier production (~100)
2nd bonding (~25)
3rd bonding (~70)

N carrier + spares!
Time to provide first feedback
Naming: split-pitch-coupling-process

Miko Suljic @ ITS3 Plenary 23.04.2021
Bent ALPIDE testing

- Feasibility tests - **Done**
  - First tests in spring last year, next beam tests in July @SPS

- Test of chips bent in various directions - **Mostly done**
  - Lab and beam tests with wire bonded chips - **done**
  - SpTab bonded chips bent in lab - **ongoing**
  - µITS3 (6 bent chips, various radii) – **partially done**

- Test bent ALPIDE-Superchips - **ongoing**
  - Diced portions of wafers containing many ALPIDE reticles
  - Connection to existing test system & powering scheme **being produced**
2020 Testbeams

Bent ALPIDE (short side)
18-22 mm radius

Measured inefficiency Vs Threshold (and Row)

Bent ALPIDE (long side)
18 mm radius
Double-crossing configuration

Single-crossing configuration

Standard setup

Beam
April 2021 Testbeam: 3-layer micro-ITS3

- Chips exposed for visibility
Goals

- 3 ALPIDE telescope
  → μITS3 (4 layers: L0B, L0T, L1T, L2T)
  → carbon foam
  → normal bent setup / parallel ALPIDE / ACF
Moving to larger size: ALPIDE Super-chip

- Idea: cut out large “super chips” from a wafer
  - about the area of 1/2 ITS3 half-layer 0
    - ~140 x 60 mm
  - 9 x 2 chips
    - 9 interconnection areas in z-direction
  - need individual connections:
    - no interconnections on wafer-level
    - SpTAB or wire-bonding
Super-ALPIDE project

• Thinning and dicing
  • 30 – 40 – 50 µm / 9*2 ALPIDE matrix
  • 30 µm example, as measured by the thinning company through optical scan
    • 18.6 µm average with 1.4 µm st. dev
    • Does not include ~11 µm thick metal stack

• Shipping membrane box for large size dice
  • Larger size needed for final size
  • To be optimized and validated
Super-ALPIDE project: FPC + Exoskeleton

Dimensions, tolerance, details being optimized
Super-ALPIDE: wire-bonding @ Bari

- Preliminary wire-bonding test on real ALPIDE, avoiding conflict between bonding head and FPC
  - Loop height: 6.6mm (target: ~ 8mm)
  - Distance between pads along z: 8.7mm
  - First soldering on chip (down), second on FPC (up)
  - Inter-pad bondable distance 220 µm = two consecutive small pads
  - 6 degrees angle between bonding pads direction and wire
  - Interference with previously soldered wires due to clamp dimensions 
    → reduced by rotating the foot at chip pads by 15 degrees
Super-ALPIIDE Edge-FPC @ Bari

• First prototype of the final front-edge ITS3 interconnections
Super-ALPIDE wire-bonding setup @ Bari

- Component design being finalized or already in production

D. Colella @ ITS3 WP4

Rotational stage
Matrix FPC
Edge FPC connectors
Exoskeleton
Mandrel

Domenico Colella - Bari
BBM: BBM1 and BBM2

BBM1 DONE
L0 = heater; L1 = G10 sheet; L2 = G10 sheet

3 dummy layers (fiberglass), first equipped with kapton heaters

Wind-tunnel set-up

BBM 2 ONGOING
L0 = heater; L1 = heater; L2 = heater

New CFRP support design for BBM2 (Plan B for EM)

• Flat edges to minimize glue but have a reasonable gluing area.
• Cross section 1x0.05 mm²
**BBM: wind tunnel test**

**BBM1 Ready** for preliminary Test in wind tunnel

L0 equipped with 3 PT1000 temperature sensors.

Wind-tunnel set-up

Next implementation of ..

Laser displacement sensor
Micro-Epsilon ILD2300-20LL
Resolution 0.3micron

@CERN
Highlights: Engineering model 1 --> Fully assembled

The first half barrel model with dummy silicon HLS at nominal radius has been completed.

Notes:
- Layers’ position guaranteed by small foam wedges only;
- 50µm thick L0 has been used to demonstrate bendability (min radius)

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@Duocell ERG wedge

C. Gargiulo / M. Angeletti @ ITS3 Plenary 23.04.2021
EM1: Improvement of sensor interface to support

ongoing

MINIMIZE footprint $\rightarrow$ special preparation of carbon foam/fleece (also to reduce glue)

MINIMIZE bending $\rightarrow$ enlarge contact surface i.e. increase number of wedges; continuous wedge (requires vacuum chuck).

Hybrid solution with Al porous vacuum chuck and thin FINGER-maylar foil under investigation
Possible engagements in ITS3 WPs towards EIC dev.

• MLR1 test structure and small matrix characterization
  ➢ Test setup development and sensor characterization for EIC

• Large sensor thinning/bending/interconnections
  ➢ Development for EIC vertex radii/dimensions

• Mechanics and cooling development
  ➢ Development for EIC vertex radii/dimensions
  ➢ Integration with EIC services