ETROC: CMS ETL ReadOut Chip

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May 14, 2021, at LGAD-for-EIC discussion

ASIC design: The System Point of View

ASIC: Application Specific Integrated Circuit

ASIC: A System design that Includes a Chip

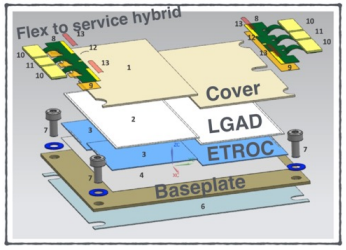
Proper System Design is the Key to the success of any challenging ASIC project

A good design is a compromise between system design and ASIC design

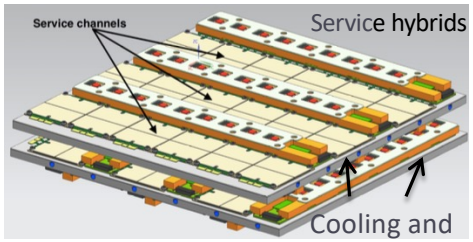
Need to think hard on system design to relax ASIC requirements

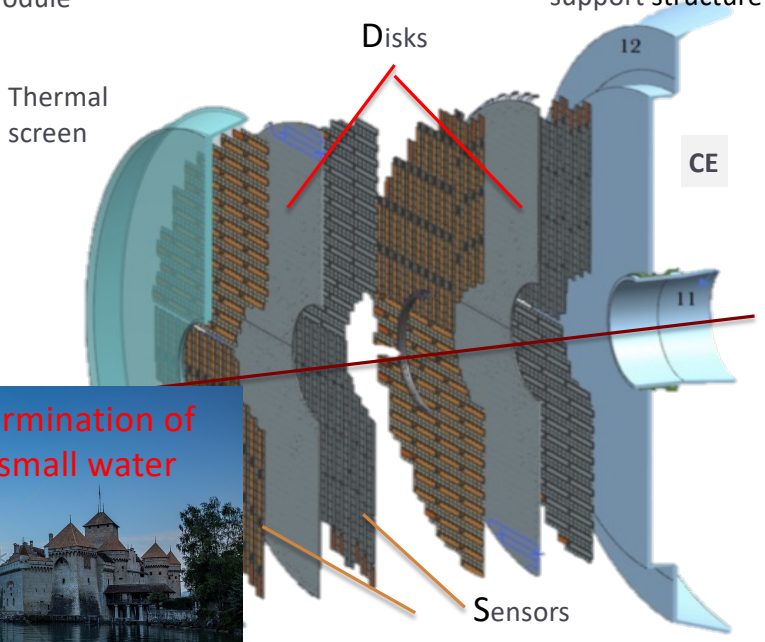
(multi-layers, more power/cooling budget, larger pixel size, ….)

ETL precision timing *challenges*



Module





- Low Gain Avalanche Detectors (LGADs)
  - 2x2 cm^2 LGAD bump-bonded to 2x2 cm^2 ETROC ASIC
  - Each pixel size: 1.3 mm x 1.3mm
  - Two layers/disks per endcap mounted on the HGC nose (~2 hits per track)
  - 50ps per hit → 35ps per track
  - 1.6 < |η| < 3.0, +- 3m
    surface ~14 m^2; ~8.5 M channels
  - Nominal fluence: ***1.6×10^{15} n_{eq}/cm^2*** (@ 3000 fb^{-1})
- LGAD gain modest: 10-30
  - Landau contribution: ~ 30-40ps
  - Front-end contribution kept < ~40ps
- ***Extract precision timing from***

  LGAD signal size: ~10 to 30 fC

  ~10 fC at end of operation (ETROC design: aim for 6fC)

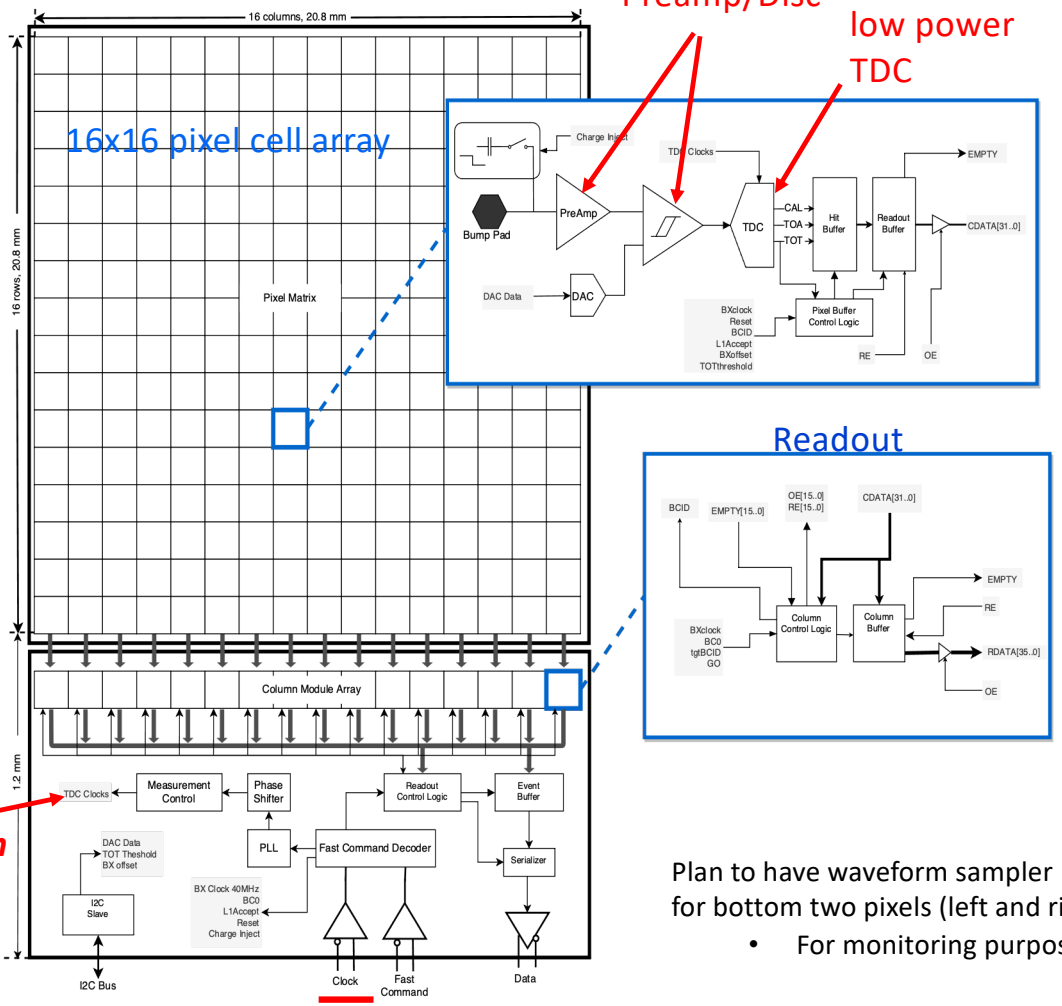
  With low power: ~1W/chip (2-3mW/channel)

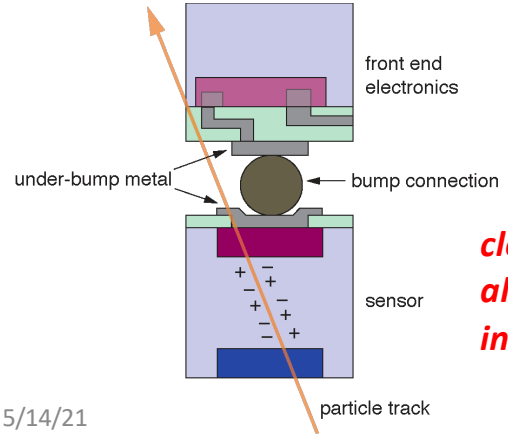
Total system power/cooling budget: <~40kW

ETROC bump-bonded to LGAD,
To handle 16x16 pixels
Each 1.3 mm x 1.3 mm

Power consumption < 1W/chip
(about ~2-3mW/pixel)
L1 buffer latency: 12.5 us
65nm

ETROC: ETL ReadOut Chip





clock distribution all the way into each pixel

Plan to have waveform sampler for bottom two pixels (left and right)

- For monitoring purpose

ETROC Development: *divide & conquer*

ETROC0: 1x1 pixel channel with preamp + discriminator (submitted Dec 2018)

Goal: core front-end analog performance

Done

ETROC1: 4x4 clock tree, preamp + discriminator + TDC (submitted Aug 2019)

Goal: full chain front-end with TDC, 4x4 clock tree

This is the first full chain precision timing prototype

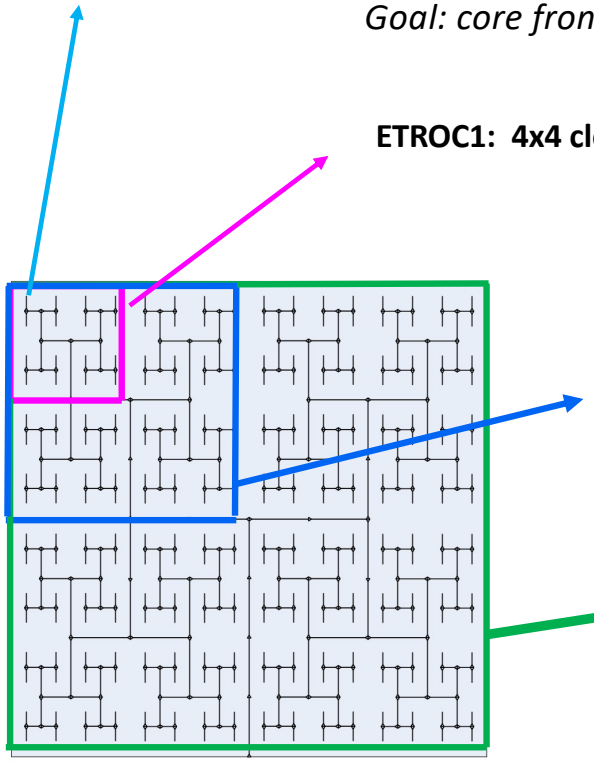
Beam test on going

ETROC2: 8x8 → 16x16, *full size & functionality* (late 2021)

Design on going

ETROC3: 16x16 (full size & functionality):

Goal: as pre-production



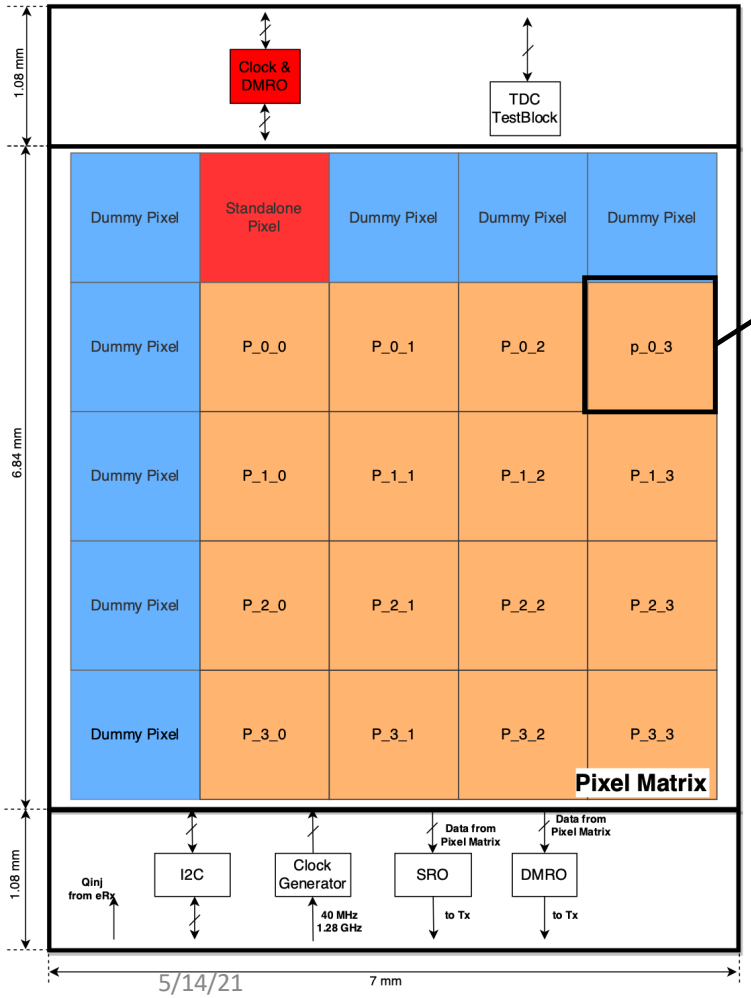
16 x 16 clock H-Tree

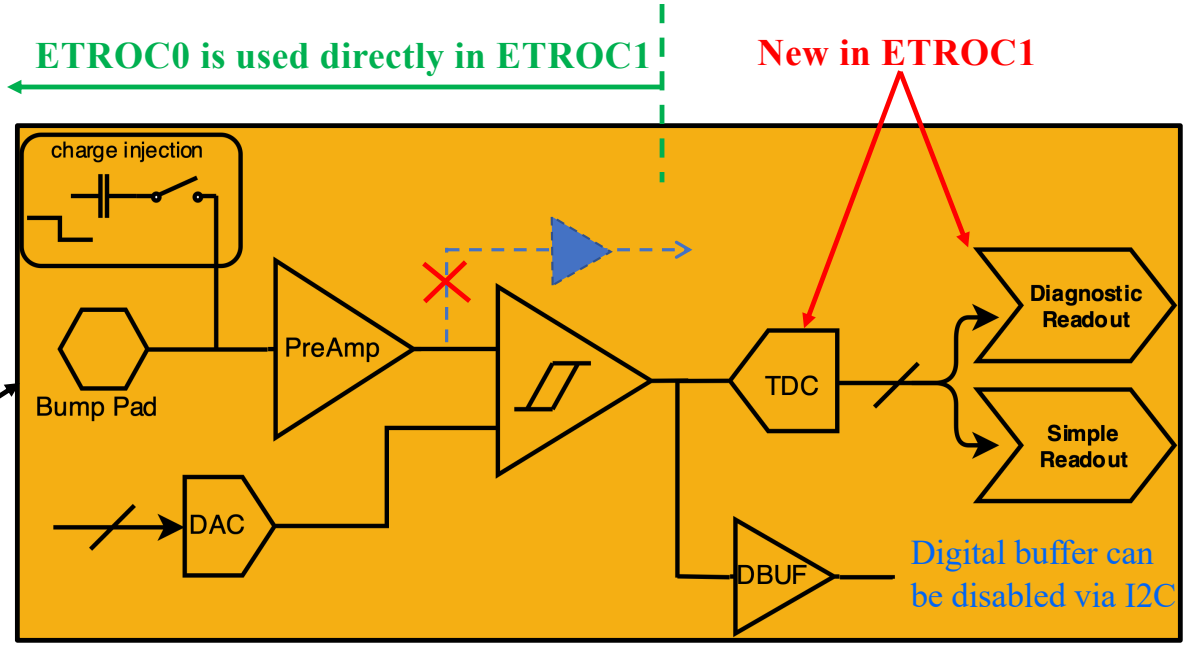
Design: FNAL/SMU/LBNL

Testing: + UIC/KNU/CNU

We have followed this plan since project started (Sept. 2018) …

Designed to be bump-bonded with 5x5 LGAD sensor



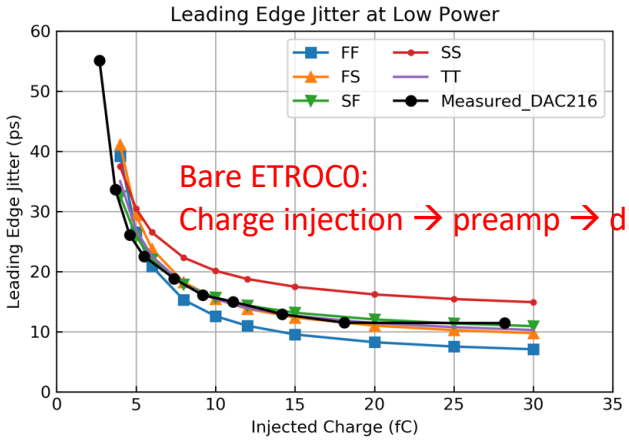


Bare ETROC1 testing has been very successful, performance is excellent and has been just as expected (wrt simulation), and at all levels.

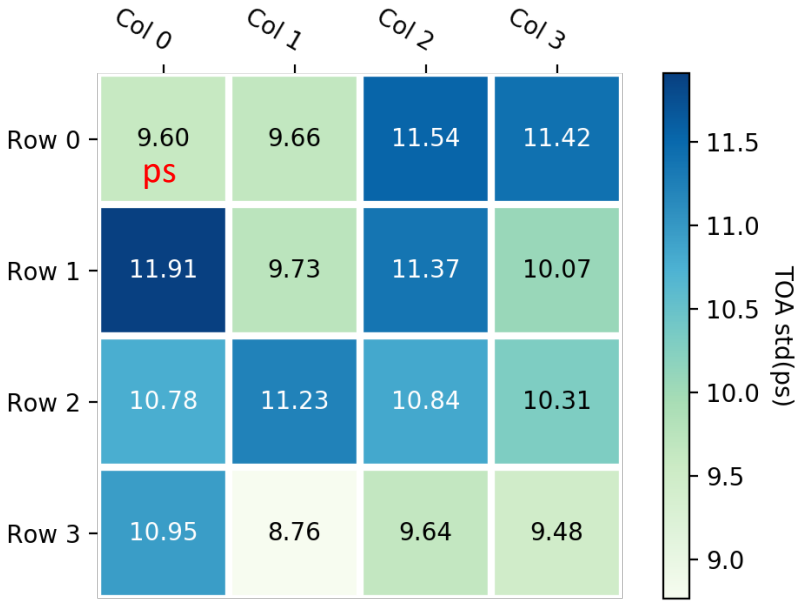
Bump bonded ETROC1 testing: encountered 40MHz noise issue, a subtle issue related to LGAD + ETROC interface

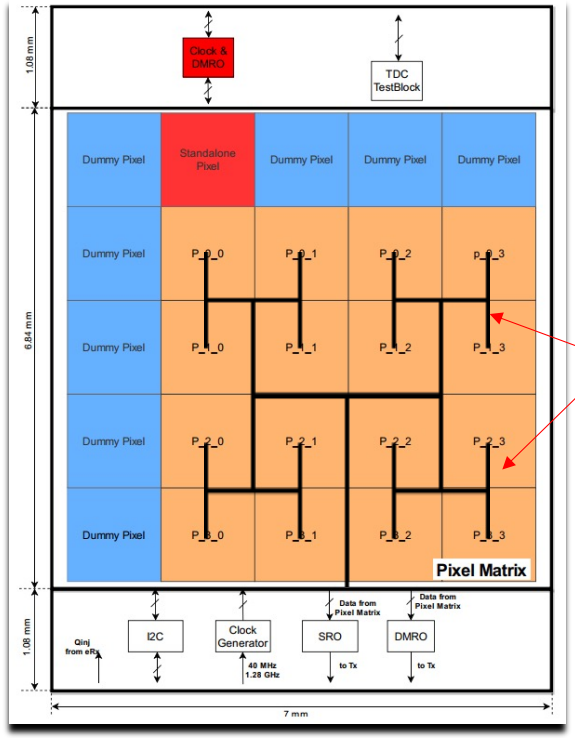
- *This has been the focus over the past few months*
- *As well as the ETROC1 beam test*

Bare ETROC1 works very well, matches with simulation



Bare ETROC0:
Charge injection → preamp → discriminator → scope





ETROC1
4x4 clock
H-tree

40MHz
320MHz

Jitter measurements with bare ETROC1: Full chain with Charge injection → preamp→ discriminator→ TDC

Comparing to ETROC0:

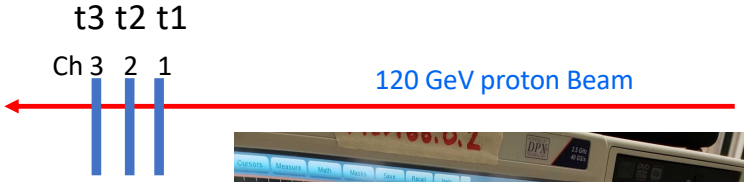
A simple ETROC0 Beam Telescope (with 3 HPK-ETROC0 boards)

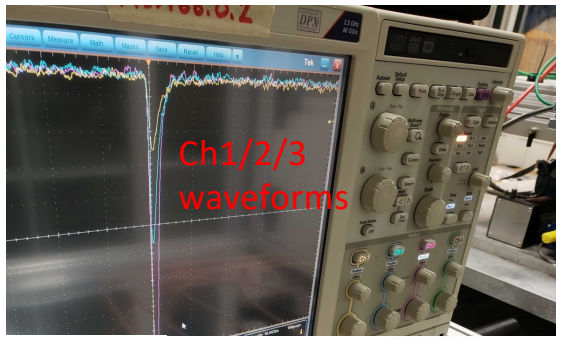
Jan-Feb 2020

Simple "suitcase" setup in parasitic mode running at FNAL MTest

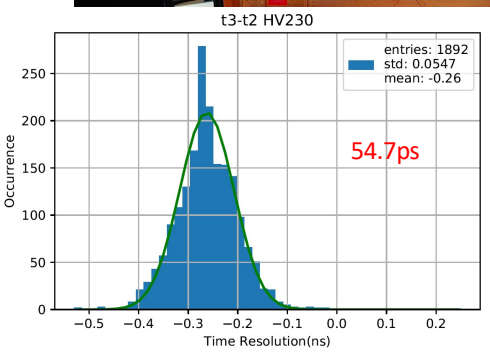
April – May 2020 parasitic run cancelled due to COVID-19

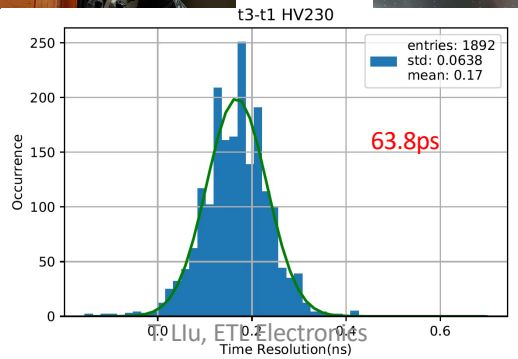
$$\sigma_2 = \sqrt{0.5 \cdot (\sigma_{21}^2 + \sigma_{32}^2 - \sigma_{31}^2)} \approx 33\ (ps)$$

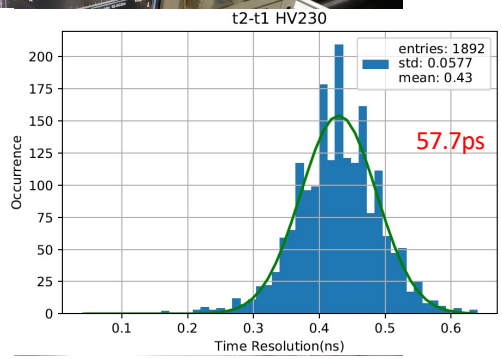




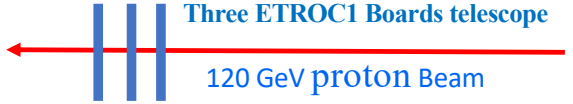
preamp waveform analysis

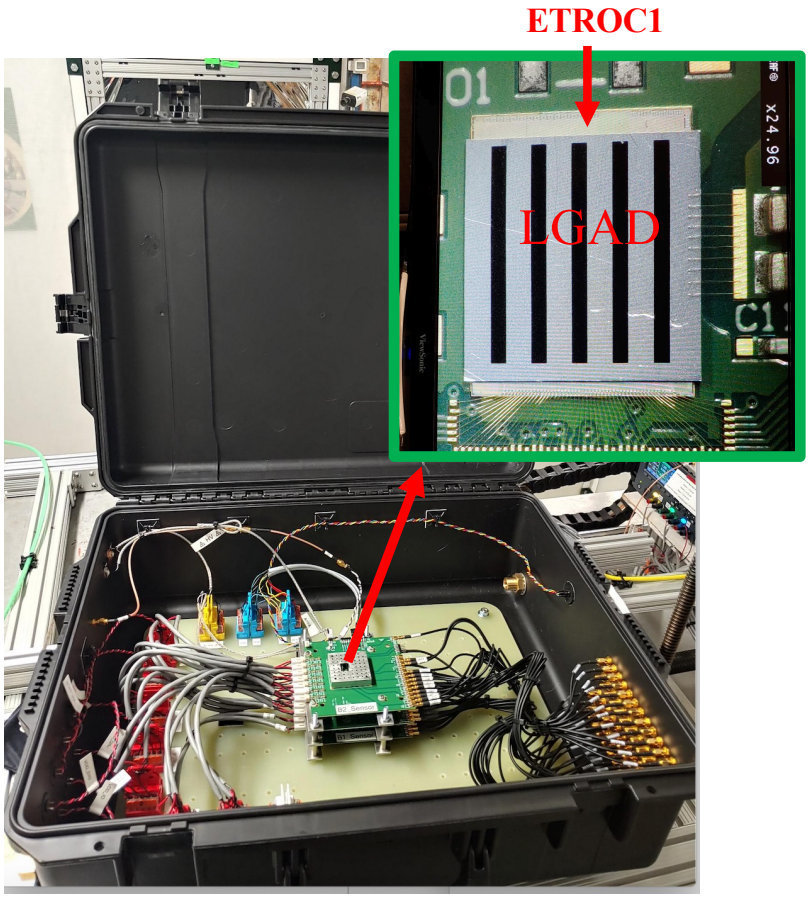




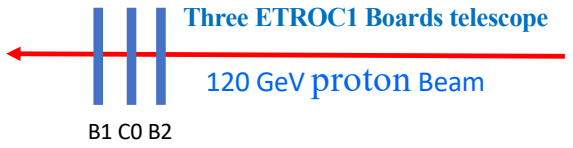


ETROC1 Beam Telescope @ FTBF



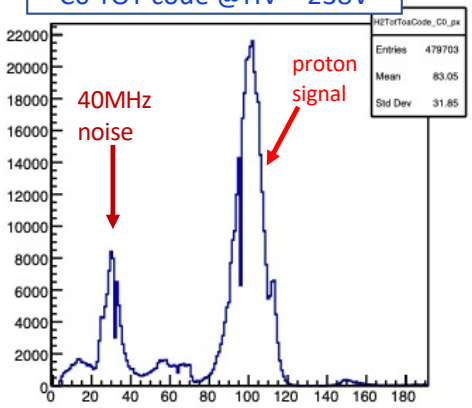


ETROC1 Beam Telescope @ FTBF

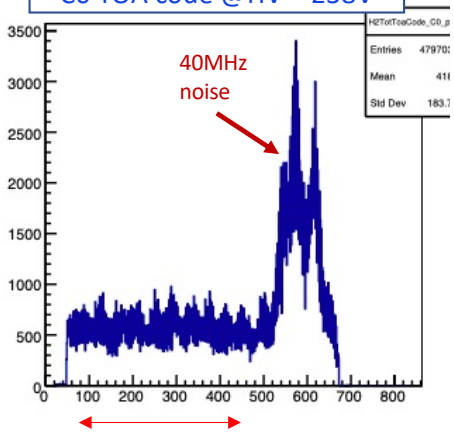


Telescope DAQ:
Triggered on B1
offline confirmed with B2
C0 is Device Under Test

C0 TOT code @HV = 238V



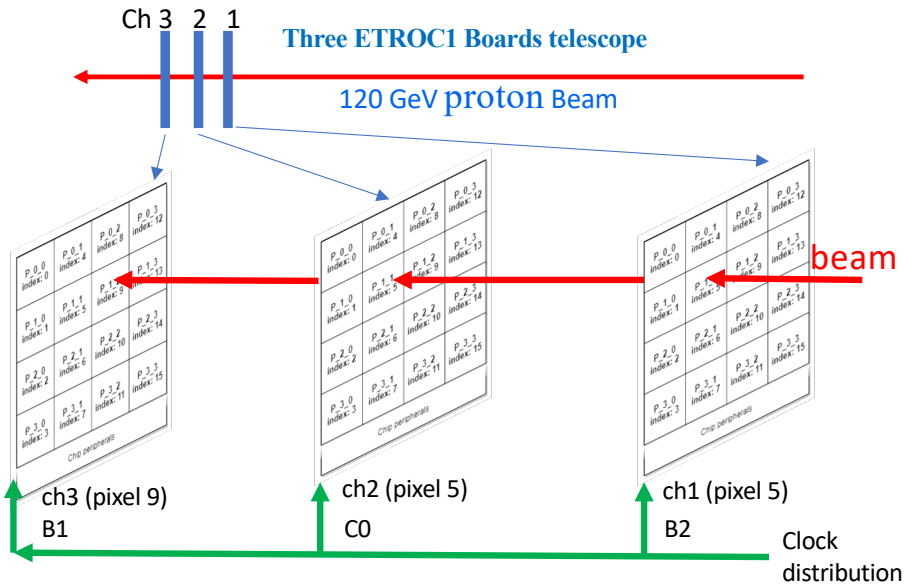
C0 TOA code @HV = 238V



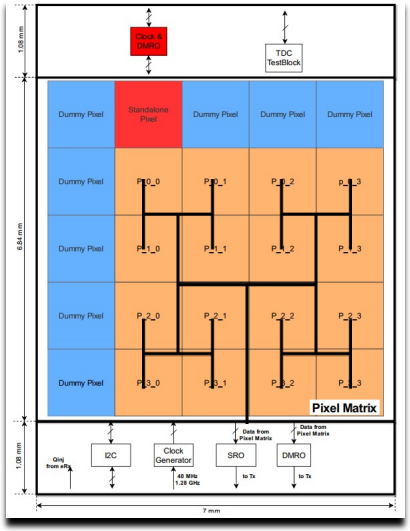
Tevatron machine clock 53MHz
ETROC clock 40MHz

Beam TOA (time of arrival) is flat,
and 40MHz noise is not.
Can stay away from the noise this way

LGAD+ETROC1 – Preliminary Test Beam Results (data from April 2021)



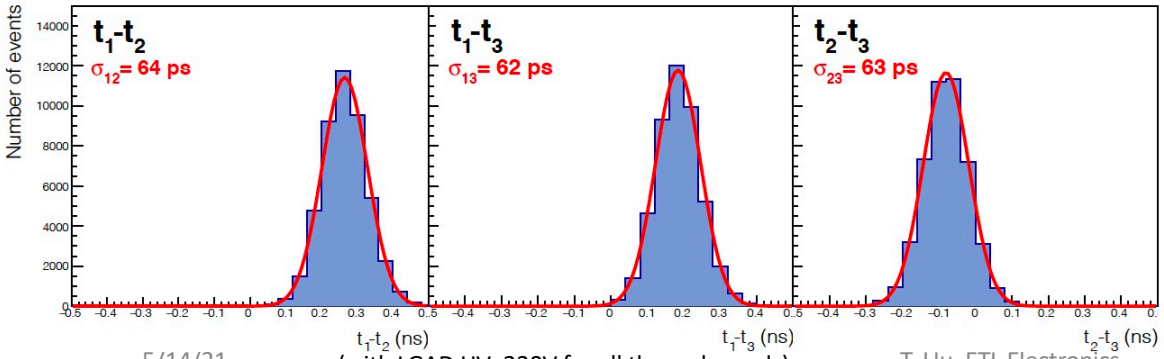
ETROC1 4x4 H-tree clock distribution within chip



ETL Time resolution

Simulation vs spec (unit: ps)

LGAD+ preamp/discriminator + TDC bin	35	
Time-walk correction residual	< 10	
Internal clock distribution	< 10	
System clock distribution	< 15	
Per hit total time resolution	41	50 ps
Per track (2 hits) total time resolution	29	35 ps



(with LGAD HV=230V for all three channels)

From preliminary analysis of the data from ongoing beam test at FNAL, the total time resolution per hit for each LGAD+ETROC1 layer has reached:

$$\sigma_i = \sqrt{0.5 \cdot \left(\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2\right)} \sim 42 - 46 \text{ ps}$$

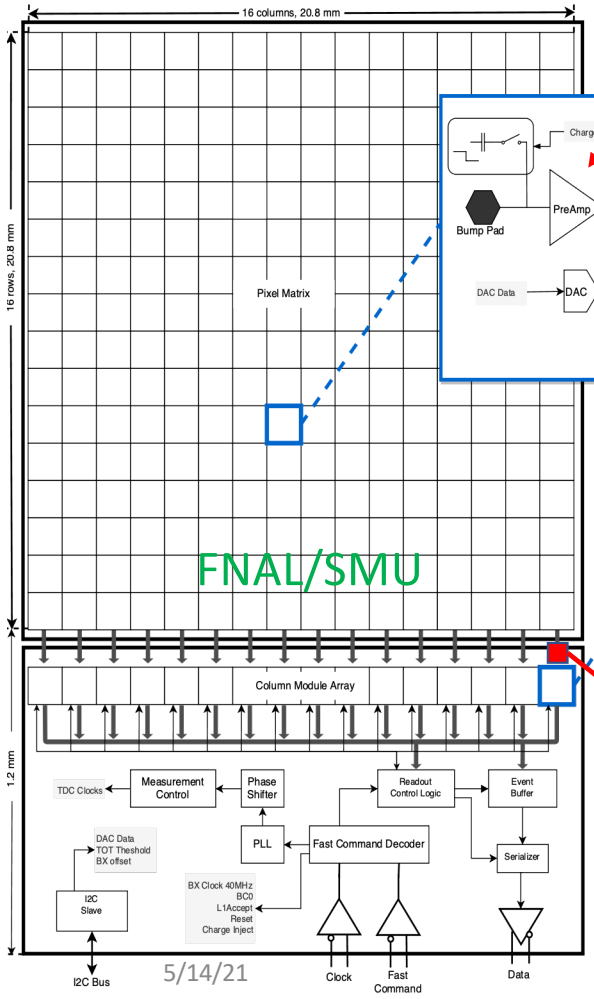
This measured time resolution includes all four contributions in the table

ETL ASIC (ETROC) status

- ETROC0
  - Charge injection/Cosmic/Laser done
  - TID test to 100Mrads done
  - Beam testing ~30ps achieved in beam (preamp waveform analysis)
- ETROC1 (good progress made despite COVID over the past year)
  - New TDC extensively tested: excellent performance (<~6ps resolution)
  - Bare ETROC1 charge injection testing: matches well with simulation at all levels
  - ETROC1 and 5x5 LGAD sensor bump-bonded
    - ***Encountered some noise related to 40MHz clock activity after bump bonding with sensor***
      - ***Being studied. For now, threshold set at 8fC to avoid the noise for beam test***
        - ***Final system needs ~4fC threshold***
    - ***Recent beam testing: preliminary results from April beam data***
      - ***Observed 42 - 46 ps per hit at system level in beam (Specification ~50 ps per hit).***
  - *ETROC1 TID testing (to be done at CERN, delayed due to COVID)*
- ETROC2 (on going)
  - ETROC PLL mini-ASIC (based on lpGBT)***: test results very good, including SEU test***
  - Waveform sampler mini-ASIC: works well
  - ***ETROC readout: design optimization in progress***
  - ETROC emulator: *V0 is ready, and V1 testing on going, firmware advanced*
    - ***The main digital blocks being prototyped in the emulator***
      - ***Fast command decoding, DAQ readout, system interfaces***
  - Knowledge gained from ETROC1 testing has been highly valuable to ETROC2 design

ETROC

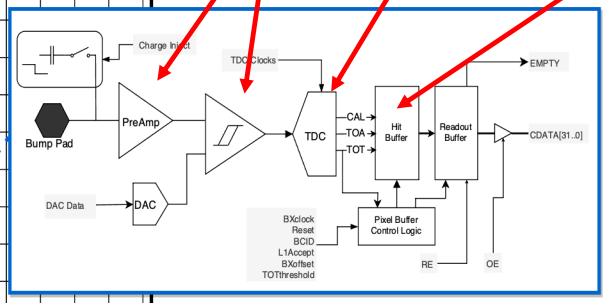
16x16 pixel cell array (1.3mm x 1.3 mm)



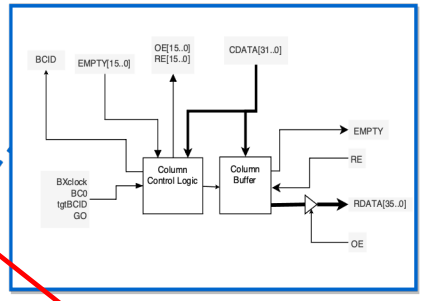
Preamp/Disc

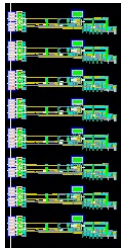
low power TDC

Hit buffer



FNAL/SMU





300um x 800um

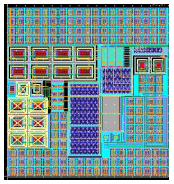
3.2GS/s waveform sampler

Ted Liu, ETROC

5/14/21

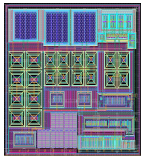
65nm implementation

90 um X 94 um



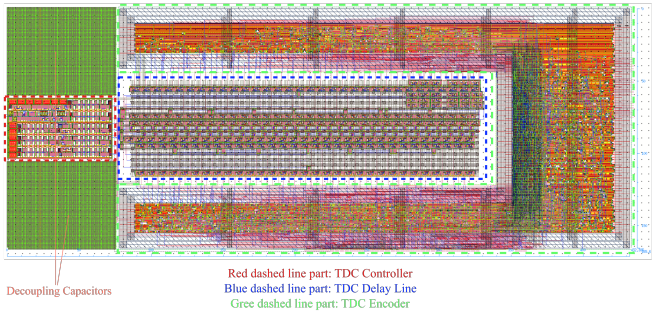
Preamp

81 um X 67 um



Discriminator

467 um X 166 um

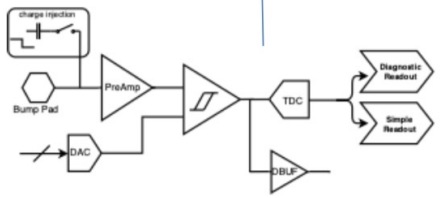


TDC

SRAM hit buffer
250 um x 150 um

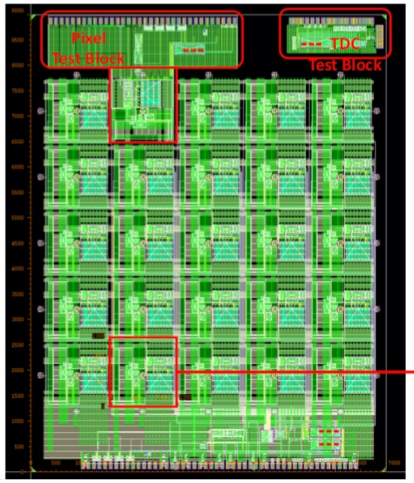
Hit circular buffer

ETROC0



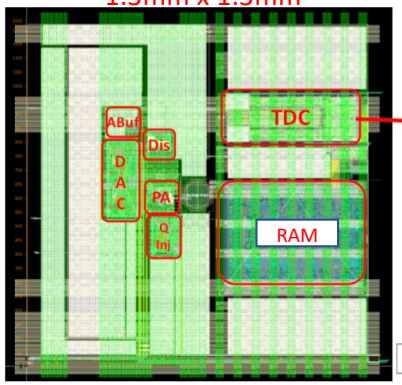
Low power TDC: <0.1mW

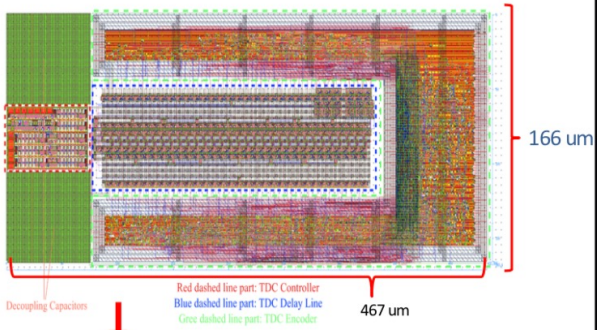
ETROC1 Top Layout

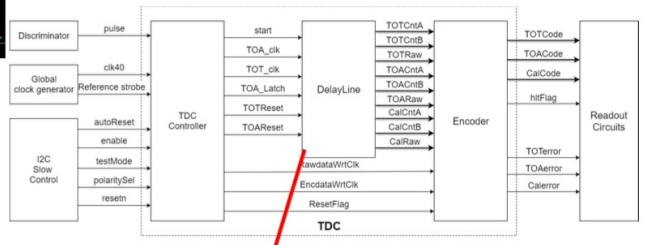


ETROC1 Single Pixel Layout

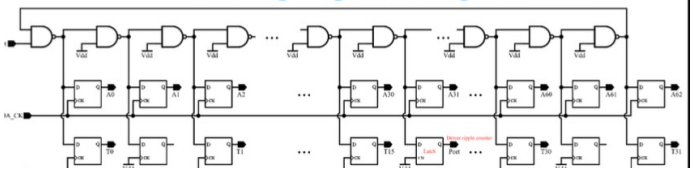
1.3mm x 1.3mm







TDC core logic: gated ring oscillator



ETROC1 TDC Design

- TDC requirements
  - TOA bin size < ~30ps, TOT bin size < ~100ps
  - Lower power highly desirable
    - ***ETROC TDC design goal: < 0.2mW per pixel***
- ETROC TDC design optimized for low power
  - A simple delay line without the need for DLL's to control individual delay cells, with a cyclic structure to reduce the number of delay cells, to measure TOA & TOT at the same time
- ***In-situ delay cell self-calibration technique***
  - For each hit, will use two consecutive rising clock edges to record two time stamps, with a time difference of the known 320 MHz clock period: 3.125ns
  - Crucial to reach the required precision using a tapped delay line with uncontrolled delay cells (thus lower power)