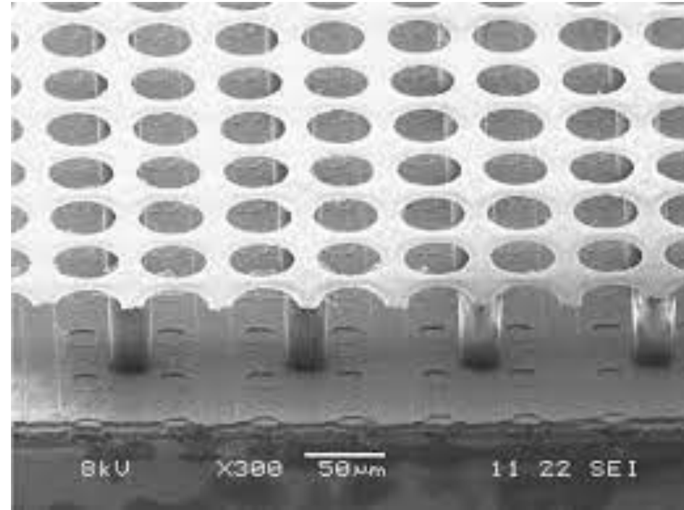


Low momentum PID at High B-field

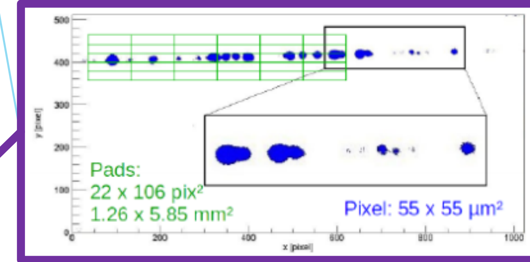
(“Mostly Silicon” Tracker with a PID layer)

TK Hemmick, K Dehmelt, (SBU)
N Smirnov, (Yale)
J Kaminski (Bonn)
S Park (SBU)
P Garg (SBU)

- GridPix is a 55 µm × 55 µm pixel readout for a gaseous TPC
- First Timepix3 based GridPix test beam (2017)
- Quad module performance from test beam (2018)
- Investigations of the 8 quad detector (2020)

Low Momentum PID

- High magnetic field curls low(er) momentum particles.
  - Option #1: We don't care about them. (bad option)
  - Option #2: Lower the B-field for "special runs". (poor option)
  - Option #3: PID on these particles BEFORE they curl up.



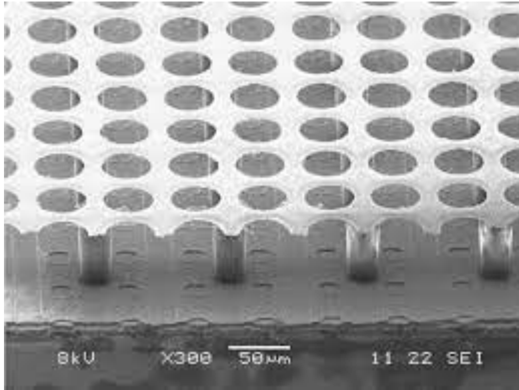
membrane

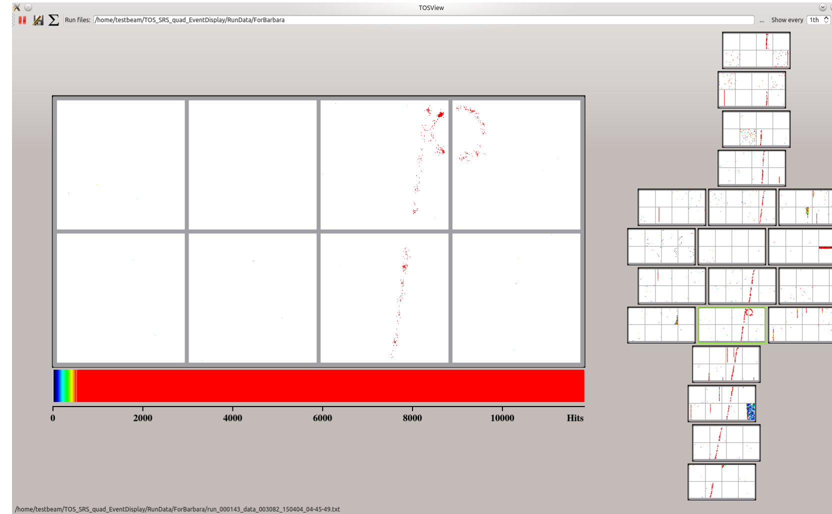
dE/dx Device

GridPIX

Mostly ~~All~~-Si Tracker

GridPIX Overview





- Ultimate dE/dx device.
  - Avalanche grid in front of 55 x 55 μm^2 pixels.
  - >90% efficiency for single electrons (Polya NOT exponential).
  - Goal:
    - Enough diffusion to get every electron into a different hole.
    - Count electrons one-by-one.
  - Three generations of development and continuing.
- Large area is VERY expensive, but this proposal is small area.
  - Careful: ~3kW of power must be removed.

3D e-by-e tracking

Observed standard deviation	41 µm
Statistical errors	25 µm
Systematic errors in the pixel plane and drift direction	19 µm
Multiple scattering	22 µm
Unidentified systematic error	14 µm

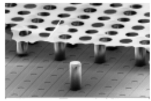
Pros:

- Known/Proven Technology
- Active further development (Bonn)
- Best $\frac{dE}{dx}$ possible (~count each electron)
- Affordable for a small area
- High resolution tracking
  - Also loves outer MPGDs!
- Low mass in electron arm
- Continuous (aka streaming) readout

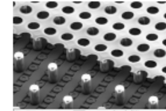
Cons:

- 3 kW of power.
- Must find a low pass way to handle.
- Services "bulky" (compared to just Si)
  - Gas
  - HV membrane
  - Cooling
  - DC power lines (3kV goes in too)

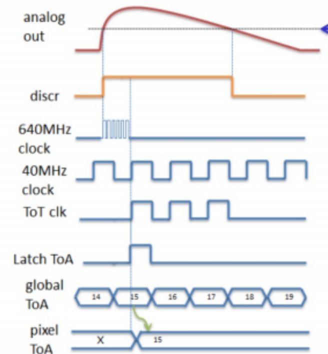
A Little Geometry

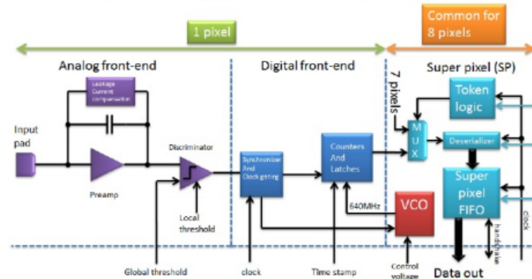


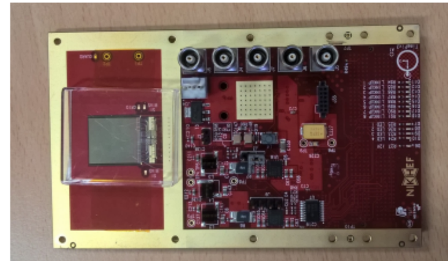
Timepix3



- Number of pixels: 256 × 256 pixels
- Pixel pitch: 55 × 55 µm²
- ENC: ~ 60 e⁻
- Charge (ToT) and time (ToA) available for each hit
- Timing resolution: 1.56 ns for duration of ~410 µs
- Zero suppression on chip (sparse readout)
- Multi-hit capable (pixels sensitive after t_{ToT}+475 ns)
  Super-pixels store hits for some time
- Output rate up to 5.12 Gbps
- Power pulsing possible (800 ns for start up)







J. Kaminski
MPGD2017

6

Timepix3 → Timepix4

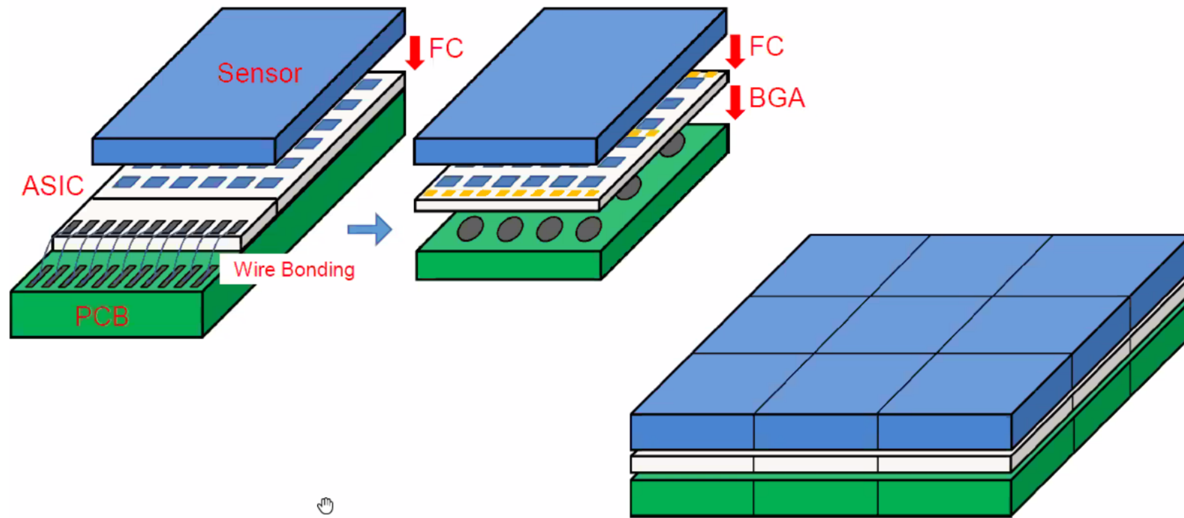
			Timepix3 (2013)	Timepix4 (2019)
Technology			130nm – 8 metal	65nm – 10 metal
Pixel Size			55 x 55 µm	55 x 55 µm
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448 **3.5x**
Sensitive area			1.98 cm²	**6.94 cm²**
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA	TOT and TOA
		Event Packet	48-bit	64-bit **33%**
		Max rate	0.43x10⁶ hits/mm²/s	**3.58x10⁶ hits/mm²/s** **8x**
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)
		Max count rate	~0.82 x 10⁹ hits/mm²/s	~5 x 10⁹ hits/mm²/s **5x**
TOT energy resolution			< 2KeV	< 1Kev **2x**
TOA binning resolution			1.56ns	**195ps** **8x**
TOA dynamic range			409.6 µs (14-bits @ 40MHz)	**1.6384 ms** (16-bits @ 40MHz) **4x**
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	**≤163.84 Gbps** (16x @10.24 Gbps) **32x**
Target global minimum threshold			<500 e⁻	<500 e⁻

- $55\ \mu m \times 256 = 1.4\ cm$ active area.
- 100cm/1.4cm = 71.4….call it 72 chips x 72 chips (but must eliminate holes)
- Rough number of actual chips: $\frac{\pi(50^2 - 25^2)}{1.4^2} = 3{,}005\ chips$ $\quad \frac{\pi(50^2 - 20^2)}{1.4^2} = 3{,}366\ chips$

https://indico.cern.ch/event/581417/contributions/2522462/attachments/1465797/2265982/GridPix_TP3.pdf

TimePIX4 is more Promising for EIC

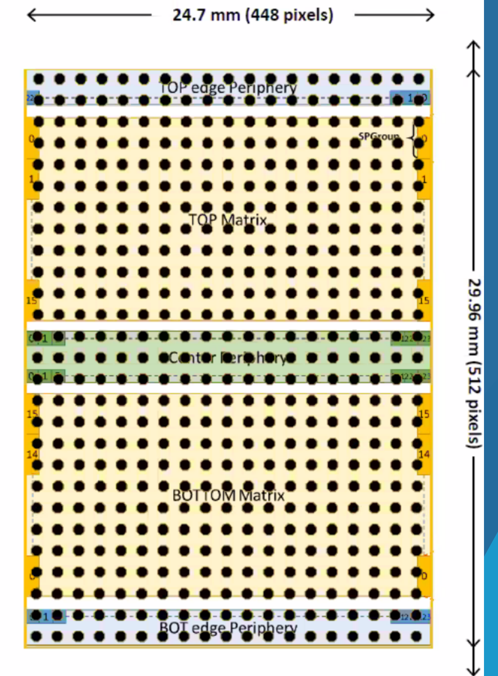
4-side buttable pixel arrangement



- Target to build **large area detectors** by combining smaller modules
- The through-silicon vias (TSVs) is the key technology for this paradigm shift

Timepix4 floorplan arrangement

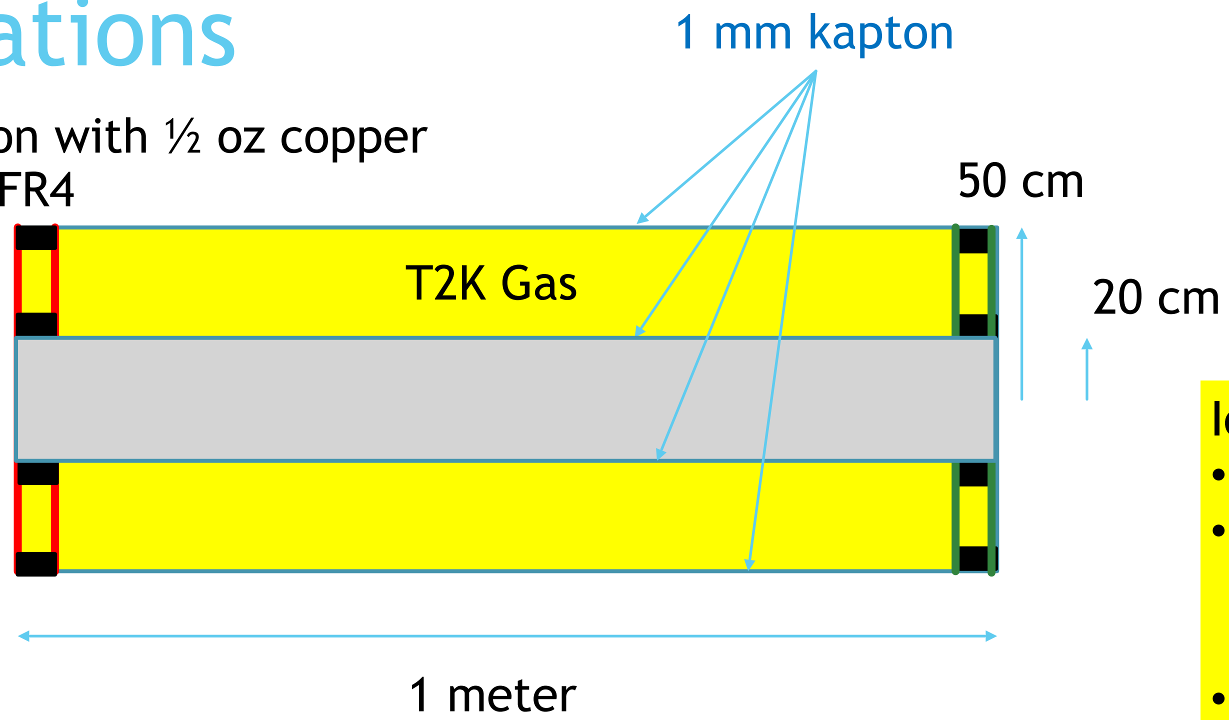
- 512 x 448 of 55 x 55 µm pixels
- 3 “hidden” peripheries with TSV (Through-Silicon-Vias):
  - TOP Edge: Data Readout & Slow Control
    - 147 TSVs/WBs: 106 POWER/GND and 41 IO
  - BOTTOM Edge: Data Readout & Slow Control:
    - 147 TSVs/WBs: 106 POWER/GND and 41 IO
  - CENTER: Slow Control and Analog Blocks (DACs, ADC, Band-Gaps…)
    - 147 TSVs: 124 POWER/GND and 23 IO
- On-chip bump to pixel redistribution layer (RDL)
- Chip size:
  - With WB (wirebonds extenders): 29.96 mm x 24.7 mm
    - **>93.7%** active area (28.16mm x 24.64mm)
  - Without WB (TSV Only) : 28.22 mm x 24.7 mm
    - **>99.5%** active area (28.16mm x 24.64mm)
- Control architecture allows to operated Timepix4 from any of the 3 peripheries:
  - i2C protocol
  - Custom Slow Control protocol
  - Interface to DAQ:
    - Through 3xTSVs
    - Through 2xWB
- Fast readout requires at least 1 serial link enabled in each edge periphery:
  - Serial links are highly configurable 40MBps → 10GBps



- Model 4 replaces wires bond with bump bond (improves active area).
- 93.7% → 99.5% active area.
- DAQ interface by Through-Silicon-Vias (TSV).

First Simulations

5 mil Kapton with ½ oz copper
0.063 inch FR4



2cm x 2cm C-fiber box with 2 mm walls (Hollow)

Ionization Stats:
- 95% Ar approx. as 100% Ar
- Avg: 23 primary/cm; 94 total/cm
  - Best case dE/dx ~4%
  - Worst case: dE/dx ~7%
- NOTE:
  - Life is easy at low p

- A starting Geometry.
- Primary ionization from Garfield
- GridPIX response from Jochen, Michael Lupberger (RD51)
- Geometry from Sanghwa
- Parallel Efforts
  - Standalone and GEANT – made correct