

DE LA RECHERCHE À L'INDUSTRIE



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Micromegas technology for ATHENA

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EIC YR – Tracking WG
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Requirements:

- Maximum total material budget: 5% of X_0
- Compatible with physics performances

Simulations:

- Beam pipe
- Si 3 vertex + 2 tracking layers
- MPGD layers: 6 (max)

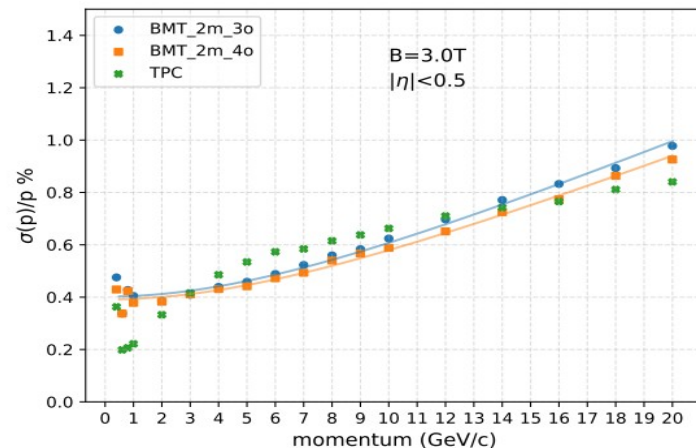
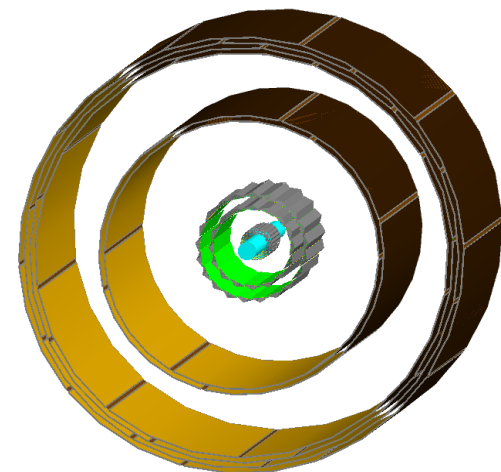
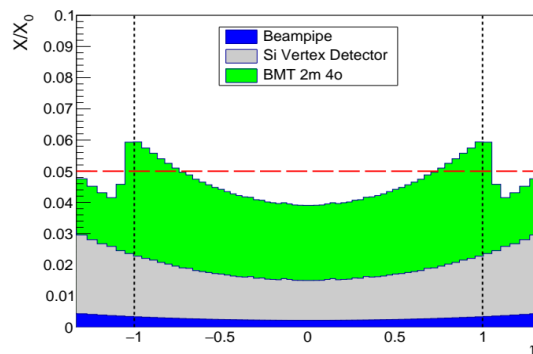
MPGD layers implementation:

- Detailed implementation based on CLAS12 Micromegas
- 2D readout, assuming $150\mu\text{m}$ resolutions
- Tiles $\sim 50\text{cm}$ wide
- $\sim 2\text{cm}$ gaps filled with PCB and Cu $25\mu\text{m}$

Material budget: $\sim 0.4\%$ of X_0

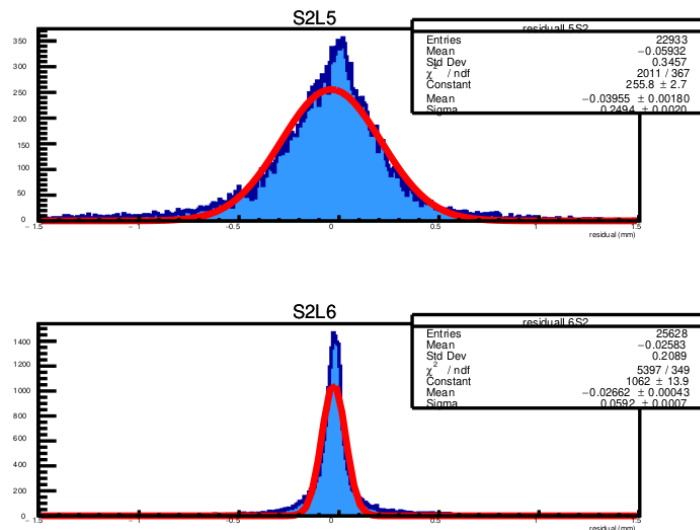
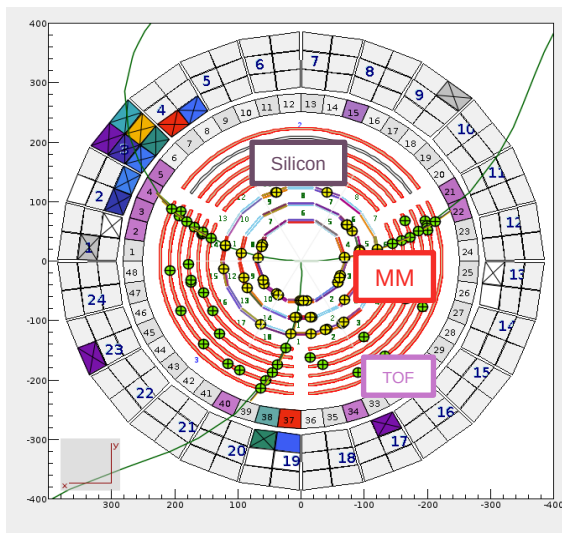
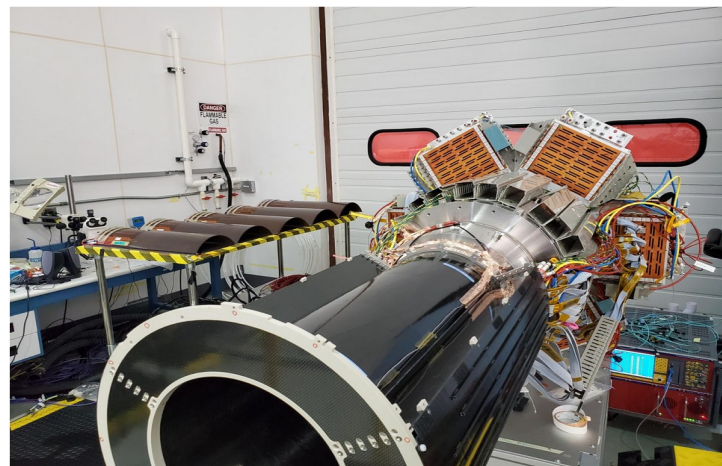
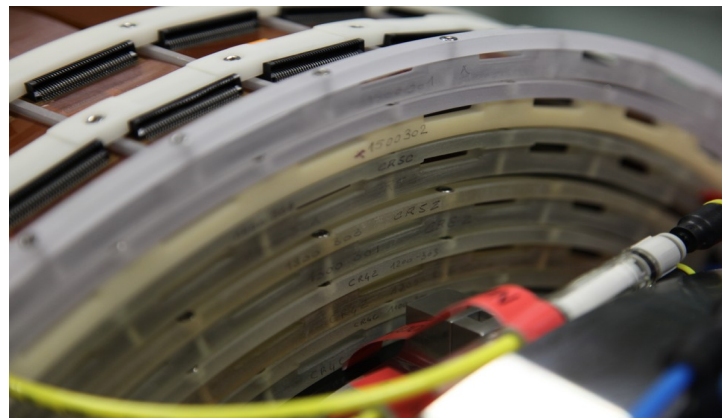
Results:

- At 3T, tracking performances within specs**
- Material budget within limits**



CLAS12 Micromegas Vertex Tracker

- 4 m² of curved Micromegas detectors
- DREAM based Front-End Electronics ~ 20k ch.
- Low momentum particles => Light Detectors ~0.4% of X0
- Limited space of ~10 cm for 6 layers (small radius ~12 cm)
- High magnetic field (5T)
- 6 Layers with different R (18 detectors total), 1D readout
- Up to 30 MHz of particle rate
- Taking data since 2017



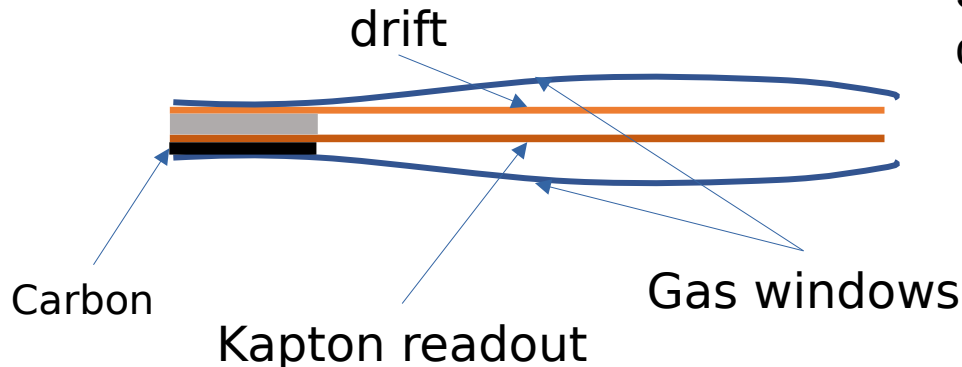
Residuals examples with preliminary alignment

- **Curved Micromegas**
- Consolidated technology
- CLAS12 MM are 1D readout
- $\sim 0.4\%$ of X_0 per tile
- 2D readout already used in other experiments
- Ongoing R&Ds to improve resolutions (See next slides)
- A 2D prototype Micromegas tile to be build in 2023

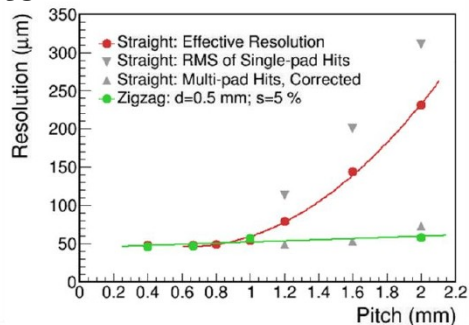
- **Flat ultra light Micromegas: “sail tracker”**
- Goals: optimization of overall material budget, simplification of production line
- Modular design
- Very low X/X_0 : aiming at $0.07\%X_0$ in the active area

Step by step R&D:

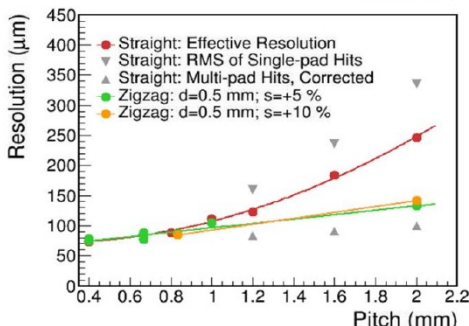
- PCB → Just a Kapton layer (2021)
- Inox mesh → LASER etched Al or Cu (2022)
- Cu strips → deposited Al (2023)
- Some of these R&Ds can be ported to the curved technology too



Zigzag 1D residual Pitch 2mm



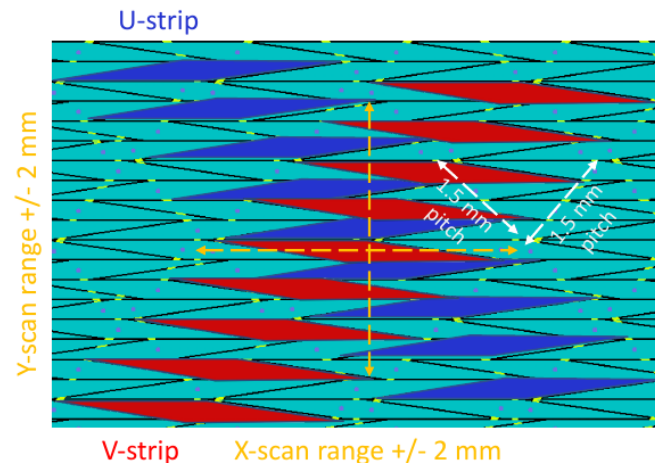
4-GEM : $<70\mu\text{m}$



Micromegas: $<150\mu\text{m}$

A Comparative Study of Straight-Strip and Zigzag-Interleaved Anode Patterns for MPGD Readouts

C.Perez-Lara & all, <https://arxiv.org/abs/2101.12134>



4-GEM

- Measure U- and V-coordinates **at once**
- Residuals from $\sigma \sim 55 \mu\text{m}$ to $\sigma \sim 85 \mu\text{m}$
- Remaining DNL below $\sim 50 \mu\text{m}$

Presented at TIPP 2021 by Alexander Kiselev

Resolution of the order of $150\mu\text{m}$ is expected for 2D with Micromegas with 2mm pitch

120 m² of clean room for Micromegas bulk and resistive layer manufacturing.

Bulk process: addition of a mesh on PCB by photolithography

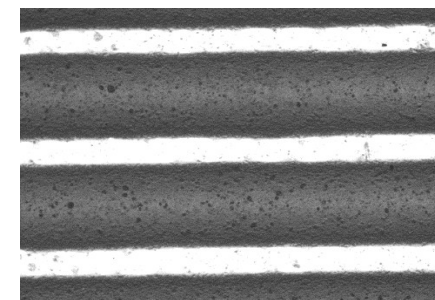
- Maximum detector size: 600 x 700 mm².
- Amplification gap from 50 to 292 μ m
- Mesh woven (18 μ m wires) or thin mesh (down to 5 μ m)
- PCB with strip, XY strip, pixel,...
- Production : ~ 150 bulk in 2019
- R&D : thins mesh, curved bulk, segmented mesh, double mesh....

Resistive screen printing on various surface

- Maximum size: 600 x 600 mm²
- Resistive value: from 10 KOhm/sq, to 10 Gohm/sq
- Possibility of neutral on conductive paste
- Substrate: Kapton, glass, FR4
- Production: ~ 100 resistive substrate in 2019
- R&D : mixture for ad hoc resistive value, segmented resistive,...



Double face micromegas



Resist strip of 500 μ m



Bulk lab



Resist lab

- An hybrid EIC detector with a Micromegas barrel tracker fulfills the Yellow Report requirements
- Ongoing R&Ds are aiming at 2D readout with about 150 μ m resolutions on both directions
- A parallel R&D effort aims at lowering the material budget even further
- Low material budget Micromegas not just for the barrel region
- CEA Saclay can provide engineers for design and production
- Ongoing discussions with the electronics department to develop a ASIC for MPGD readout