EIC Roman Pots / AC-LGAD

IJCLab Progress Report

BNL-IJCLab-OMEGA Meeting - June 2nd, 2021

Dominique Marchand

on behalf of IJCLab team:

Carlos Munõz Camacho, Emmanuel Rauly, Laurent Serin, Ana-Sofia Torrento, Philippe Vallerand

- **Progress report on activities related to:**
  - * **an AC-LGAD (strips) sensor , 17 channels wire-bonded by BNL to an ALTIROC1_V2 (PCB #30)**
  - * **a DC-LGAD (pixels) sensor, 2 channels wire-bonded to an ALTIROC1_V2 (PCB #19)**

B19 and B30 PCBs shipped to BNL: estimated delivery on Thursday June 3rd

- **Outlook**
  - * **suggestions for next the wire-bonding(s) of an AC-LGAD to an ALTIROC1_V2**
  - * **foreseen activities at IJCLab**

(ALTIROC1_V2 + AC-LGAD) typical observed output signals on scope: B30

VPA *AC-LGAD sensor unpolarized (No HV applied)*

ALTIROC1 inner pulse (DAC pulser 63), no additional capacitance

Discriminator output signal disabled)

ALTIROC1 grounded wires cut and HV cable cut

Switching 40 MHz and/or 320 MHz clocks has no effect

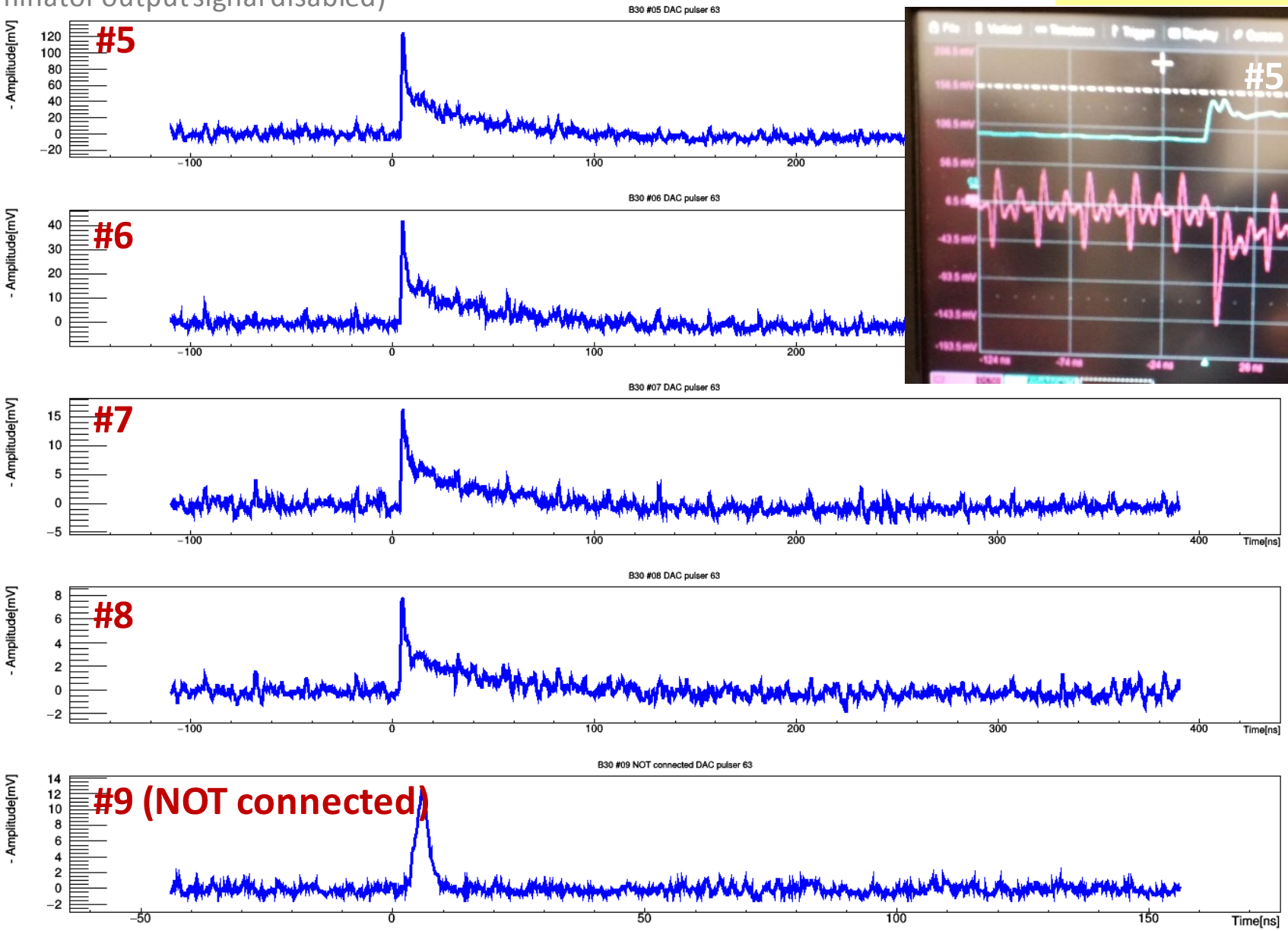
(ALTIROC1_V2 + AC-LGAD) typical observed output signals on scope: B30

VPA *AC-LGAD sensor unpolarized (No HV applied)*

ALTIROC1 inner pulse (DAC pulser 63), no additional capacitance

Discriminator output signal disabled)

ALTIROC1 grounded wires cut and HV cable cut



ALTIROC1 grounded wires and HV cable

Switching 40 MHz and/or 320 MHz clocks has no effect

(ALTIROC1_V2 + AC-LGAD) typical observed output signals on scope: B30

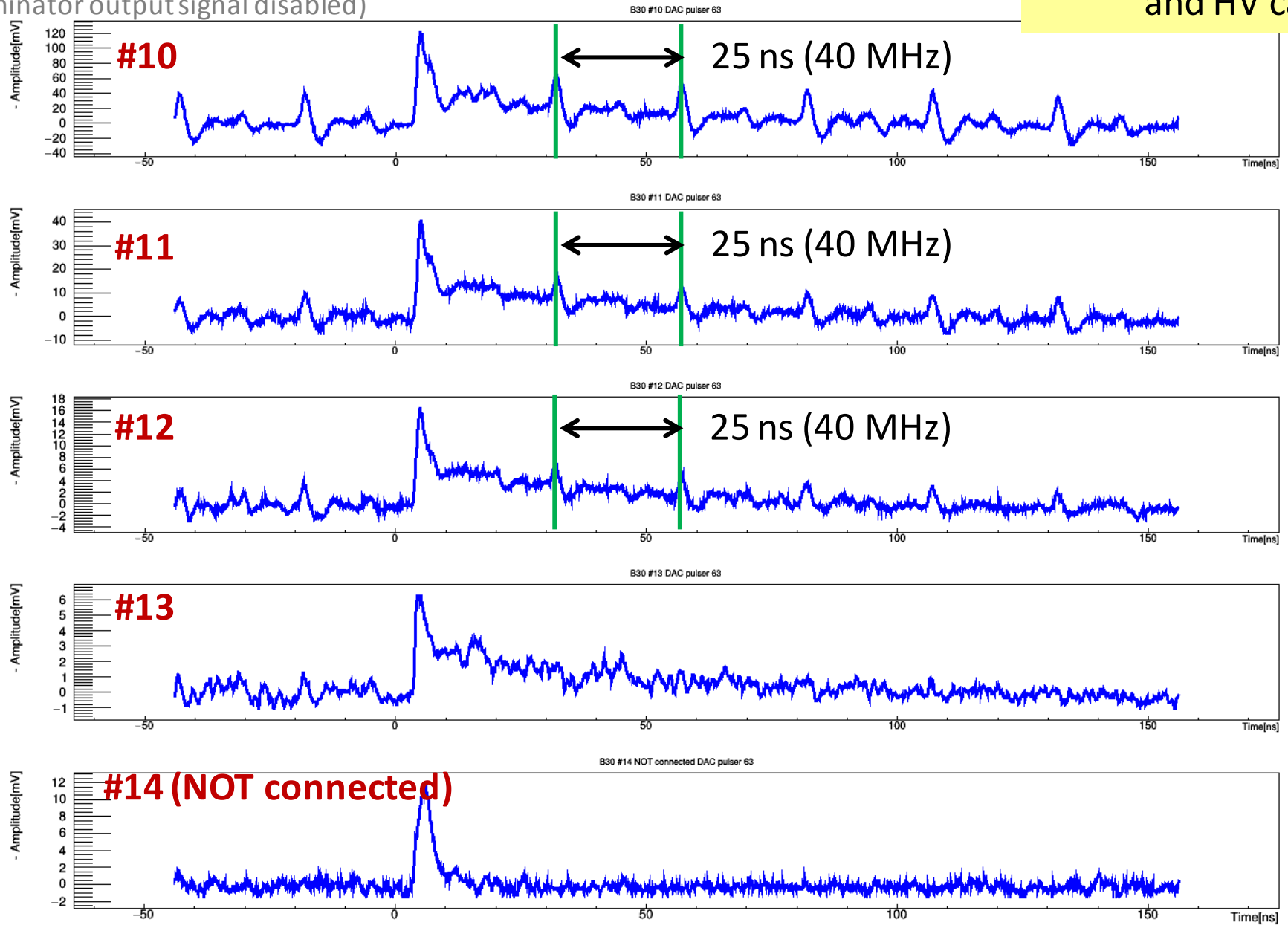
VPA

AC-LGAD sensor unpolarized (No HV applied)

ALTIROC1 inner pulse (DAC pulser 63), no additional capacitance

Discriminator output signal disabled)

ALTIROC1 grounded wires cut and HV cable cut



Switching 40 MHz and/or 320 MHz clocks has no effect

(ALTIROC1_V2 + AC-LGAD) typical observed output signals on scope: B30

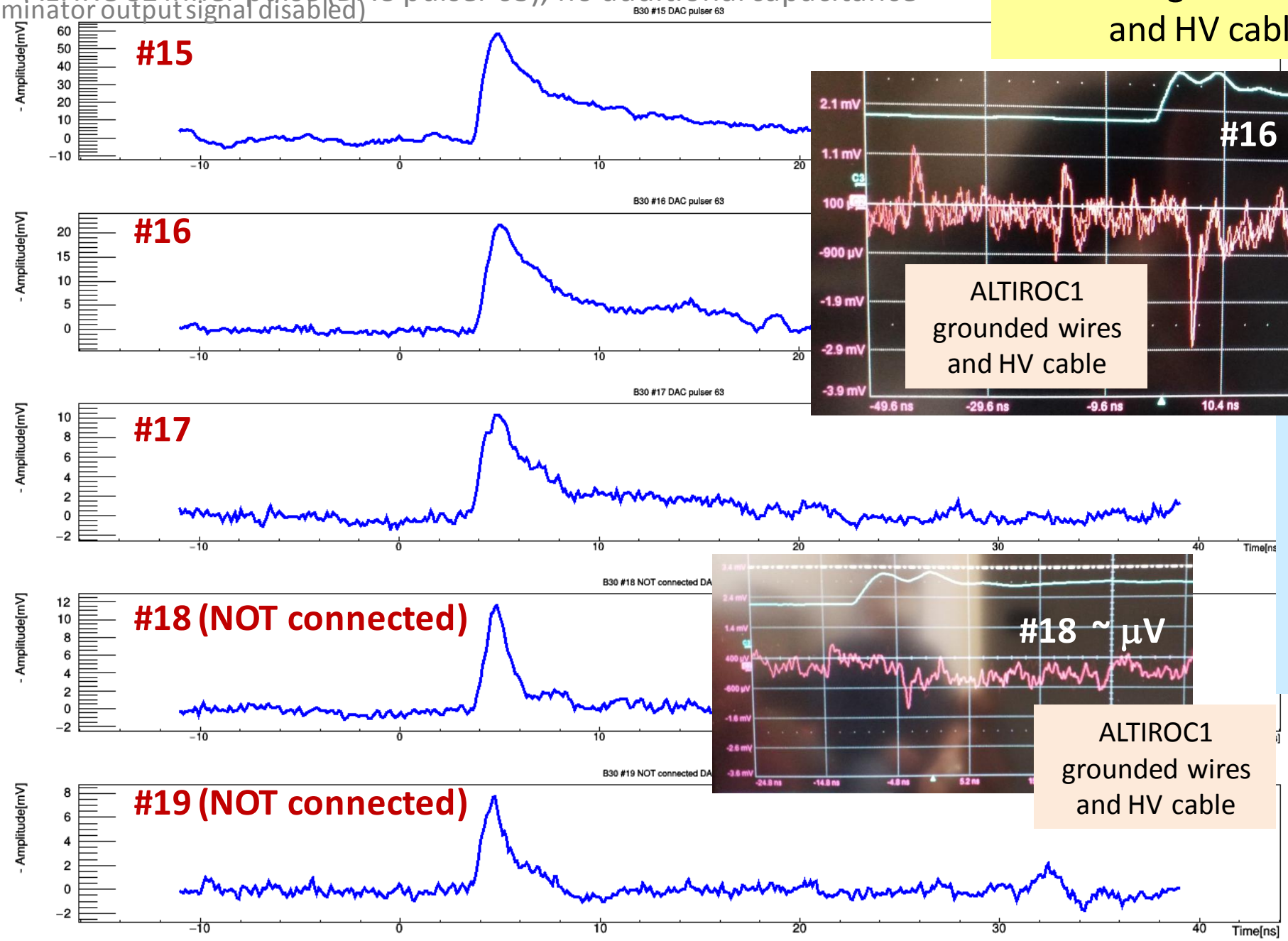
TZ

AC-LGAD sensor unpolarized (No HV applied)

ALTIROC1 inner pulse (DAC pulser 63), no additional capacitance

Discriminator output signal disabled)

ALTIROC1 grounded wires cut and HV cable cut



Switching 40 MHz and/or 320 MHz clocks has no effect

(ALTIROC1_V2 + AC-LGAD) typical observed output signals on scope: B30

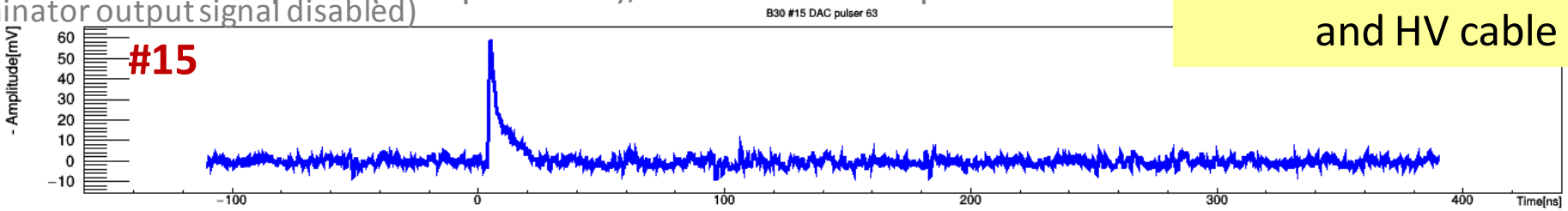
TZ

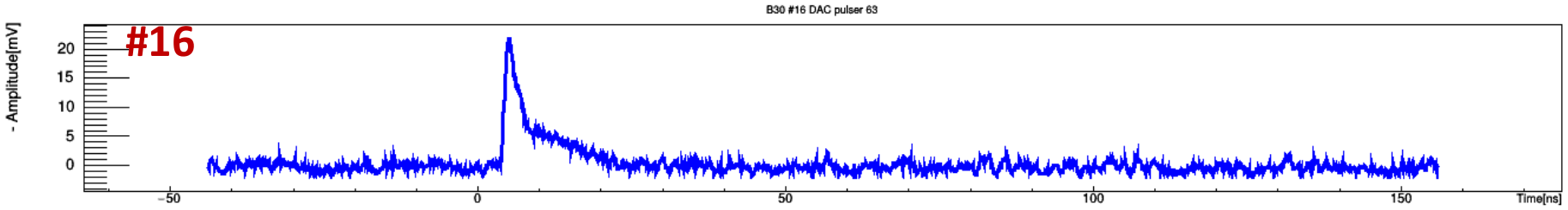
AC-LGAD sensor unpolarized (No HV applied)

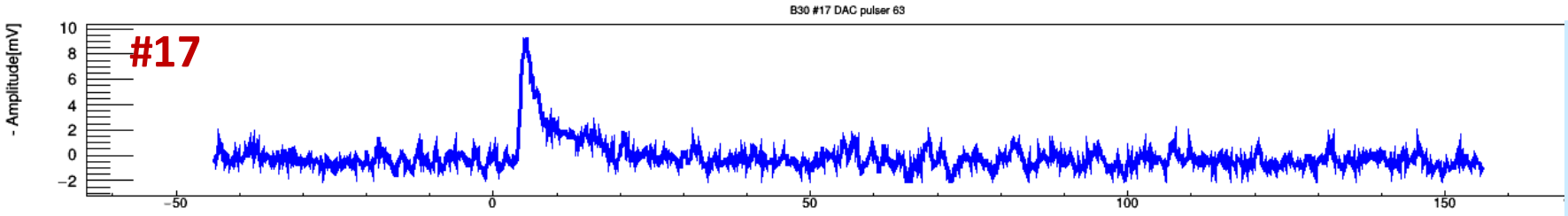
ALTIROC1 inner pulse (DAC pulser 63), no additional capacitance

Discriminator output signal disabled)

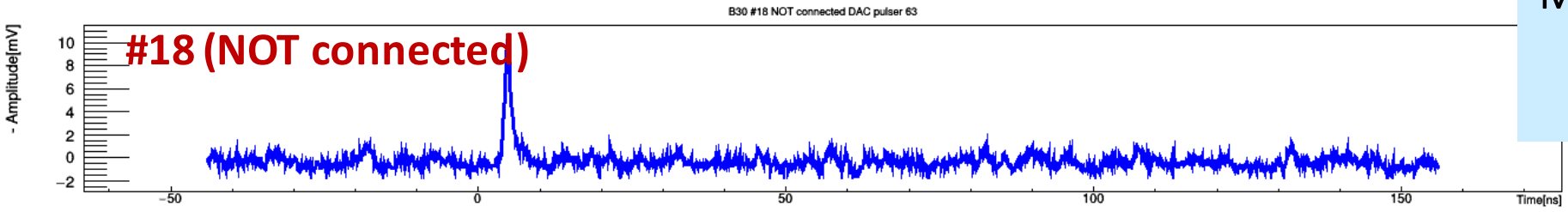
ALTIROC1 grounded wires cut and HV cable cut

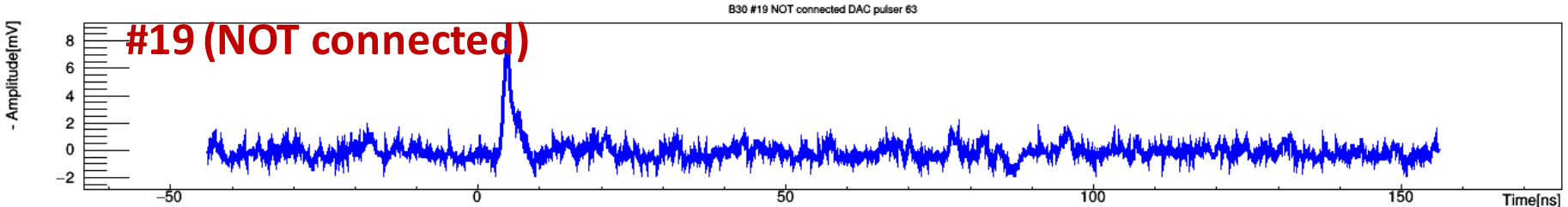






Switching 40 MHz and/or 320 MHz clocks has no effect





(ALTIROC1_V2 + AC-LGAD) observed output signals on scope: B30 SUMMARY

*AC-LGAD sensor unpolarized (No HV applied): **no way to deplete the sensor***

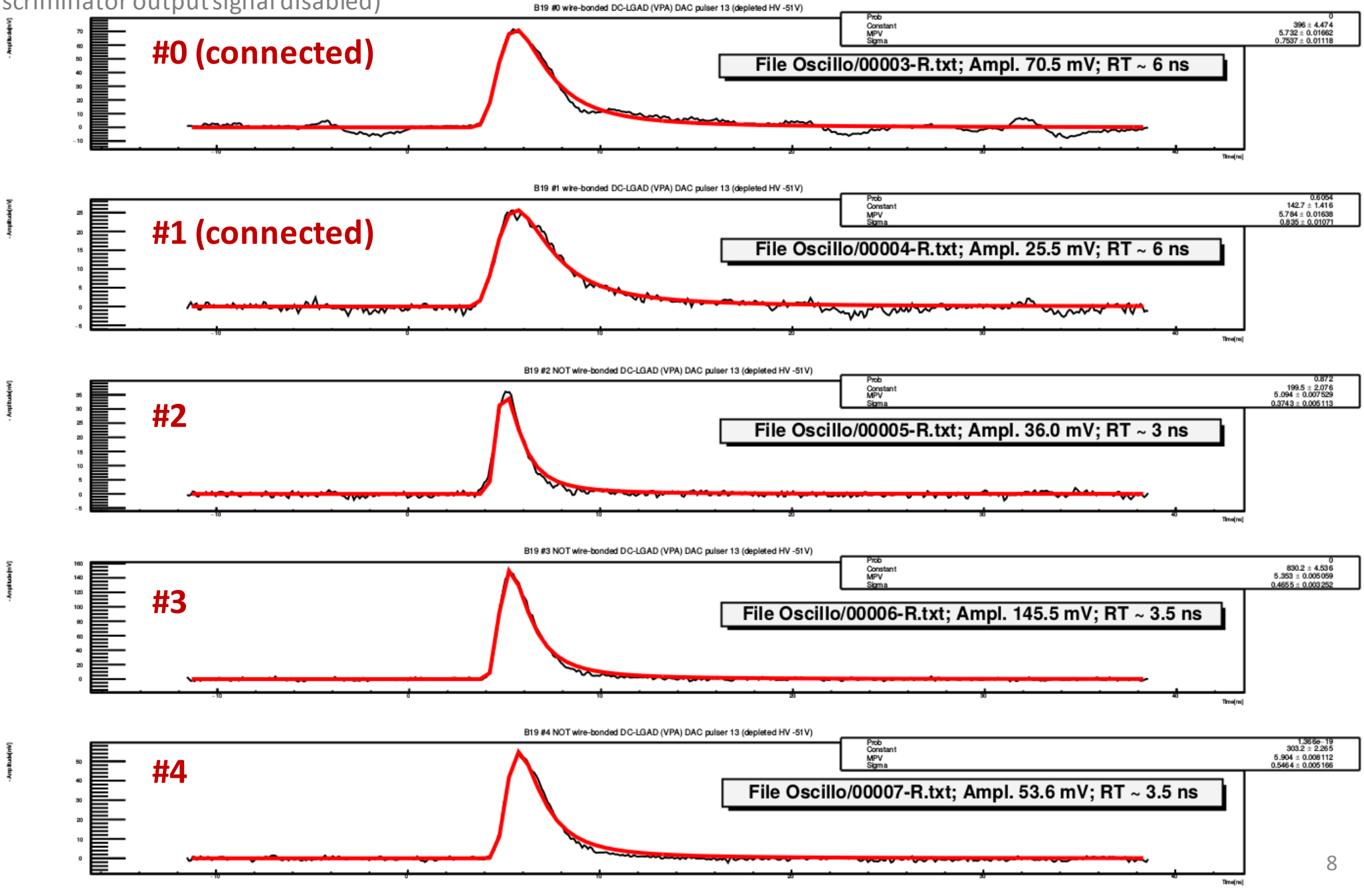
ALTIROC1 inner pulse (DAC pulser 63), no additional capacitance

- Disconnecting wires from ALTIROC1 to ground for non wire-bonded channels had an impact on output signal amplitudes: « proportional » to inner pulser
- Disconnecting HV cable reduced coupling: much cleaner signals
- Switching 40 MHz and/or 320 MHz clocks on PCB has no effect (slightly more noisy)

VPA

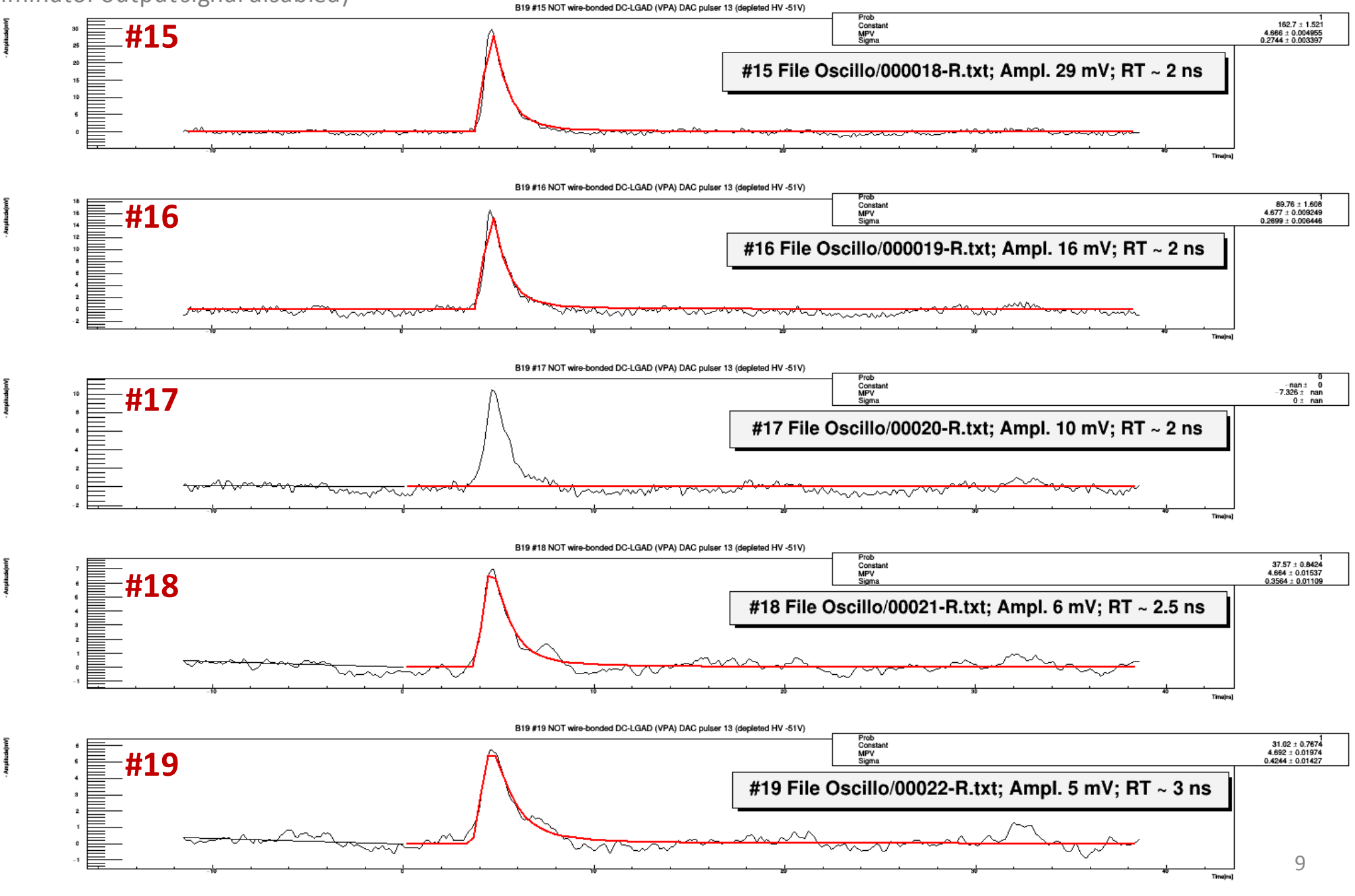
B19 (wire-bonded ALTIRC1 to DC-LGAD (depleted -51V): channels #0 -> # 4

ALTIROC1 inner pulse (DAC pulser 63), no additional capacitance
Discriminator output signal disabled)



B19 (wire-bonded ALTIRC1 to DC-LGAD (depleted -51V) : channels #15 -> # 19 (not connected)

ALTIROC1 inner pulse (DAC pulser 63), no additional capacitance
Discriminator output signal disabled)



TDC measurements on B19 and B30 PCBs

➢ 2 TDCs in ALTIROC1: 1 for TOA, 1 for TOT

➢ 3 Delay-Locked Loop to adjust soldering discrete resistance on PCB for TOA (LSB ~20ps) and for TOT (slope ~160 ps)

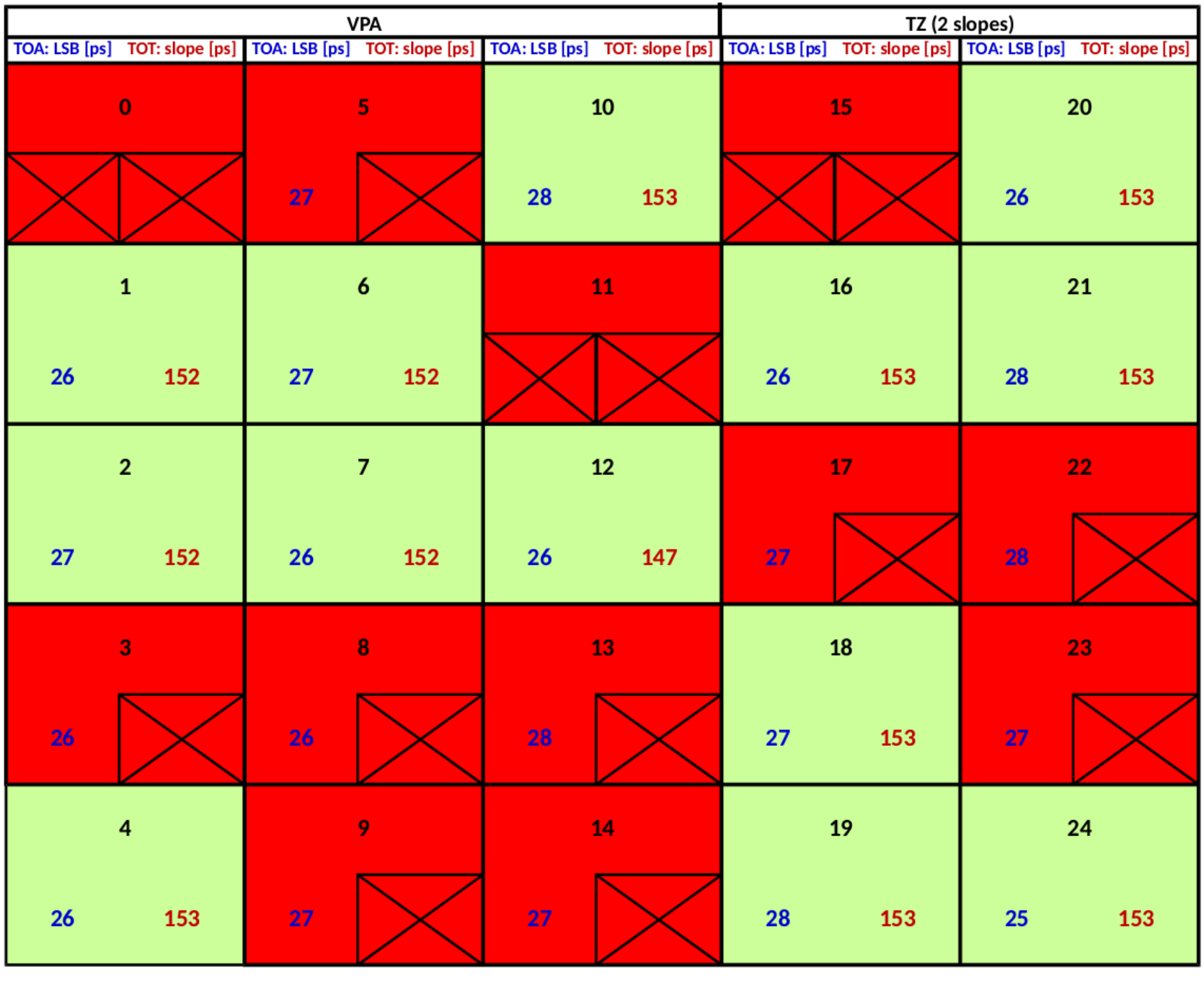
- B19: adjustment performed May 12th (Nathalie and Laurent)
- B30: DLL NOT adjusted (a jumper added)

➢ Requires to set a switch (#18) on interface board (has to be blue) to generate sliding delays within a 2.5 ns window (TOA) and to vary the width (TOT)

➔ **GOAL:** to identify « good » / «working » ALTIROC TDC channels to suggest for next AC-LGAD wire-bonding to ALTIROC1_V2.

B19

TOA and TOT measurements; DLL adjusted



13 ALTIROC1 TDC channels **OK**

B30

TOA and TOT measurements; DLL NOT adjusted (jumper added)

VPA				TZ (2 slopes)	
TOA: LSB [ps]	TOT: slope [ps]	TOA: LSB [ps]	TOT: slope [ps]	TOA: LSB [ps]	TOT: slope [ps]	TOA: LSB [ps]	TOT: slope [ps]
0		5		10		15		20	
14	160	14		13	160			15	
1		6		11		16		21	
14	158	15		14	163	14		13	161
2		7		12		17		22	
14	162	14		14	160	14		15	162
3		8		13		18		23	
16		15		14		18	169	15	162
4		9		14		19		24	
15	160	15		16		15		14	161

10 + 2 ALTIROC1 TDC channels **OK**

(ALTIROC1_V2 + AC-LGAD) wire-bonding concerns (1/2): suggestion of TDC channels

PCB #19: 13 functional TDC channels

VPA channels :
- #1, #2, #4,
- #6, #7
- #10, #12

} **7**

TZ channels :
- #16, #18, #19,
- #20, #21, #24

} **6**

PCB #30: 10 (+2) functional TDC channels

VPA channels :
- #0, #1, #2, #4,
- #10, #11, #12

} **7**

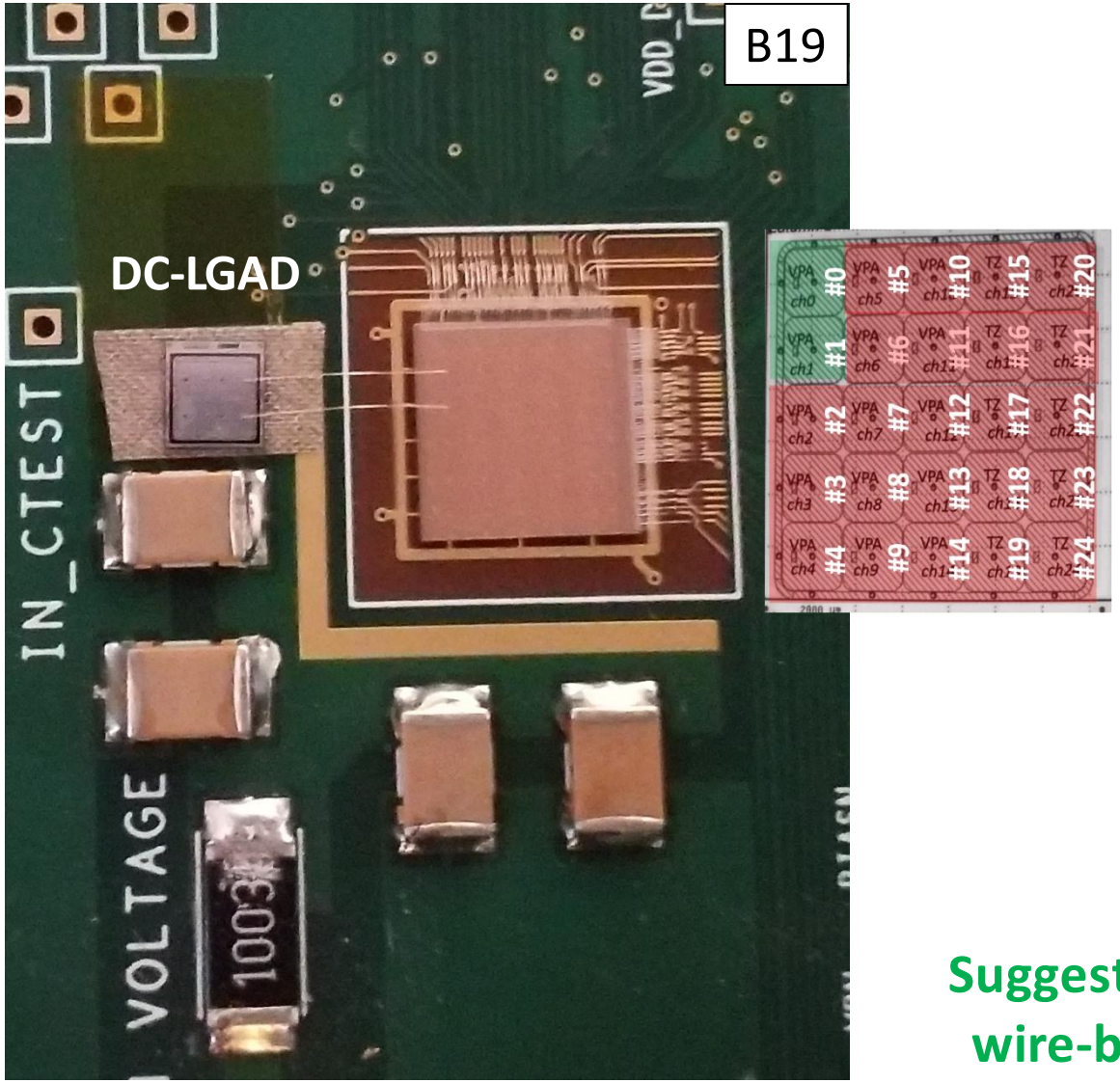
TZ channels :
- (#18),
- #21, #22, (#23), #24

} **3 +(2) = 5**

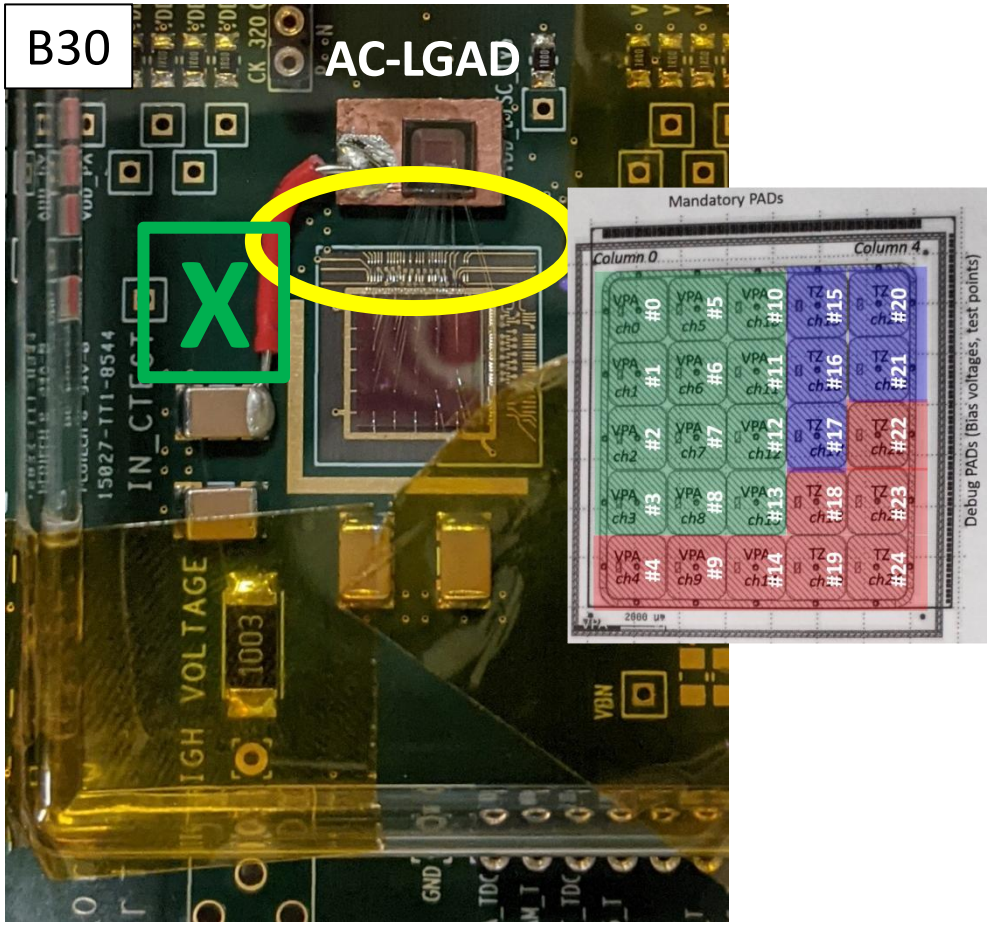
We suggest that at least **3 VPA** AND **3 TZ** channels to be wire-bonded

(ALTIROC1_V2 + AC-LGAD) wire-bonding concerns (2/2): sensor implantation

PCB **#19**:
a **DC-LGAD** wire-bonded to an ALTIROC1_V2ALTIROC1_V2 (channels 0 & 1)



PCB **#30**:
an **AC-LGAD** wire-bonded to an ALTIROC1_V2ALTIROC1_V2 (17 channels)



Suggestion: displaced the location of the wire-bonding / AC-LGAD to avoid clock paths and use the copper plate for HV

Summary of suggestions for next AC-LGAD wire-bonding

- To use both, B30 and B19 PCB, if possible
- NOT to connect ALTIROC1 non wire-bonded channels to ground
- Displace the location of AC-LGAD sensor on PCB to avoid clock paths
- To avoid to add an additional HV cable candidate for selfic noise
- To choose ALTIROC1 TDC functional channels
- To measure on a probe station I(V) curve prior to shipping to IJClab

Questions

- AC-LGAD (4 x 4 pixels) availability at BNL?
- When the next wire-bonded could be ready to be shipped to IJCLab?

Outlook

- To make measurements at ILJCLab on previously tested PCBs holding an ALTIROC1_V2 to check our setup.

- To make a simulation of resulting peak position resolution to evaluate the necessary number of bits (10 // 8) for ADC option based on Maxime's simulation of signal amplitude sharing in neighboring pads (3 x 3).

- A PCB with an ALTIROC1_V**3B** might be available after the summer.