sPHENIX INTT - Weekly Report

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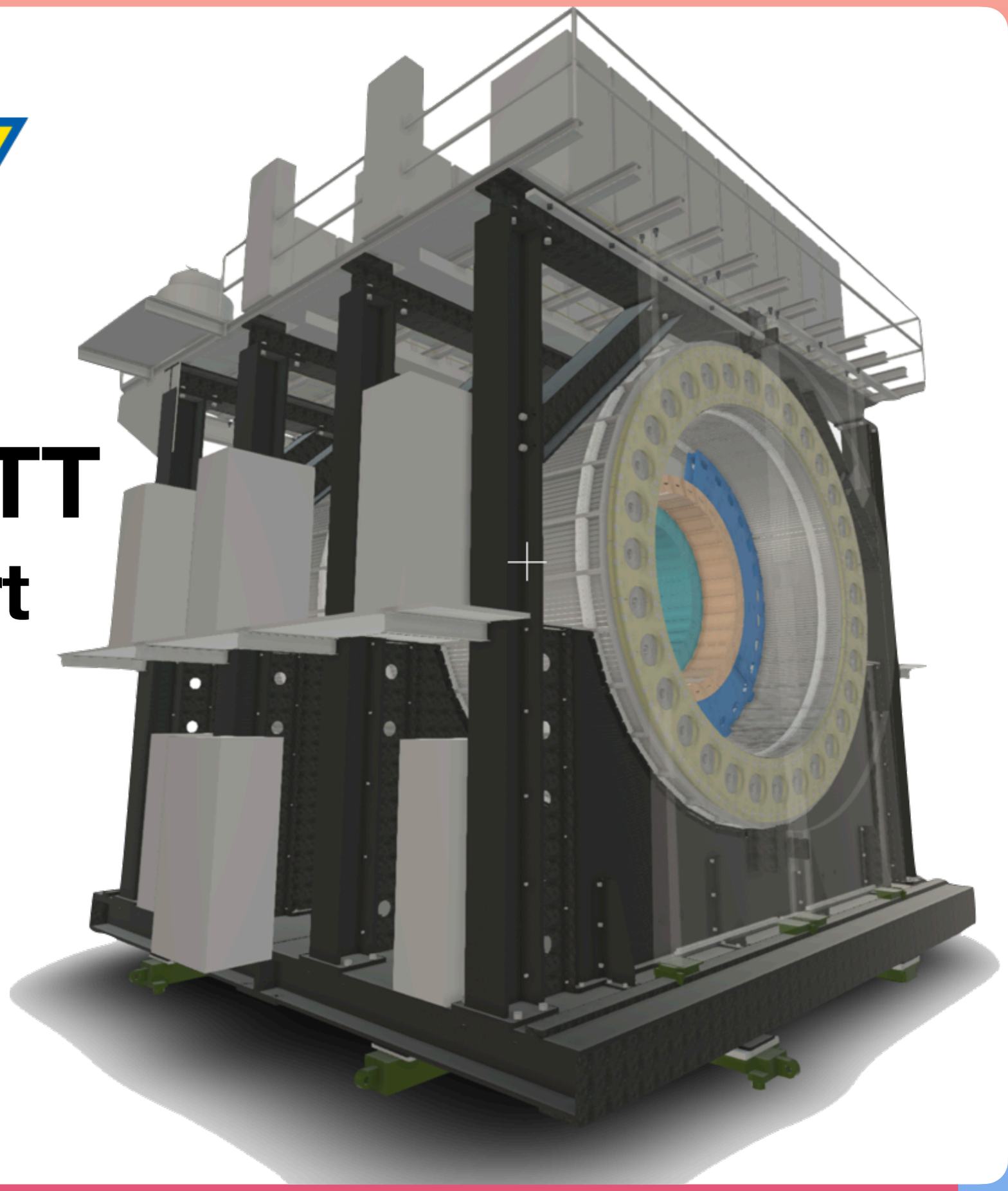
NCUHEP

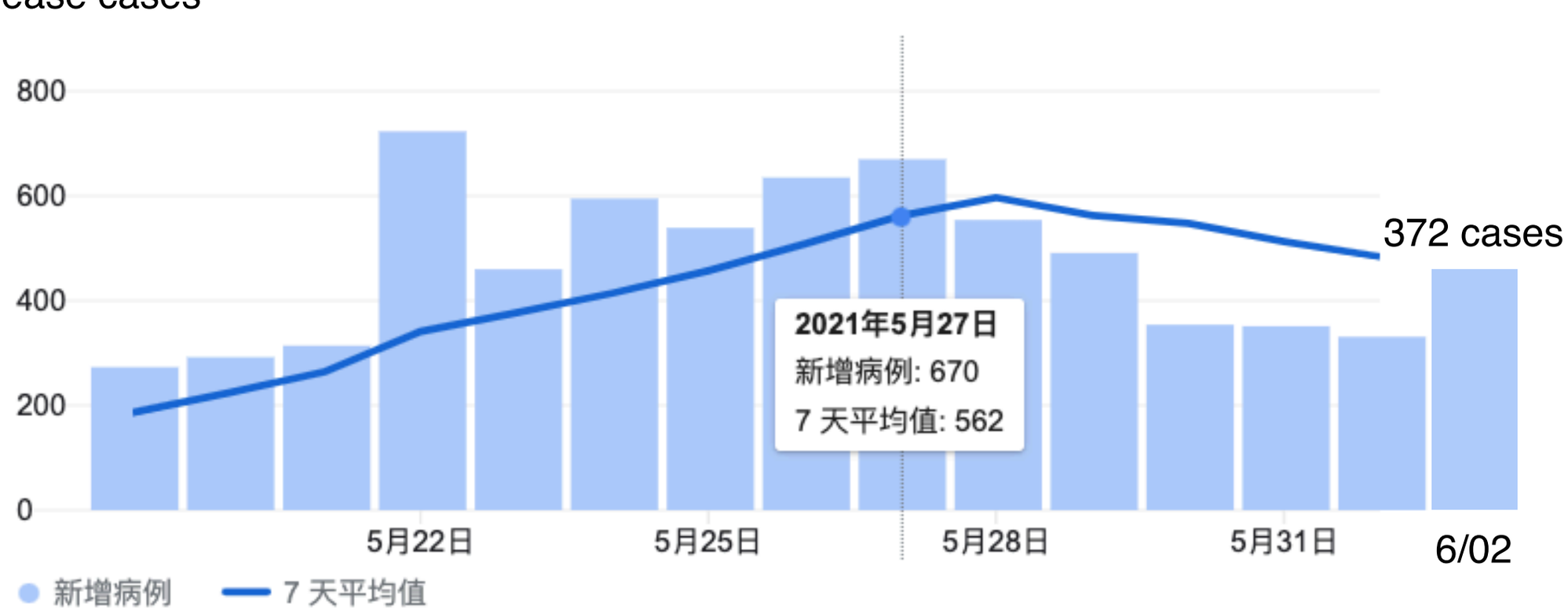
2021/6/3



COVID-19 status in Taiwan

- ~ 400 new COVID-19 cases each day.
  - Most of the cases are from Taipei (NTU) and new Taipei City.
- National level 3 epidemic warning until 6/14 (so far)
  - We still stop to go to NTU
  - We will try to apply DP460 in NCU.

Increase cases



Channel classification update

- The macro of channel classification is finished, the codes and instructions are in the Link.

- The time information is included :

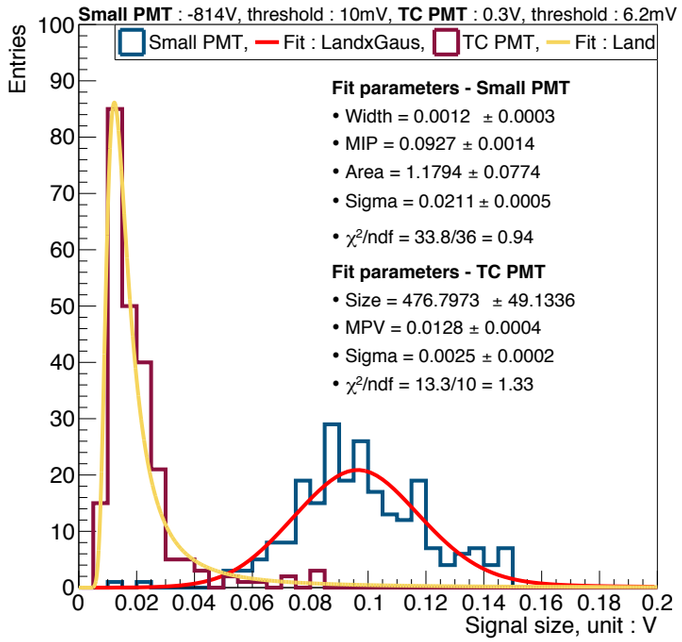
```
Noise channel found, chip : 2   channel : 0     failed times : 13/20    ratio : 0.65
Noise channel found, chip : 7   channel : 12    failed times : 20/20    ratio : 1
Noise channel found, chip : 19  channel : 36    failed times : 20/20    ratio : 1
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
Noise channel, chip : 2 channel : 0
 failed in file index : 2       file name : fphx_raw_20210428-1320_0, gaus width : 46.9425
 failed in file index : 3       file name : fphx_raw_20210428-1321_0, gaus width : 78.376
 failed in file index : 4       file name : fphx_raw_20210428-1322_0, gaus width : 4.47558
 failed in file index : 5       file name : fphx_raw_20210428-1324_0, gaus width : 4.59855
 failed in file index : 6       file name : fphx_raw_20210428-1331_0, gaus width : 75.7756
 failed in file index : 7       file name : fphx_raw_20210428-1332_0, gaus width : 32.8639
 failed in file index : 8       file name : fphx_raw_20210428-1333_0, gaus width : 38.3274
 failed in file index : 11      file name : fphx_raw_20210428-1654_0, gaus width : 147.086
 failed in file index : 12      file name : fphx_raw_20210428-1656_0, gaus width : 127.588
 failed in file index : 14      file name : fphx_raw_20210428-1659_0, gaus width : 4.8683
 failed in file index : 15      file name : fphx_raw_20210428-1700_0, gaus width : 4.15262
 failed in file index : 17      file name : fphx_raw_20210428-1703_0, gaus width : 4.41939
 failed in file index : 19      file name : fphx_raw_20210428-1706_0, gaus width : 33.9221
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~

!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
Weird entries found, chip : 2   channel : 0     failed times : 12/20    ratio : 0.6
Weird entries found, chip : 19  channel : 113   failed times : 20/20    ratio : 1
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
Bad entries channel, chip : 2 channel : 0
 bad in file index : 2  file name : fphx_raw_20210428-1320_0, entries : 4410
 bad in file index : 3  file name : fphx_raw_20210428-1321_0, entries : 5820
 bad in file index : 5  file name : fphx_raw_20210428-1324_0, entries : 645
 bad in file index : 6  file name : fphx_raw_20210428-1331_0, entries : 7557
 bad in file index : 7  file name : fphx_raw_20210428-1332_0, entries : 2104
 bad in file index : 8  file name : fphx_raw_20210428-1333_0, entries : 4062
 bad in file index : 11 file name : fphx_raw_20210428-1654_0, entries : 20615
 bad in file index : 12 file name : fphx_raw_20210428-1656_0, entries : 17784
 bad in file index : 14 file name : fphx_raw_20210428-1659_0, entries : 569
 bad in file index : 15 file name : fphx_raw_20210428-1700_0, entries : 422
 bad in file index : 17 file name : fphx_raw_20210428-1703_0, entries : 467
 bad in file index : 19 file name : fphx_raw_20210428-1706_0, entries : 2125
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
```

INTT PMT

- Cosmic test is performed for supply voltage, threshold cut
  - NWU Supply voltage : -1100V
  - Test voltage : -800 V & -1100V

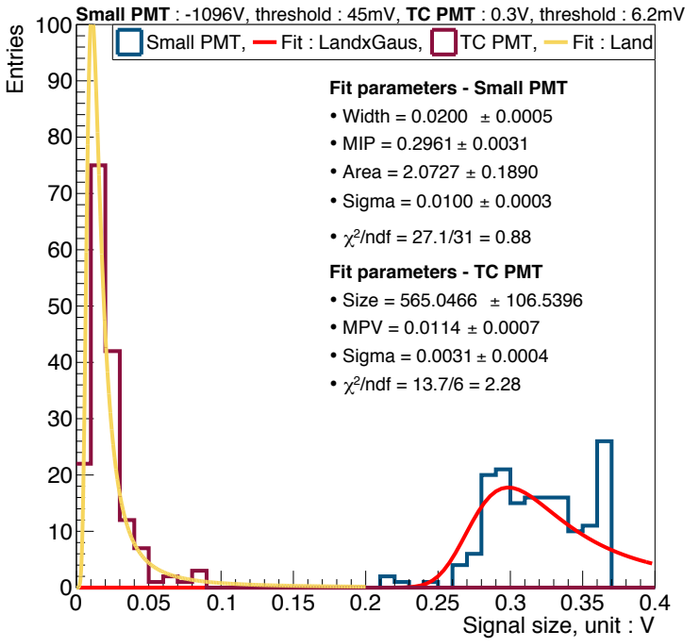
Voltage -800V, threshold : 10 mV
Event rate : 0.0038

Signal size



Voltage -1100V, threshold : 45mV
Event rate : 0.0024

Signal size



Working in progress
To do : test with different supply voltage

ROC FPGA firmware

- We discussed with engineer yesterday, we have some questions.

- We get the error when compiling the code
  - IDE version : Microsemi Libero v11.9

```
Error: PDC-71: Clock net name 'CLK' is not valid
Error: PDC-71: Clock net name 'CLK90' is not valid
Error: Failure when executing Tcl script. [ Line 25 ]
```

Successful compiling if comment these 2 lines out

Reports | StartPage | ROC_top.sdc | roc_top.pdc

```
1  assign_global_clock -net GLOBAL_RST
2  #assign_global_clock -net CLK
3  #assign_global_clock -net CLK90
4  assign_global_clock -net OUT_CLK
5  assign_global_clock -net BCO_CLK
```

```
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_0/Inst_fw_0/fifo_block_1/FIFOBLOCK0/U_9_1:PIN1 drives no load.
Warning: OnlineHelp :Q drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_ofb/Inst_ofb_1/Inst_ff_0/fifo_block_1/FIFOBLOCK0/U_5_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_0/Inst_fw_4/fifo_block_0/FIFOBLOCK0/U_11_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_1/Inst_fw_1/FULL:Q drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_0/Inst_fw_1/fifo_block_1/FIFOBLOCK0/U_5_1:PIN1 drives no load.
Warning: OnlineHelp :Q drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_ofb/Inst_ofb_0/Inst_ff_0/fifo_block_1/FIFOBLOCK0/U_11_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_1/Inst_fw_2/fifo_block_1/FIFOBLOCK0/U_15_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_0/Inst_fw_2/fifo_block_0/FIFOBLOCK0/U_8_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_ofb/Inst_ofb_0/Inst_ff_0/fifo_block_0/FIFOBLOCK0/U_15_0:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_0/Inst_fw_0/fifo_block_1/FIFOBLOCK0/U_8_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_ofb/Inst_ofb_1/Inst_ff_0/fifo_block_1/FIFOBLOCK0/U_3_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_1/Inst_fw_0/fifo_block_0/FIFOBLOCK0/U_15_0:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_ofb/Inst_ofb_1/Inst_ff_0/fifo_block_0/FIFOBLOCK0/U_7_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_0/Inst_fw_2/fifo_block_0/FIFOBLOCK0/U_7_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_ofb/Inst_ofb_1/Inst_ff_0/fifo_block_0/FIFOBLOCK0/U_1_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_1/Inst_fw_1/fifo_block_0/FIFOBLOCK0/U_11_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_ofb/Inst_ofb_0/Inst_ff_1/fifo_block_0/FIFOBLOCK0/U_10_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_1/Inst_fw_2/fifo_block_1/FIFOBLOCK0/U_9_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_1/Inst_fw_0/fifo_block_1/FIFOBLOCK0/U_9_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_0/Inst_fw_4/fifo_block_0/FIFOBLOCK0/U_5_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_0/Inst_fw_2/fifo_block_1/FIFOBLOCK0/U_6_1:PIN1 drives no load.
Warning: OnlineHelp :Q drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_1/Inst_fw_2/fifo_block_1/FIFOBLOCK0/U_8_1:PIN1 drives no load.
Warning:  CMP202: Pin Inst_roc_block/Inst_arbiter/Inst_fb/Inst_fb_0/Inst_fw_3/fifo_block_0/FIFOBLOCK0/U_5_1:PIN1 drives no load.
```

Another concern : a lot warning

- Is it ok to comment them out ?
- Does this code been successfully compiled in NWU ?
  - If yes, what the IDE version you use?

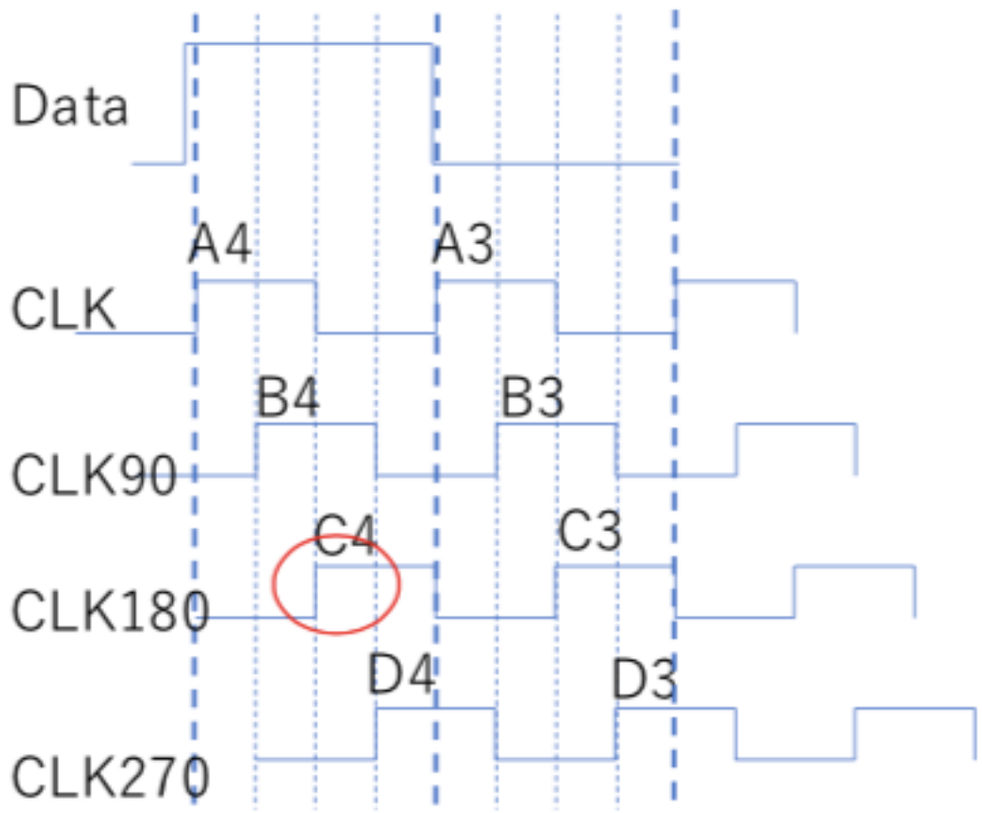
ROC FPGA firmware

- We only see 2 clock, CLK and CLK90 in the code, not 4.

In ROC_top.vhd

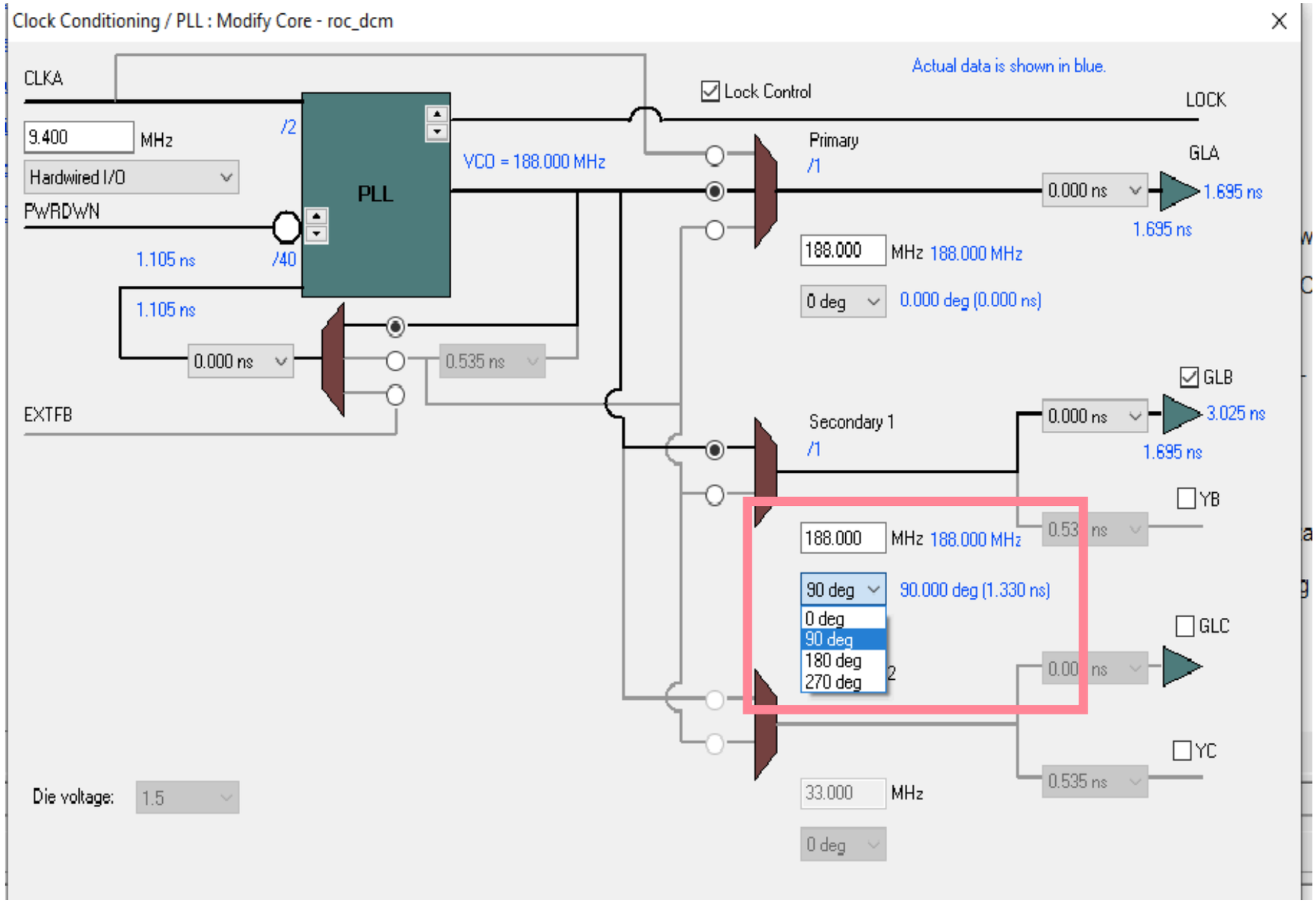
```
component roc_block is
 Port (
    RST : in std_logic;
    BCO_CLK : in std_logic;
    CLK : in std_logic;
    CLK90 : in std_logic;
    OUT_CLK : in std_logic;
    LATCH : in std_logic;
    SEND_DATA_0 : in std_logic;
    SEND_DATA_1 : in std_logic;
```

Plot from Takashi's report



ROC FPGA firmware

- We can change the clock directly by the GUI below.

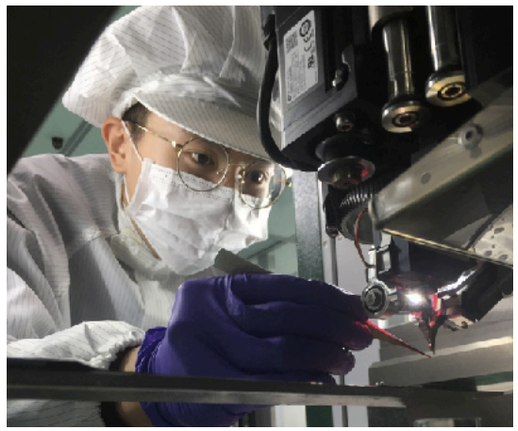


Summary

- We will try to apply the DP460 in NCU.
- The macro of channel classification is uploaded.
- I will test the PMT with different supply voltage.
- INTT FPGA to do list :
  - We will try to load the original code from (comment out the error 2 lines) to one FPGA, and see whether it can work or not.
    - Concern : if FPGA fails to work, it is dead. We don’t have solution to recover it (we don’t know the original code version in FPGA).
  - We will change the clock directly by the GUI, and load the code to FPGA and test it.
  - I will initiate a mail for the discussion

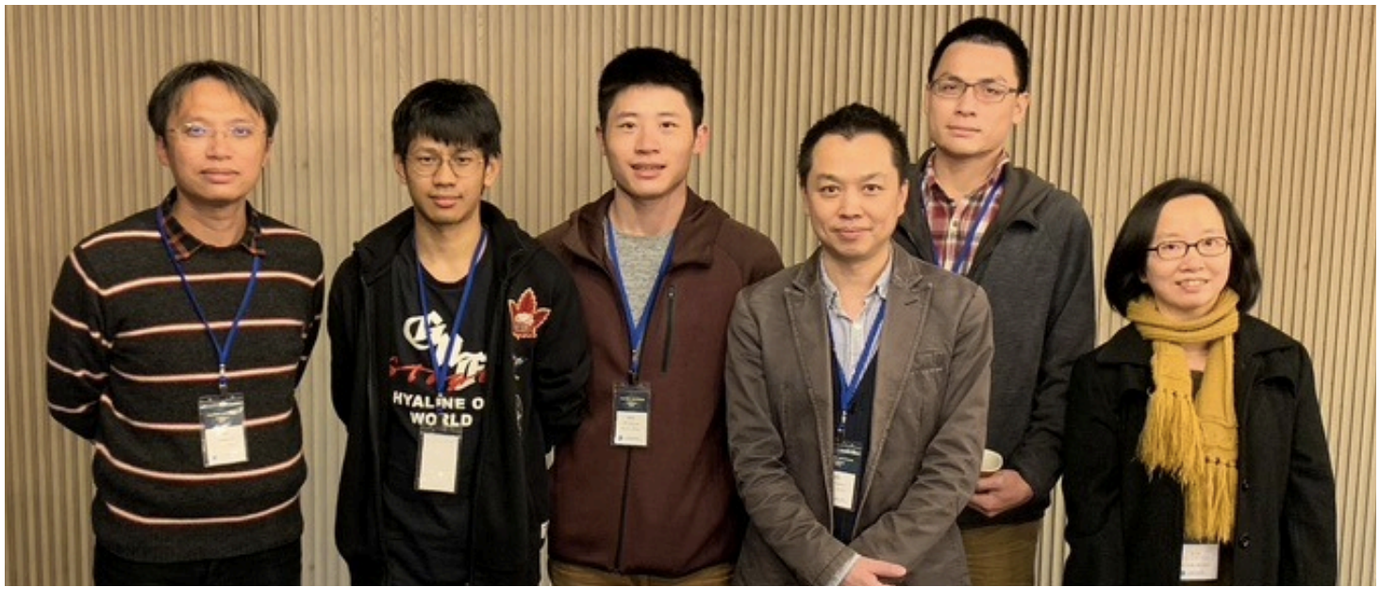
Back up

Taiwan INTT team



Ou-Wei Cheng

Kai-Yu Cheng



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Wei-Che Tang Rong-Shyang Lu Janny Huang