LGADs for EIC

By

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LGADs for EIC

- Several EIC subsystems will benefit from fast-timing (20-50 ps) for PID, fwd proton tagging
- Fast-timing can also be combined with precision tracking (4D detector) to save material budget, detector volume, no. electronic channels
- Examples of subsystems with such requirements are TOF, 4D tracker, Roman Pots, preshower
  - TOF:
    - **Position resolution:** ~30-50 μm (had. EC), ~300 μm (barrel, el. EC)
    - **Time resolution:** ~20-30 ps
    - **Tot active area:** ~7m^2/layer (had EC), 10-20 m^2/layer (barrel), 1m^2/layer (el. EC)
  - 4D tracker
    - **Position resolution:** few μm for strips in outer layers
    - **Time resolution:** ~30 ps
    - **Tot active area:** O(10) m^2/layer
  - Roman Pots:
    - **Time:** 30-50 ps
    - **Pixelation:** 500x500 μm^2
    - **Inactive edges:** < 150 μm
    - **Tot active area:** 0.13 m^2

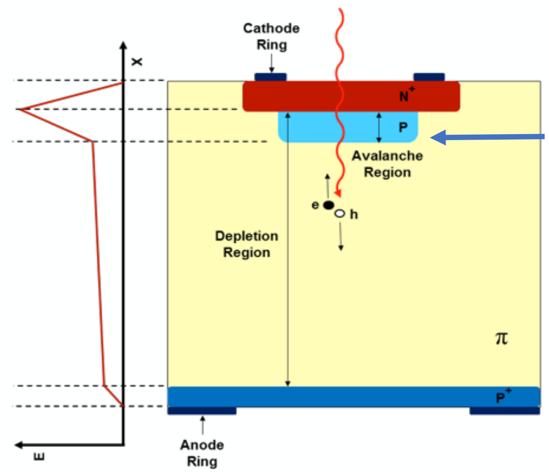
LGAD Consortium: discussions on common experience, challenges and solutions across different LGAD applications at EIC (and beyond):
- Indico: https://indico.bnl.gov/category/323/
- Mailing list: lgads-eic@mailman.rice.edu
- Contact A. Tricoli (BNL) or Wei Li (Rice), if interested in joining discussions/mailing-list

LGAD Technology

- Low Gain Avalanche Diodes (LGADs) can meet those requirements
  - Developed for timing detectors at HL-LHC (ATLAS and CMS)

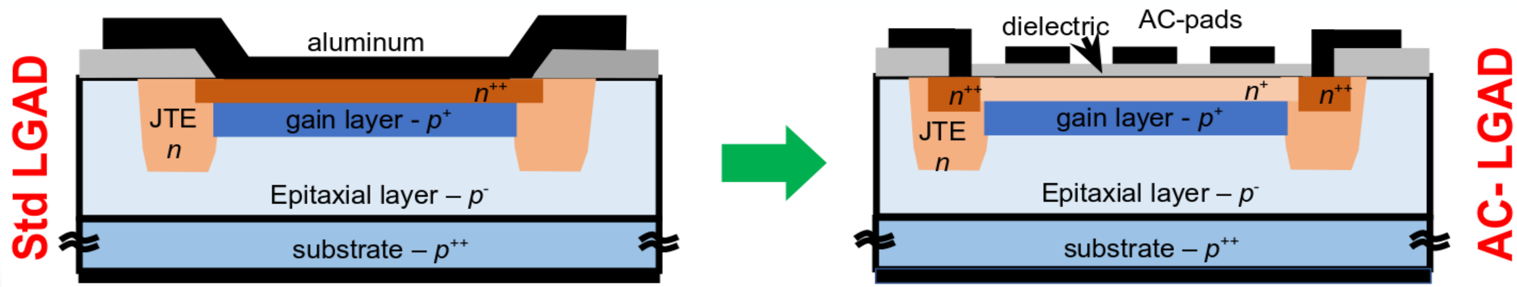
- **LGAD**:
  - **Silicon**-base technology
  - Fast-timing (**20-30 ps per hit**)
  - High Signal/Noise ratio

  → *Time resolution limited by Landau fluctuation in charge generation (the thinner is the sensor the faster it is)*



Electric Field: ~ 300 kV/cm in *Gain Layer*
Adjustable Gain: ~2-100

- ***AC-coupling allows pixelation and similar time resolution as LGADs***

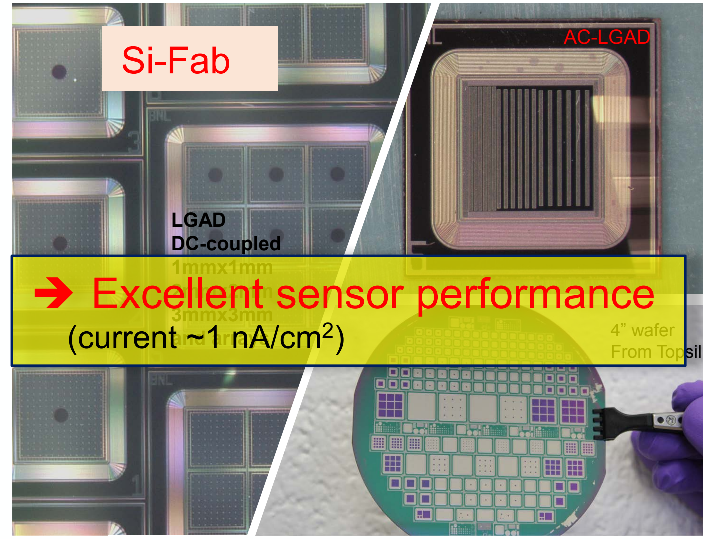


Large pads (1.3 mm²) → Timing only

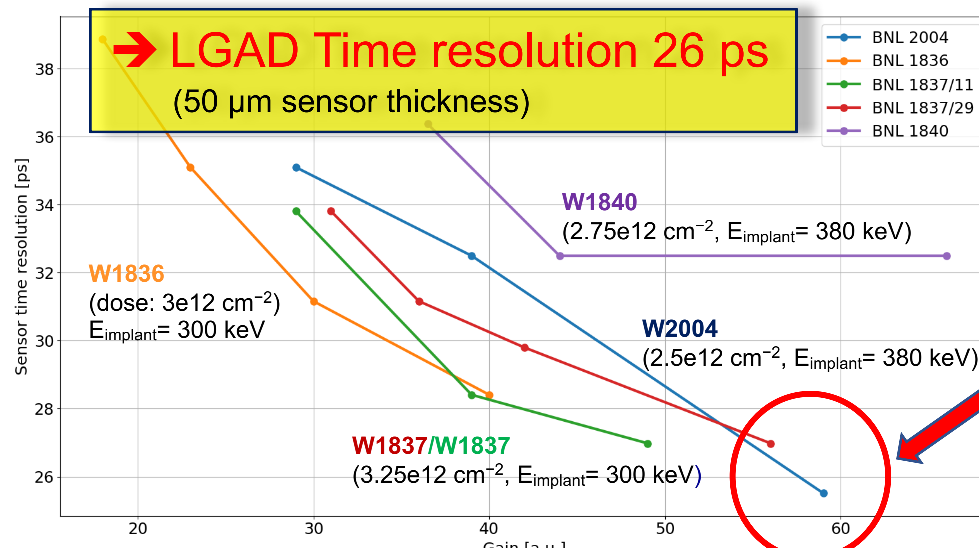
Can be finely pixelated → Time+Space (4D)
Pixel pitch mostly limited by in-pixel components in readout electronics

(AC-)LGADs at BNL

- Full LGAD R&D chain: design, fabrication, testing
- Several productions of LGADs and AC-LGADs with different designs (geometries, doping, gain etc.)
- Sensors are distributed to national and international collaborators for further and independent testing
- So far only (AC-)LGAD producer in the USA
- Other int'l producers are HPK (Japan), FBK (Italy), CNM (Spain), NDL (China), Micron, Te2V (UK)



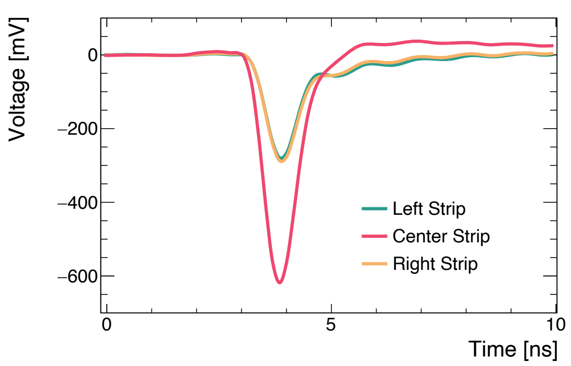
- ➢ 50 μm current active thickness
- ➢ 35-20 μm thicknesses will reduce Landau fluctuations and improve time resolution ➔ **goal ~20 ps per hit**



Performance of BNL's AC-LGADs

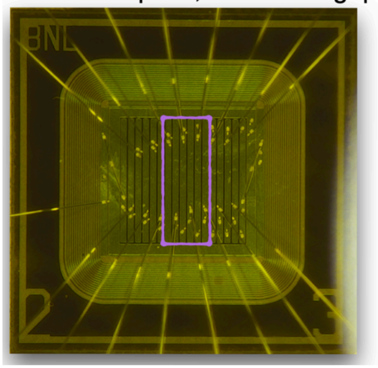
- Time resolution of AC-LGADs can be controlled to match LGADs (e.g. gain and n+ layer doping)
- AC-LGADs can measure space points with resolution better than pixel detectors by exploiting signal sharing between AC-coupled electrodes
- Measurements Space+Time resolution
  - Lab measurements with lasers and radioactive sources
  - FNAL Test Beam Facility (FTBF) with 120 GeV protons

AC-LGADs
- **Fast-timing: ~30 ps** (50 μm thickness)
- **Pixelation** as in pixel detector ~10s μm
- **High S/N** ratio
- **100% fill factor**
- **Edgeless** demonstrated: **<150 μm**
- **Signal sharing → improved space resol.**
- **Produced by BNL**



Signal induced on neighboring electrodes is exploited to improve space resolution

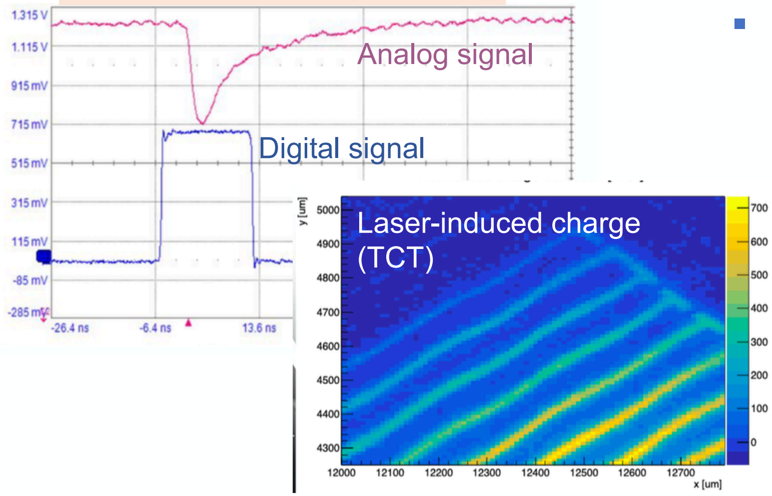
100 micron pitch, 20 micron gaps



→ <10-15 μm space resolution
→ ~30 ps time resolution
→ 100% particle detection efficiency

AC-LGAD readout

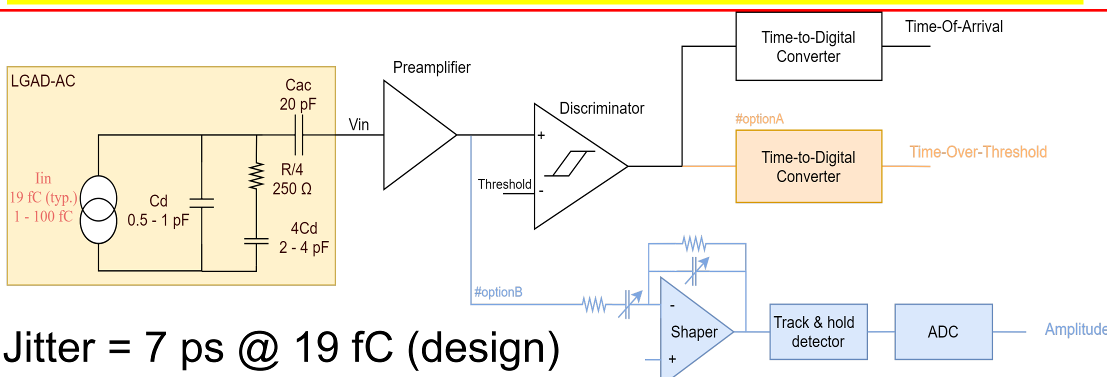
AC-LGAD + ALTIROC0



- ASIC readout tests (coll. with LAL/Omega, Paris)
  - ASIC developed for HL-LHC: ALTIROC 130 nm TSMC, two TDCs (TOA and TOT), large pitch (1.3x1.3 mm^2)

Signal induced on neighboring electrodes can be exploited to improve space resolution

Development of a dedicated 500 μm pitch ASIC (TDC+ADC)
(coll. with LAL/Omega, Paris)



Jitter = 7 ps @ 19 fC (design)

- Design is on-going
- Power dissipation goal: 1-3 mW/pixel
- Aim for 1st submission in ~Fall 2021

Readiness and Costs

- LGADs 1.3x1.3 mm^2 are qualified for use at HL-LHC (much harsher environment than EIC)
- AC-LGADs need more rigorous development and tests
  - Development at very fast pace, led by several group world-wide for different applications
  - Current research is exploring technology limits, e.g. best time and space resolution
  - With time and clearer specifications for EIC applications, R&D will become more directed, e.g. long term stability and reliability for specific designs (e.g. pixel/strip pitch)
  - **~2 year time scale for an advanced prototype with 30-40 ps time resolution**
  - **Longer time scale for an advanced prototype with 20-30 ps time resolution**
- Critical are readout electronics (ASICs)
  - Need time and money for development
  - Challenges: neighboring electrode readout, power dissipation, fine pitch (<500 μm)
  - Design depends on specific sensor geometry and requirements, and detector environment
  - **~3 years for a prototype, ~5 years for a demonstrator**
- Time synchronization to EIC clock
  - EIC clock jitter at crate measured <4 ps (valuable experience from LHC)
- Cost dominated by silicon sensors and ASICs (can be shared between subdets. or experiments)
  - ASICS: 1) NRE $221k including 6 wafers, 2) $1.2k per wafer. Cheaper with Multi Layer Masks (MLM)
  - Sensor fabrication: ~$200/cm^2 (including labor and materials) – costs of AC-LGAD similar to LGADs
  - Detector cost also scales with no. of channels and area (e.g. electronics, cooling)