

WaveForm Analysis

RKEN/RBRC

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on behalf of Bus Extender Team

Half Entry Issue Debugging Strategy

1. Data analysis of the observed waveform (μ , YA, Taskahi, IN)
 - Waveform comparison
 - Eye diagram
2. Individual Chip Reset (Genki, Yasuyuki)
 - Keep resetting only the FPHX chip causes the half entry. Rests are to be remain un-reset between Runs.
3. Phase Follower Tuning at ROC-FPGA
 - FPGA code was developed in Taiwan and available for testing
 - Prepare ROC board for this testing. 3V regulator is to be installed to the ROC-7. This board is to be dedicated for this study. There is potential risk we cannot re-install the original code to the ROC data FPGA.
 - In the meantime, wait for #1 analysis

Half Entry Debugging (5/26 ~ 28)

Inviting Takashi Kondo from Tokyo Industrial Research Center for monitoring data transmission.

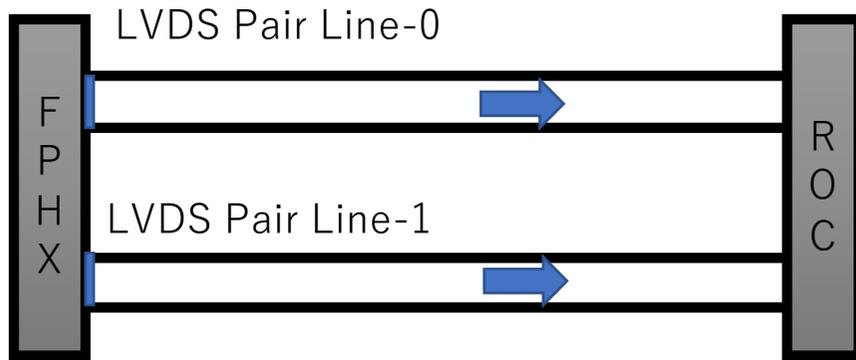


The results presenting today are the observation at the back of the ROC board

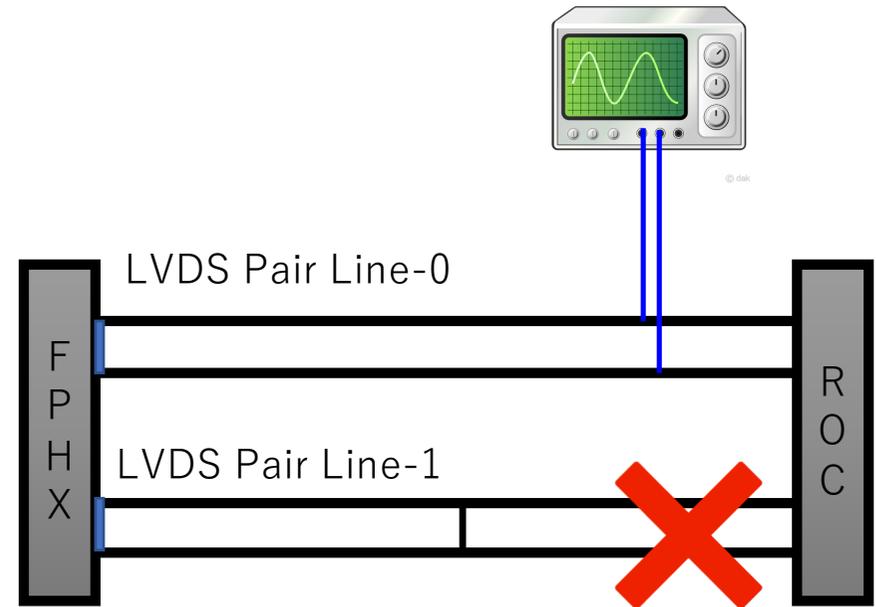
Possible Scenarios of Transmission Failure

1. Missing Sync Bit & Word Mark
2. Insufficient Signal Amplitude
3. Screwed up Phase (Timing)

Measurement Method



FPHX Data Transmission Concept



Disable opponent LVDS Pair line so that we know the data monitoring are accepted by the ROC



Run Log

No.	filename	INTT	Bus-extender	Intcpt-bd	Conv.	ROC	port	LVDS current	probe	chip-line	data	other	note
6	1 01.txt					ROC9	A-3						
7	2 02-a.txt												
8	3 02-b.txt												
9	4 02-c.txt												
10	Probing Point @ Interception Board												
11	5 03-a.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT0	chip13_line0	20210526-1505			full
12	6 03-b.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT0	chip13_line0	1509			full
13	7 03-c.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT0	chip13_line0	1513			full
14	8 03-d.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT0	chip13_line0	1519			half
15	9 03-e.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT0	chip13_line0	1524			half
16	10 03-f.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT0	chip13_line0	1529			full
17	11 03-g.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT0	chip13_line0	1534			full
18	12 03-h.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT0	chip13_line0	1537			half
19	13 04-a.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT1	chip13_line1	1544			full
20	14 04-b.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT1	chip13_line1	1548			full
21	15 04-c.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT1	chip13_line1	1600			half
22	16 04-d.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT1	chip13_line1	1604			full
23	17 04-e.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT1	chip13_line1	1608			full
24	18 04-f.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT1	chip13_line1	1612			full
25	19 04-g.txt	PPB2-LSN new4	No.003	#large 9	ROC3 C-3	8mA	J1	chip13_OUT1	chip13_line1	1616			full

No.	filename	INTT	Bus-extender	Intcpt-bd	Conv.	ROC	port	LVDS current	probe	chip-line	data	other	note
103	96 30-a.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R815	chip7_line1	1518				half
104	97 30-b.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R815	chip7_line1	1521				half
105	98 30-c.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R815	chip7_line1	1524				half
106	99 30-d.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R815	chip7_line1	1528				half
107	100 31-a.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R813	chip7_line0	1538				half
108	101 31-b.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R813	chip7_line0	1541				half
109	102 31-c.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R813	chip7_line0	1544				half
110	103 32-a.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R813	chip7_line0	1557	J1 chip07_OUT1, chip08_OUT1	short		nothing
111	104 32-b.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R813	chip7_line0	1606	J1 chip07_OUT1, chip08_OUT1	short		nothing
112	105 32-c.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R813	chip7_line0	1609	J1 chip07_OUT1, chip08_OUT1	short		nothing
113	106 33-a.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R952	chip8_line0	1617	J1 chip07_OUT1, chip08_OUT1	short		half
114	107 33-b.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R952	chip8_line0	1626	J1 chip07_OUT1, chip08_OUT1	short		dirty
115	108 33-c.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R952	chip8_line0	1632	J1 chip07_OUT1, chip08_OUT1	short		dirty
116	109 34-a.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R815	chip7_line1	1644	J1 chip07_OUT0, chip08_OUT0	short		half
117	110 34-b.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R815	chip7_line1	1646	J1 chip07_OUT0, chip08_OUT0	short		half
118	111 34-c.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R815	chip7_line1	1649	J1 chip07_OUT0, chip08_OUT0	short		half
119	112 35-a.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R950	chip8_line1	1658	J1 chip07_OUT0, chip08_OUT0	short		nothing
120	113 35-b.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R950	chip8_line1	1701	J1 chip07_OUT0, chip08_OUT0	short		nothing
121	114 35-c.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R950	chip8_line1	1703	J1 chip07_OUT0, chip08_OUT0	short		nothing
122	115 36-a.txt	PPB2-LSN new4	No.006	#large 9	ROC9 C-1	2mA	R950	chip4_line0	1737	J2 chip17_OUT1	short		chip4 full, chip

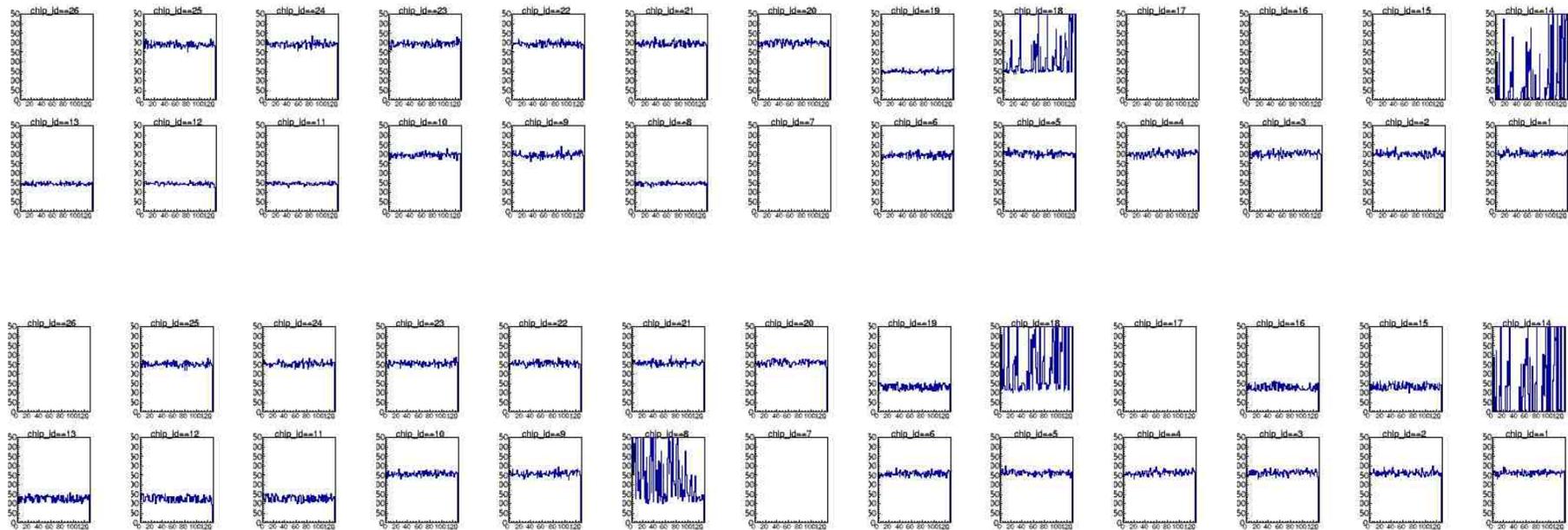
Courtesy of μ

Probe Point @ ROC Backplane

CHIP-ID	Line	Transmission	Scope Measurement #		
			Golden	Silver	Bronze
4	0	Success			36
	1	Success			37
7	0	Fail	32		
	1	Success	34		
8	0	Success	33A	33B,C	
	1	Fail	35		
19	0	Fail	38		
	1	Success		39	

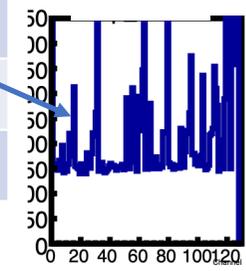
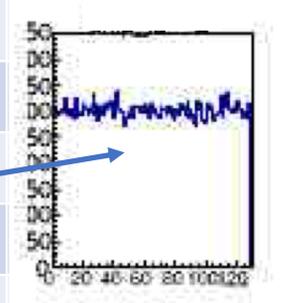
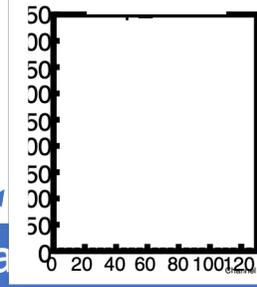
Golden : Perfect control of failure/successful transmission lines.
 Silver : Transmission successful, but data look ugly (ザビザビ).
 Bronze : Alternative line was not shorted.

Typical Calibration Results



Probe Point @ ROC Backplane

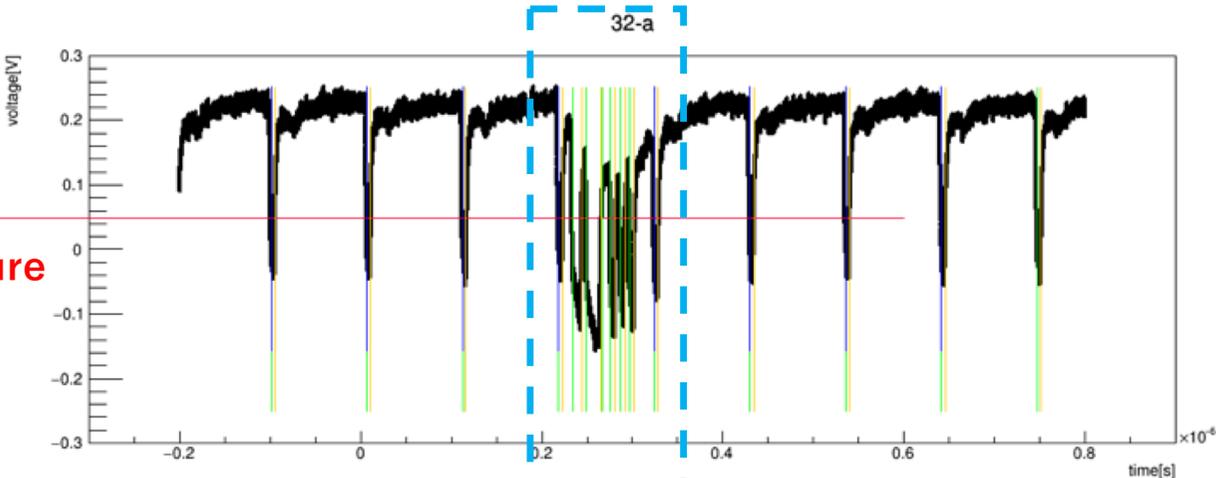
CHIP-ID	Line	Transmission	Scope Measurement		
			Golden	Silver	Bronze
4	0	Success			
	1	Success			
7	0	Fail	32		
	1	Success	34		
8	0	Success	33A	33B,C	
	1	Fail	35		
19	0	Fail	38		
	1	Success		39	



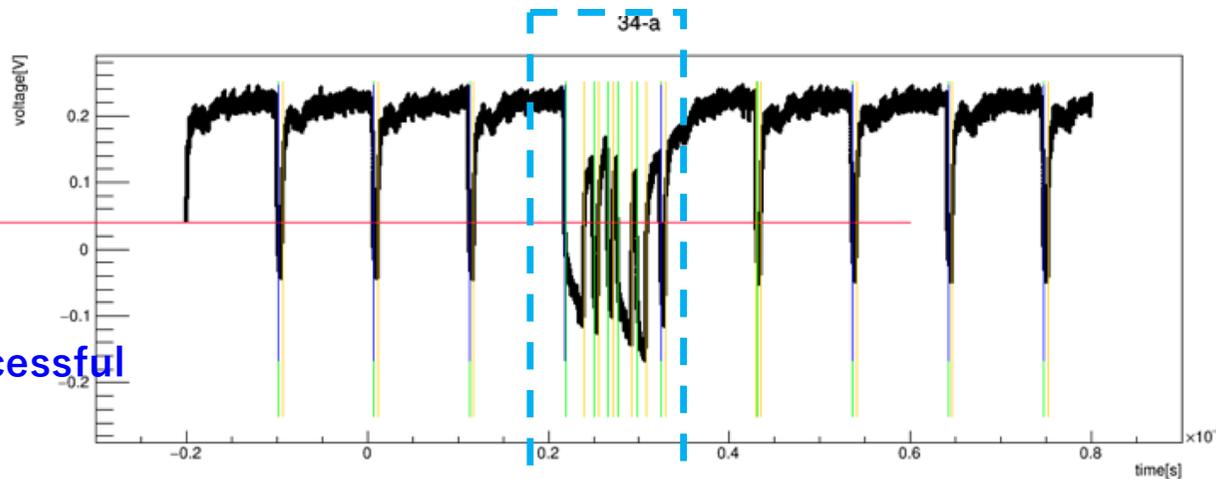
Golden : Perfect control of failure/successful transmission lines.
Silver : Transmission successful, but data look ugly (ザビザビ).
Bronze : Alternative line was not shorted.

Chip-7 Waveform Comparison (Wide)

Transmission Failure



Transmission Successful



Courtesy of Takashi

Zoom in next page

FPHX Data Bit Structure

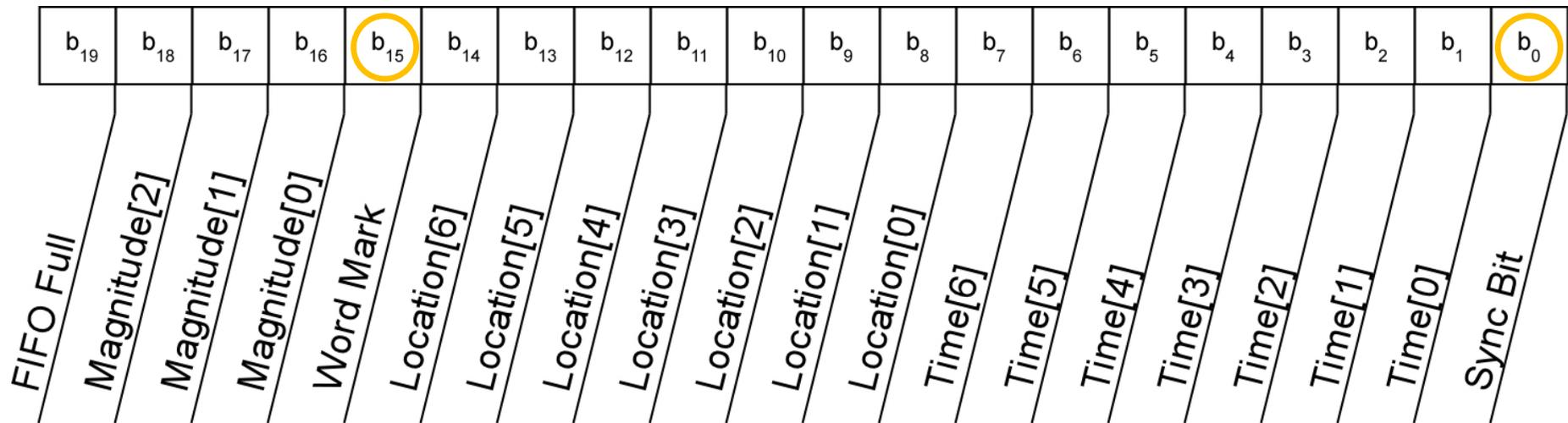


Figure 5 - The Serial Output Data Word Structure

Serial Words

Each of the FPhx's two serial output words will drive a continuous stream of 20-bit words. Each word will be 1 sync bit followed by 19 data bits. If all 19 data bits are zeros, then that 20-bit word is a Sync Word placed in the data stream to enable the data acquisition hardware to align itself to the data flow from the FPhx chip. If the 19 data bits are NOT all zeroes then that 20-bit word is a Data Word and it contains information on a hit strip. The data is organized as follows:

1. Word Mark Check (Chip-7)

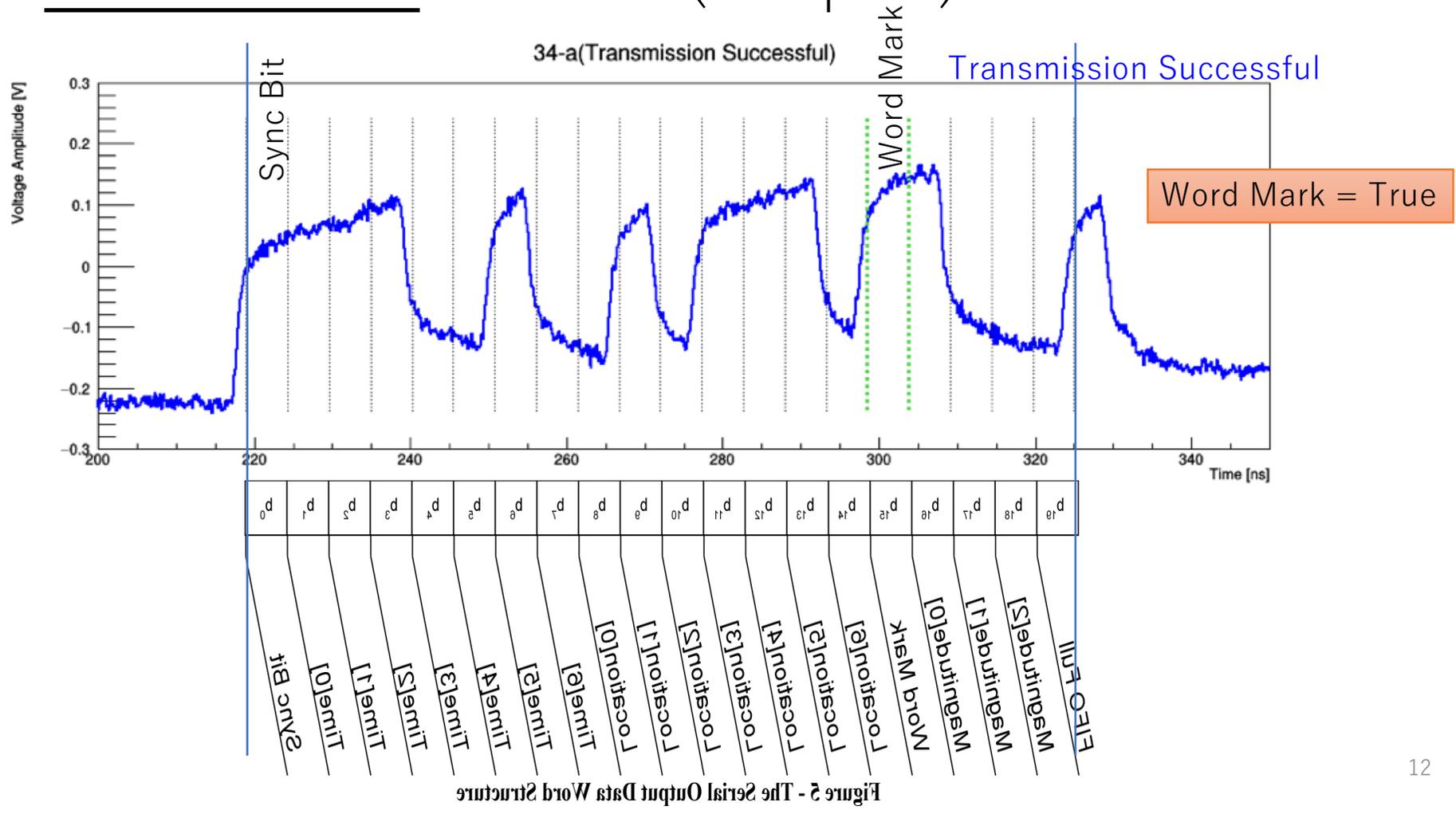
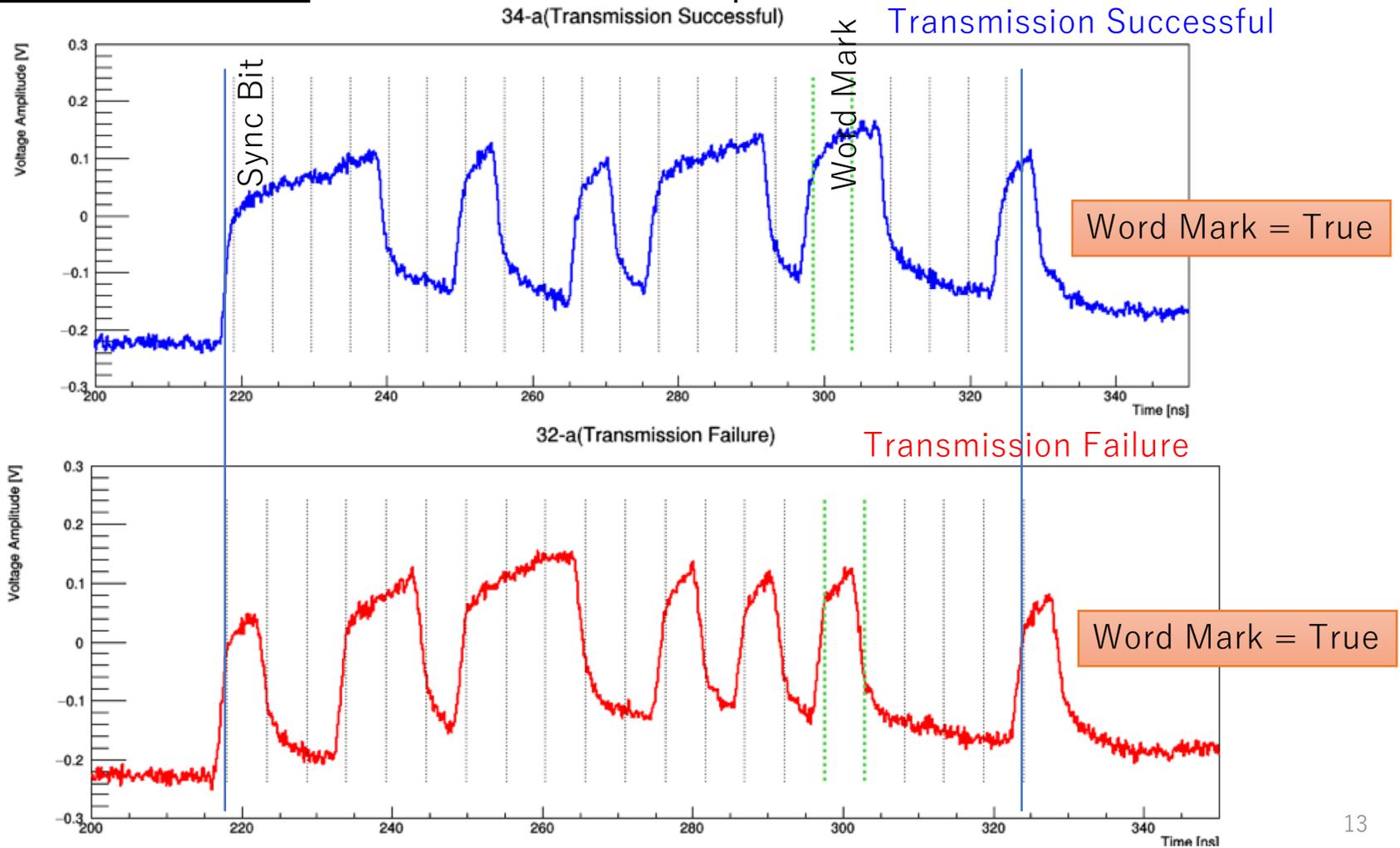


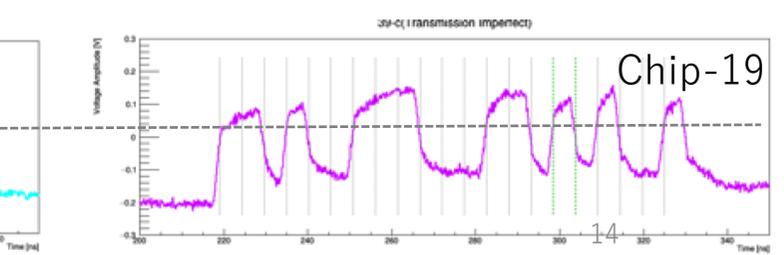
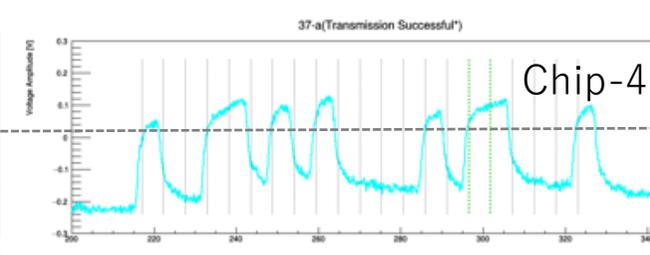
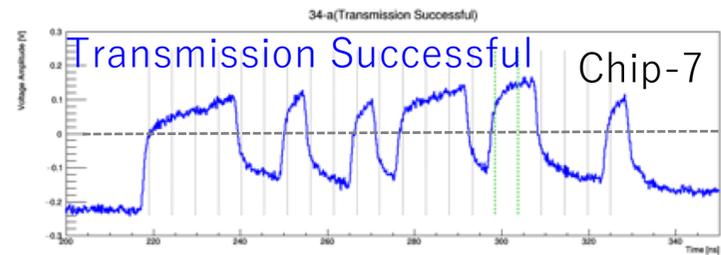
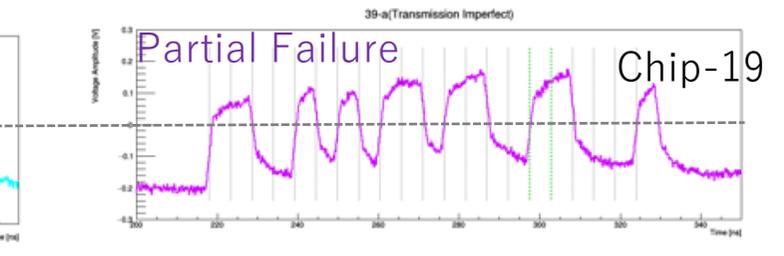
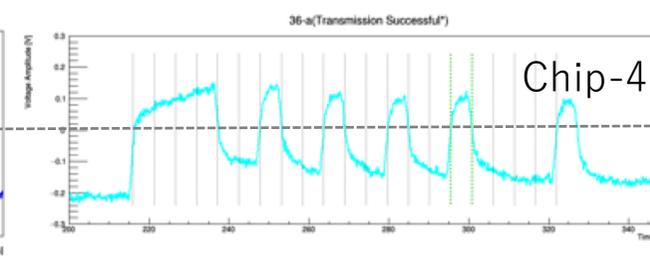
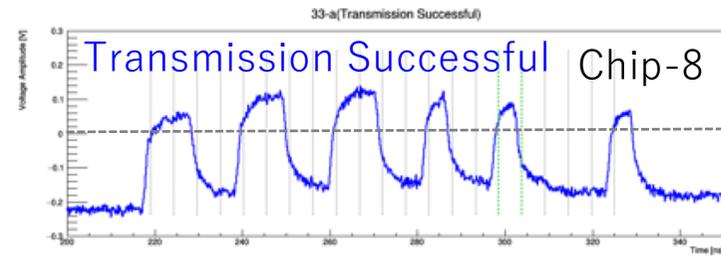
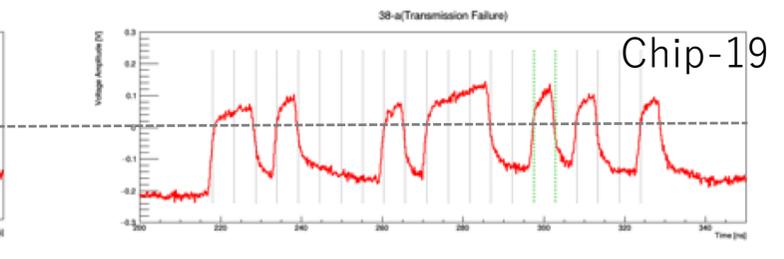
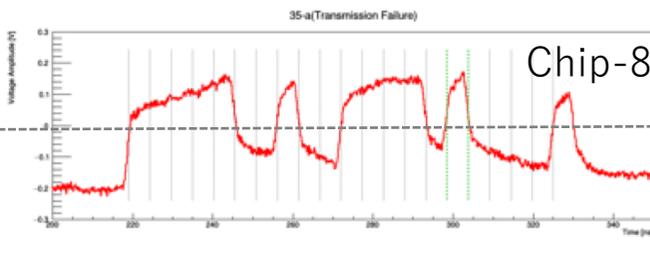
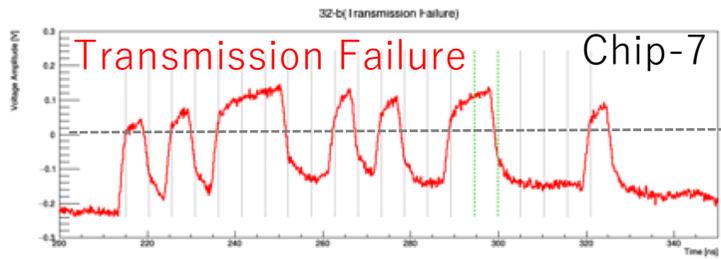
Figure 2 - The Serial Output Data Word Structure

1. Word Mark Check (Chip-7)



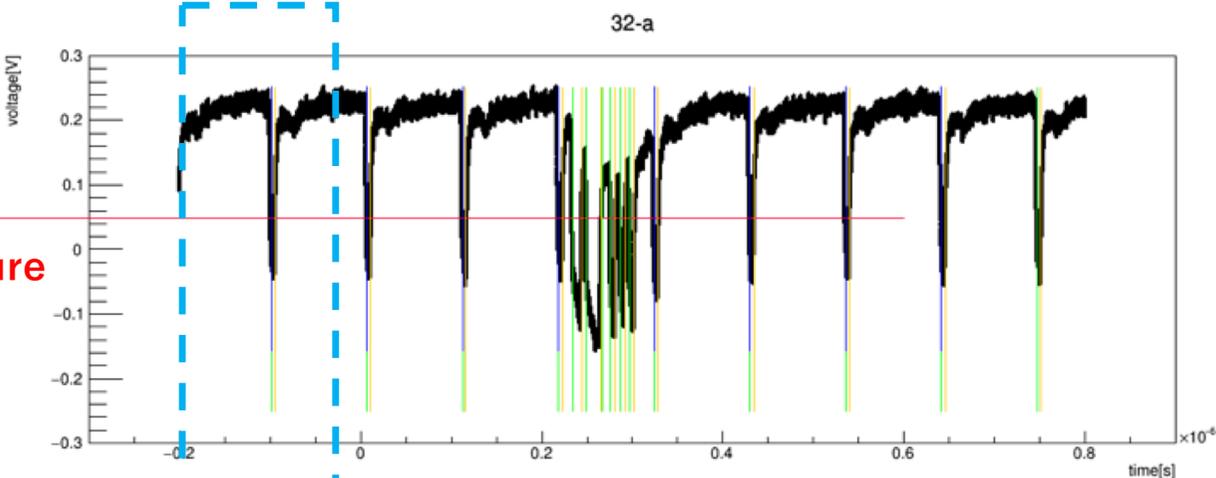
1. Word Mark Check All

Word Marks were confirmed to be always true
Also pulse height seems to be sufficient.

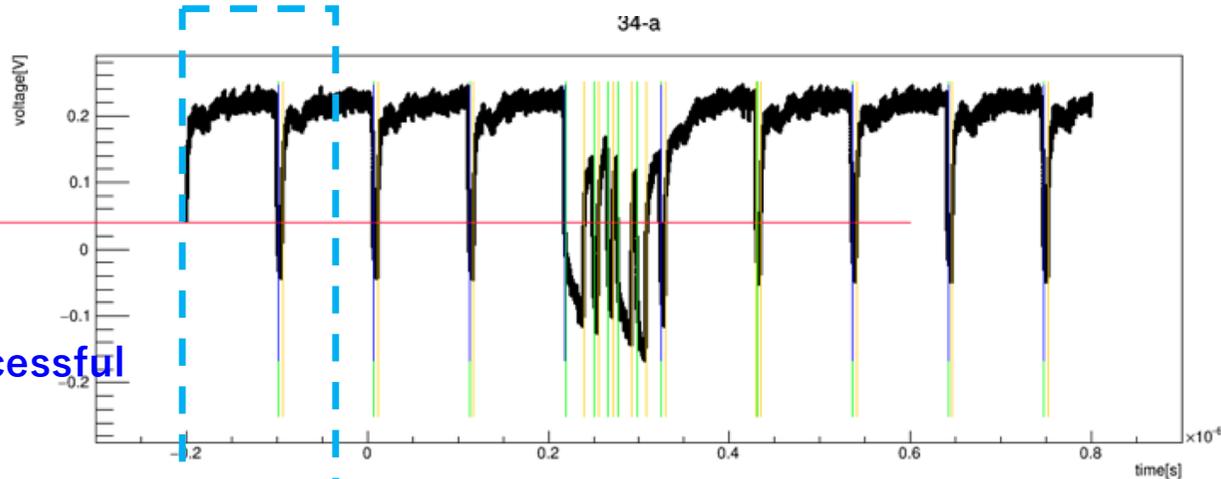


Chip-7 Waveform Comparison (Wide)

Transmission Failure



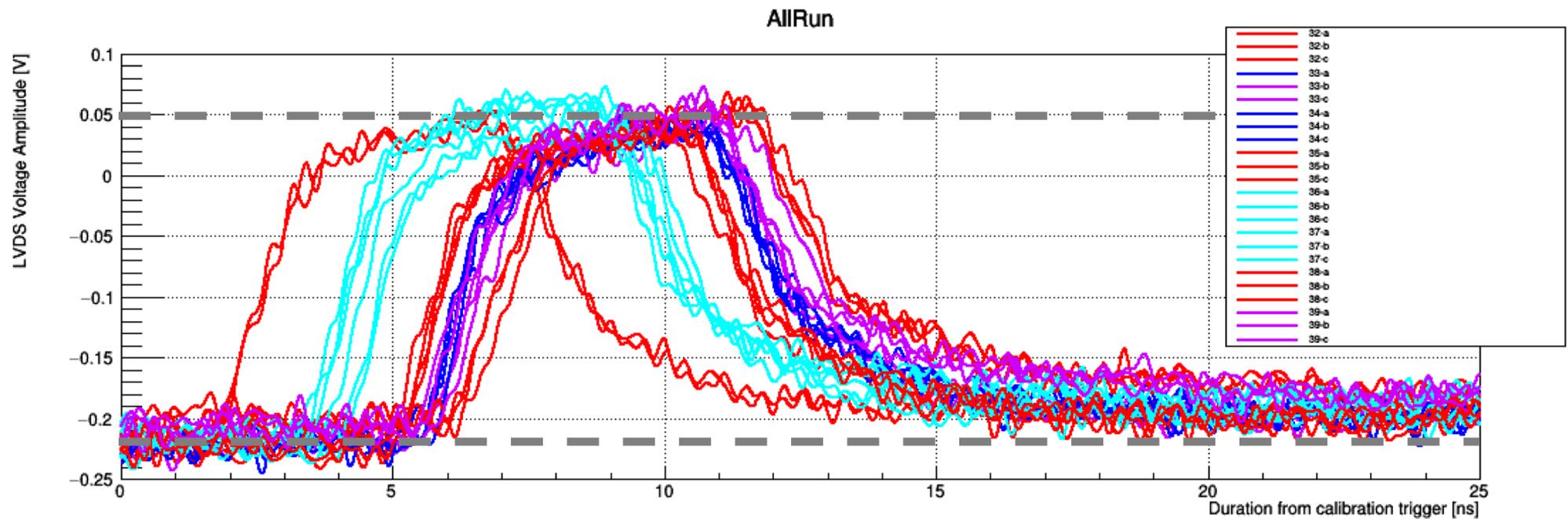
Transmission Successful



Courtesy of Takashi

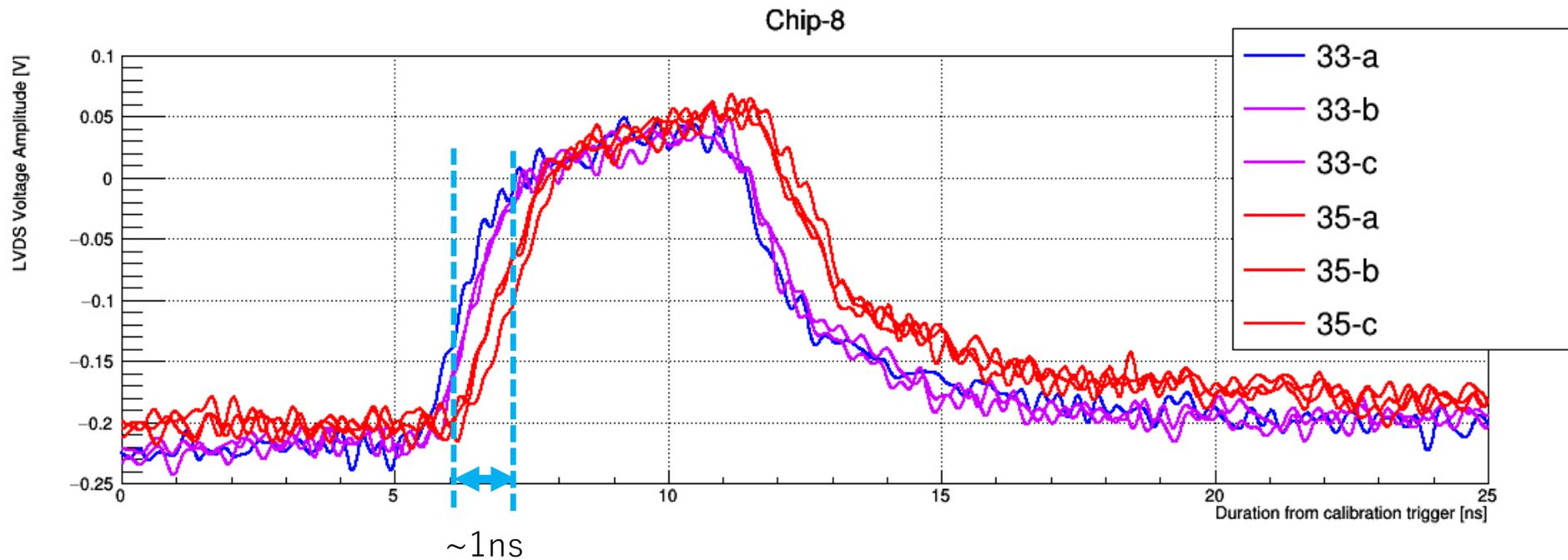
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2. Sync Bit Pulse Shape & Amplitude



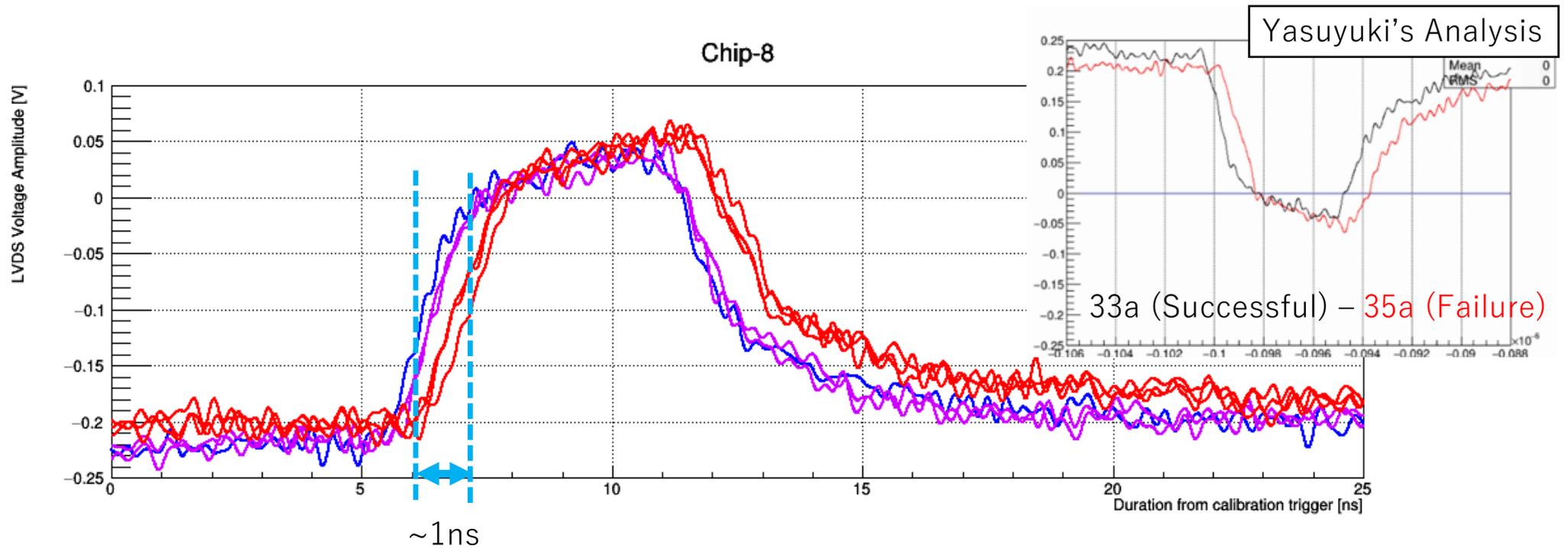
Did not observe obvious distortion of neither the pulse shape nor the amplitude between transmission successful and failure cases.

3. Relative Phase/Timing w.r.t. Trigger (Chip-8)



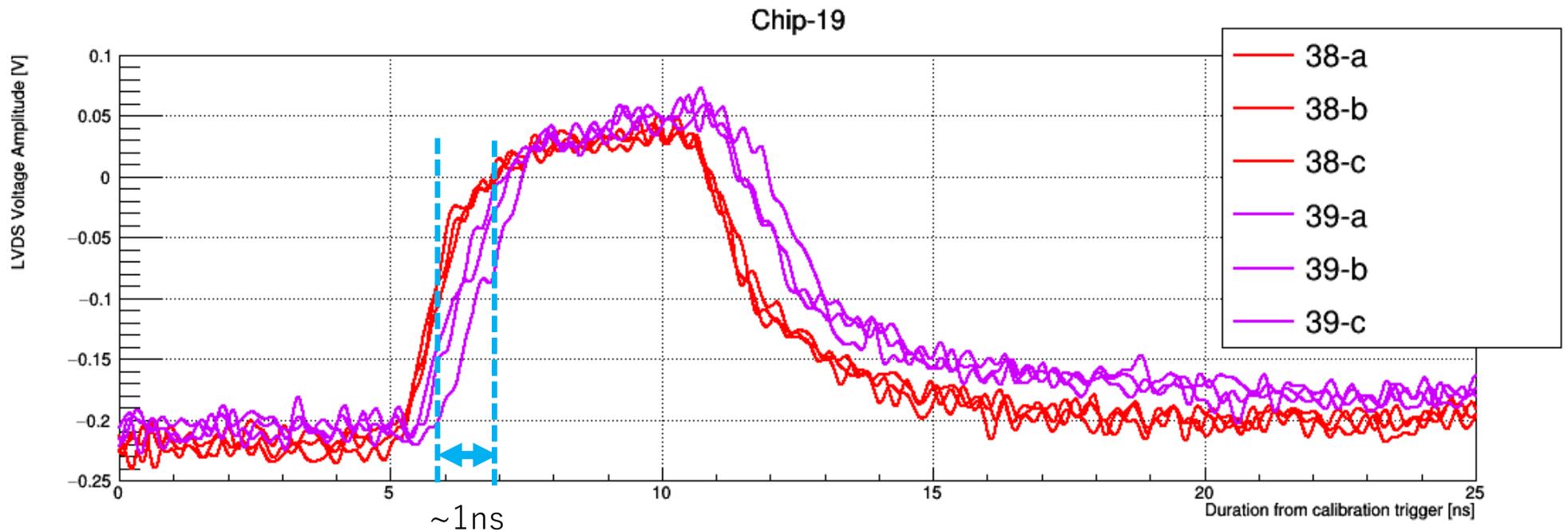
The timing is about 1ns late in the transmission failure cases compared to successful cases

3. X-Check with Yasuyuki's Analysis (Chip-8)



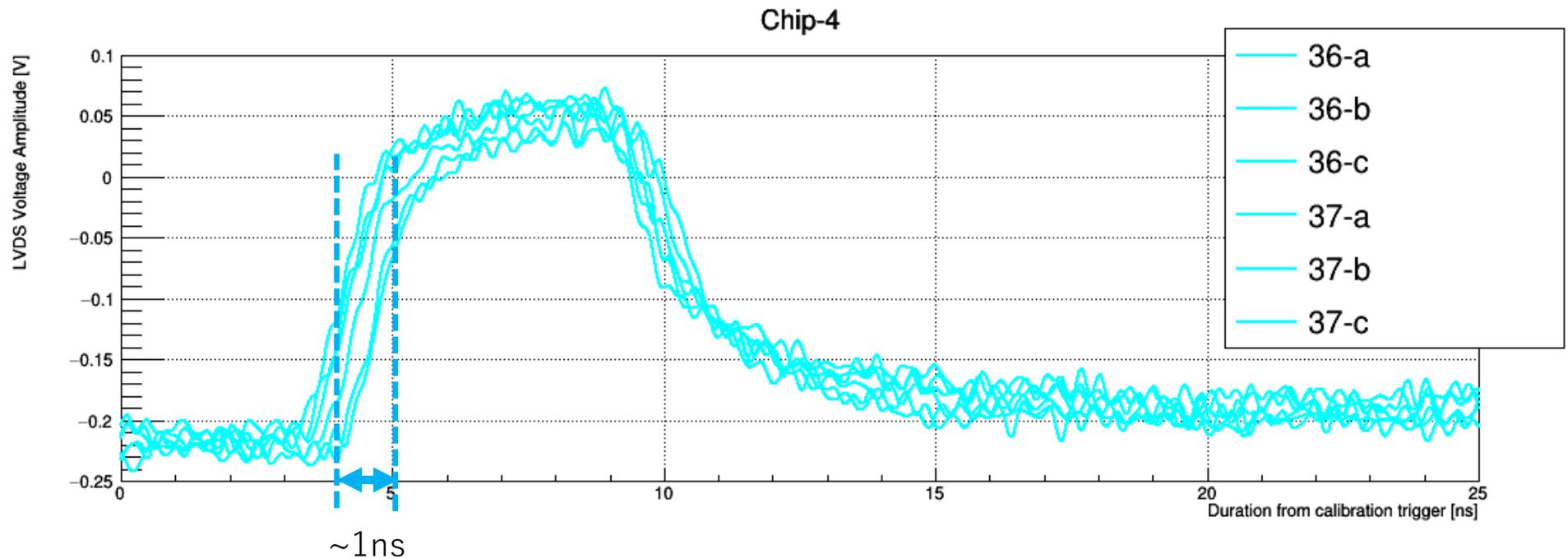
Consistent with Yasuyuki's Analysis

3. Relative Phase/Timing w.r.t. Trigger (Chip-8)



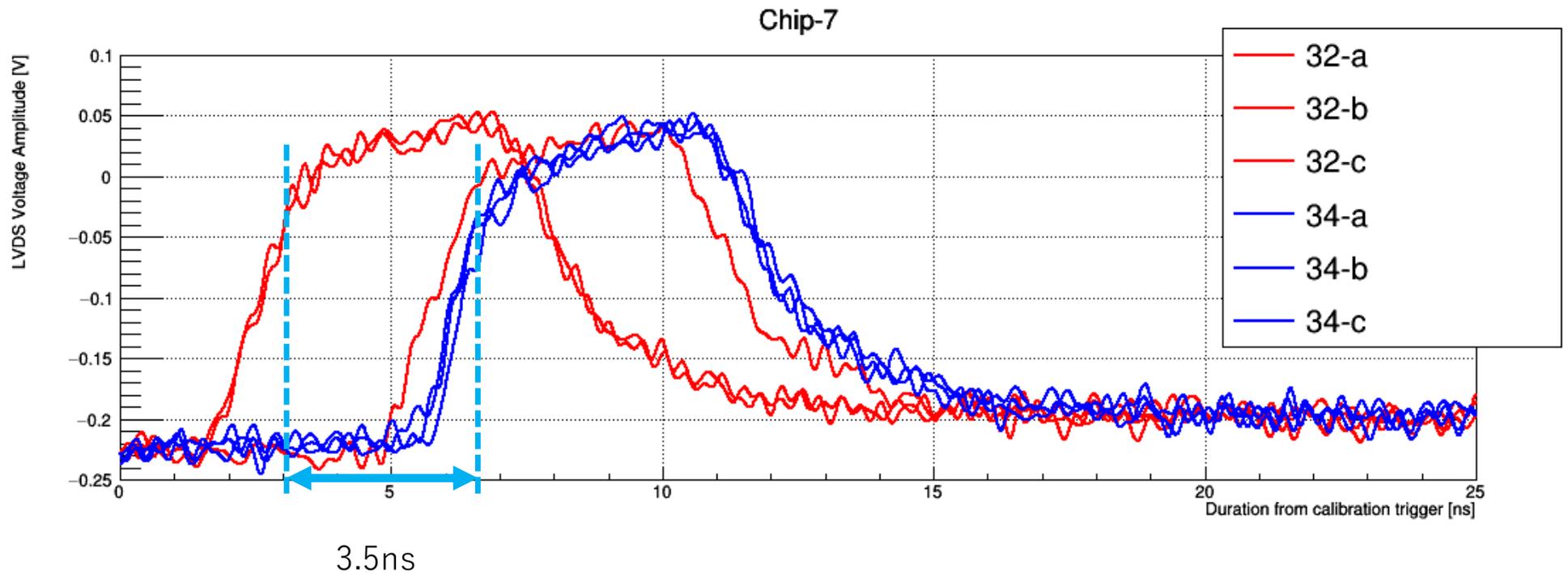
The timing is about 1ns late in the transmission partially failure cases compared to successful cases. Consistent with Chip-8 case.

3. Relative Phase/Timing w.r.t. Trigger (Chip-8)



The timing seems to be spread $< 1\text{ns}$. Unfortunately, the observation cannot lead to conclusive guidance because these pulse cannot be distinguished between from transmission successful or failure lines.

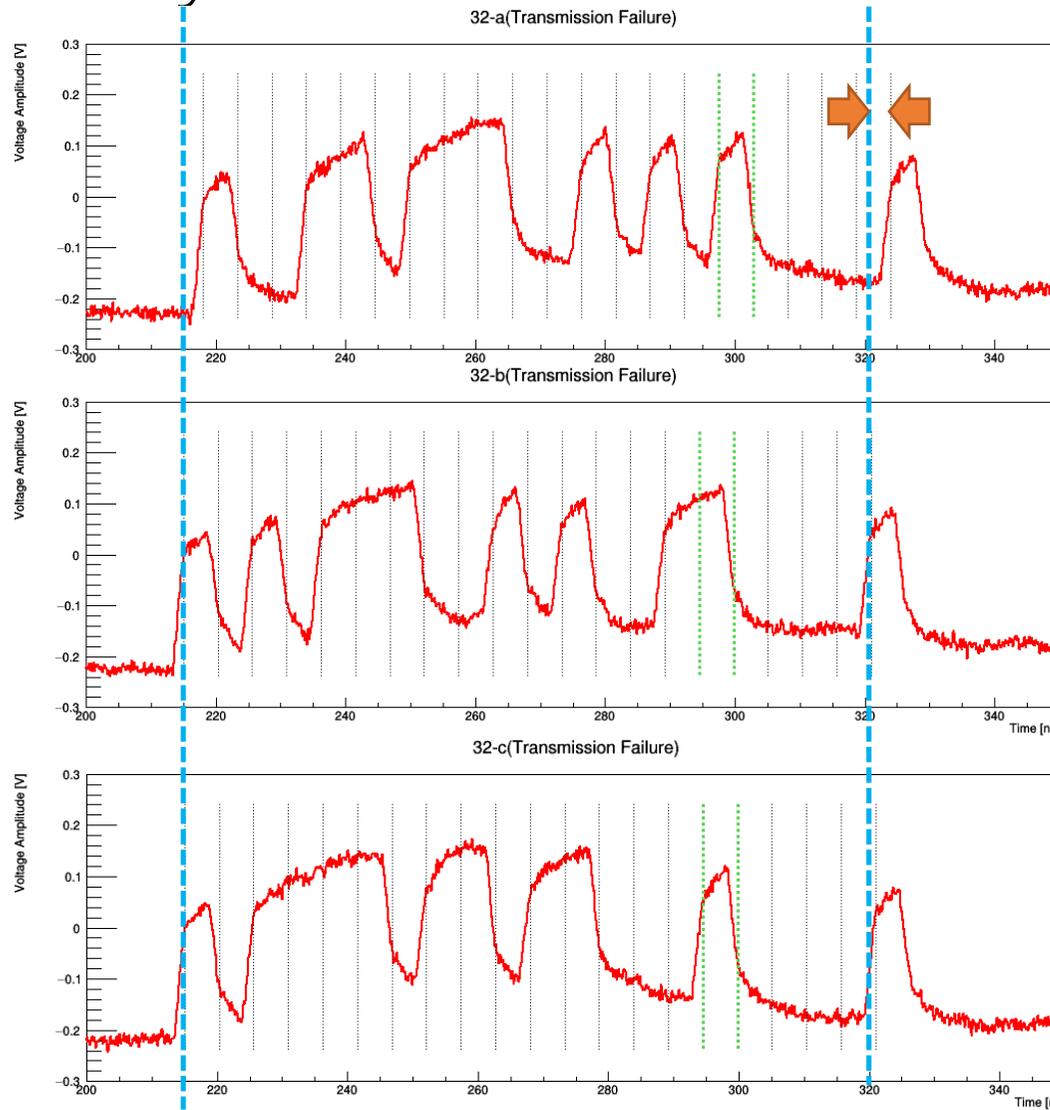
3. Relative Phase/Timing w.r.t. Trigger (Chip-7)



Observed as significant as 3.5ns timing difference between successful and failure transmission cases. However, there is one example (

3. Consistency Between Multi-Measurements

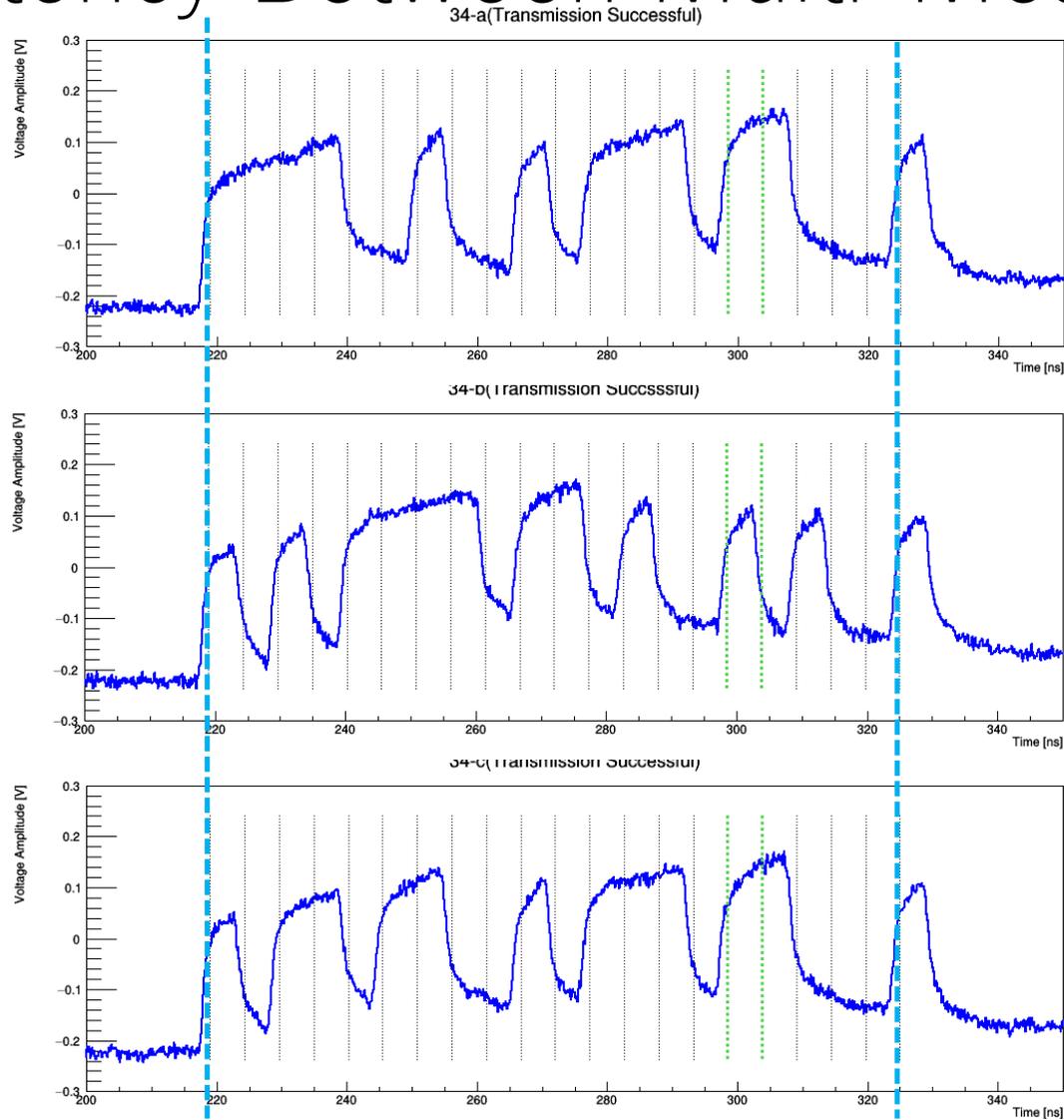
Chip-7
Run 32



32-b & 32-c are consistent,
but 32-a is off a bit

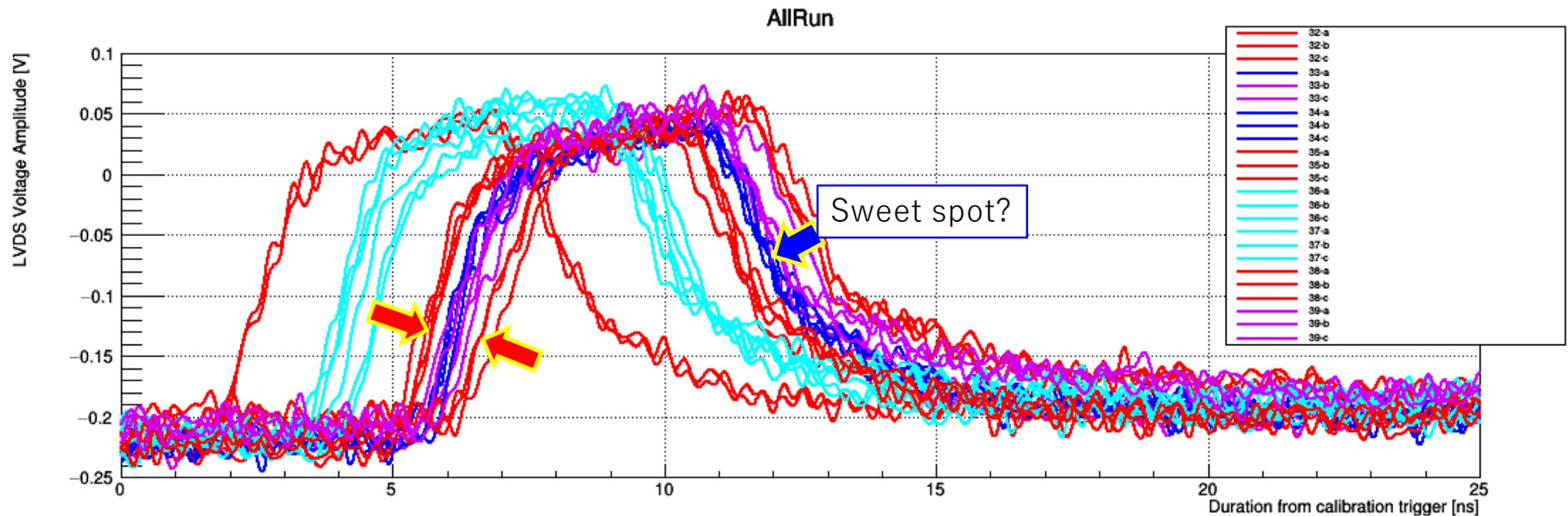
3. Consistency Between Multi-Measurements

Chip-7
Run 34



The timing seems to be quite consistent in all a,b,c measurements.

3. Sync Bit Pulse Shape & Amplitude



- All successful transmission signals 33-a and 34-a,b,c appear in the similar timing. Is this the “sweet spot” of 0.5ns band? However, partially failure measurements 33-b,c and 39-a,b,c appear in similar timing.
- The timing of transmission failure appears both earlier and later sides of the “sweet spot” as indicated by red arrows.
- Hard to conclude that we can expect improvement by the phase tuning unless we can do flexible custom tune chip-by-chip and run-by-run basis which is not feasible.

Summary

1. Missing Sync Bit & Word Mark

- Confirmed these bits are always true regardless of transmission successful or failure. No observation of particularly insufficient amplitude in these bits.

2. Insufficient Signal Amplitude

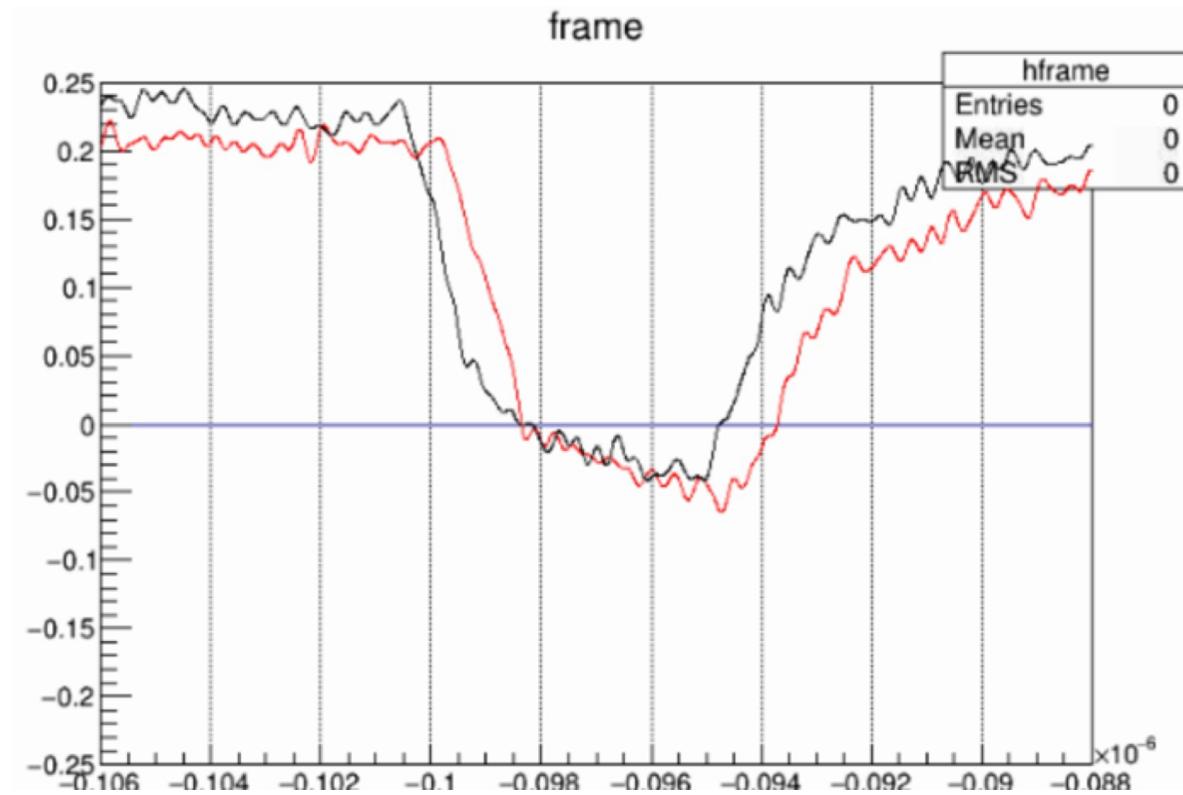
- As far as sync bit pulses are inspected, there is no obvious degradation of pulse height or deformation in the transmission failure cases compared to successful cases.

3. Screwed up Phase (Timing)

- Observed somewhat visible timing difference between transmission successful and failure cases. However a few cases doesn't necessarily follow the symptom. It is hard to draw consistent scenario to explain all phenomena at once.

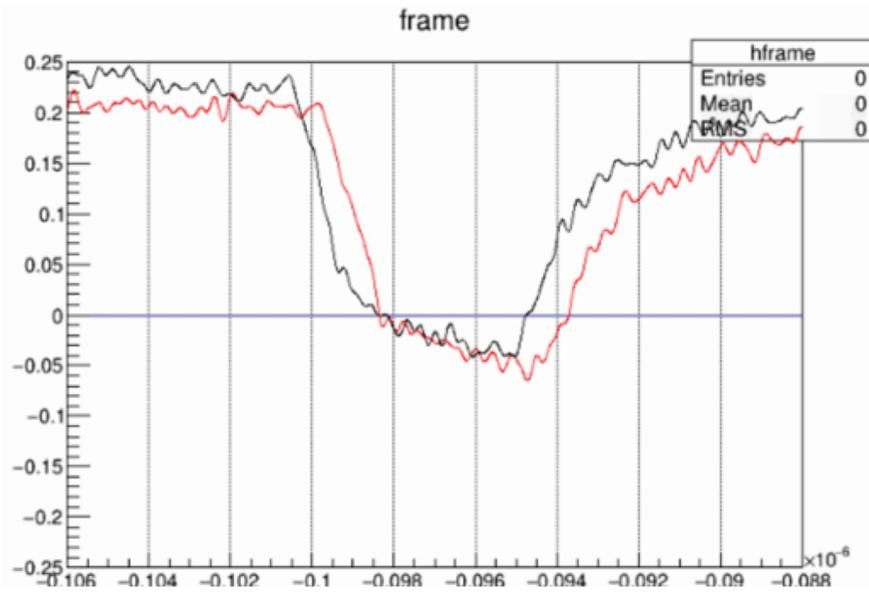
Backup

Zoom Up

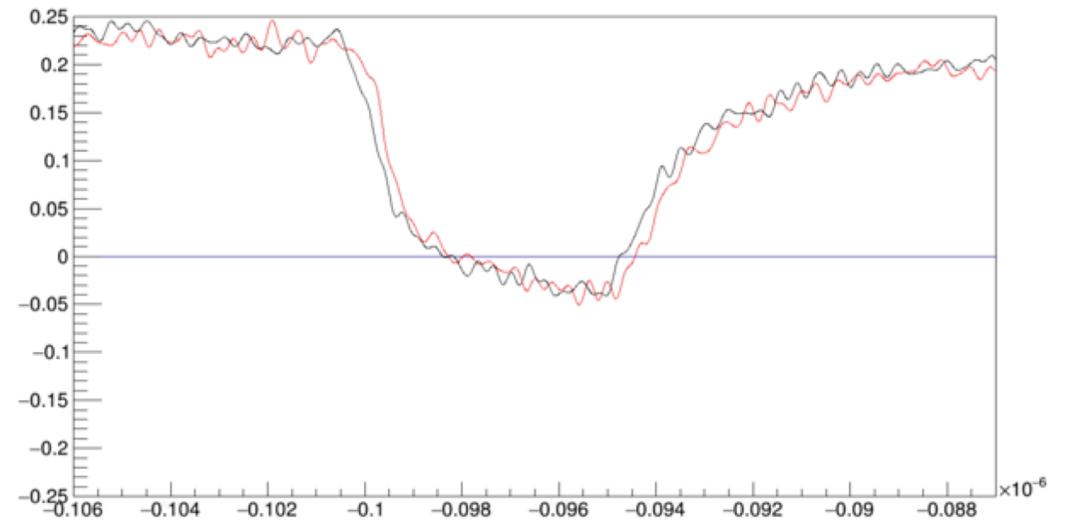


33a (Successful) – 35a (Failure)

Zoom Up



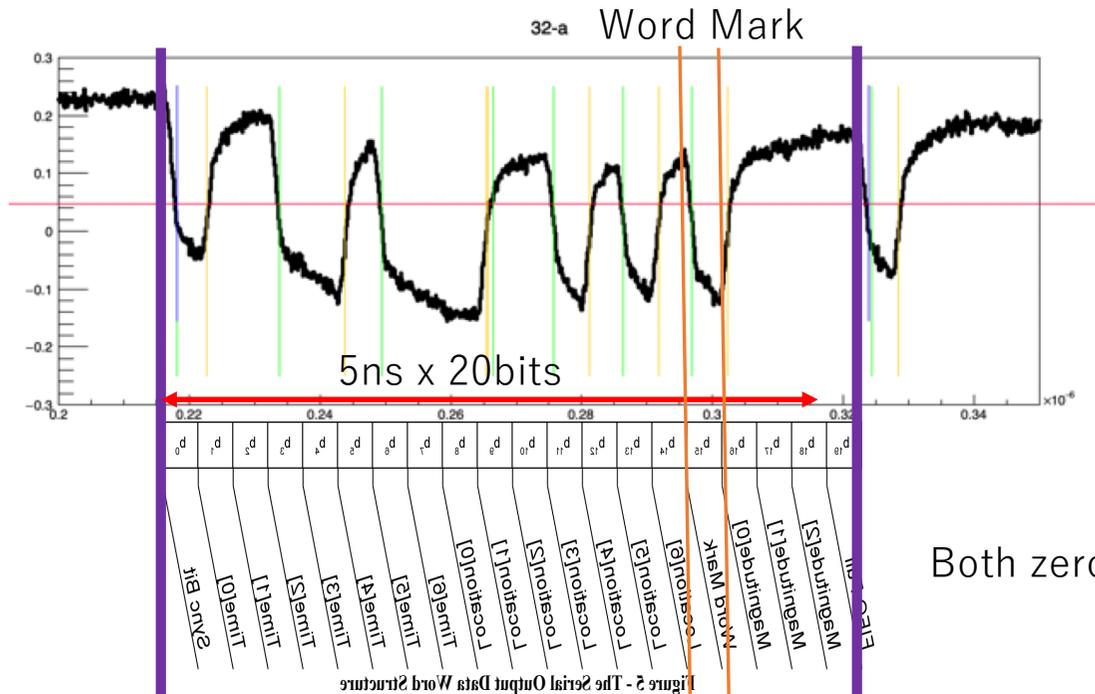
33a (Successful) – 35a (Failure)



33a (Successful) – 34b (Successful)

Data Word

Transmission Failure



Transmission Successful

