WaveForm Analysis

RKEN/RBRC

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on behalf of Bus Extender Team

Half Entry Issue Debugging Strategy

1. Data analysis of the observed waveform (μ, YA, Taskahi, IN)
    - Waveform comparison
    - Eye diagram
2. Individual Chip Reset（Genki, Yasuyuki）
    - Keep resetting only the FPHX chip causes the half entry. Rests are to be remain un-reset between Runs.
3. Phase Follower Tuning at ROC-FPGA
    - FPGA code was developed in Taiwan and available for testing
    - Prepare ROC board for this testing. 3V regulator is to be installed to the ROC-7. This board is to be dedicated for this study. There is potential risk we cannot re-install the original code to the ROC data FPGA.
    - In the meantime, wait for #1 analysis

Half Entry Debugging (5/26 ~ 28)

Inviting Takashi Kondo from Tokyo Industrial Research Center for monitoring data transmission.

3GHz Oscilloscope

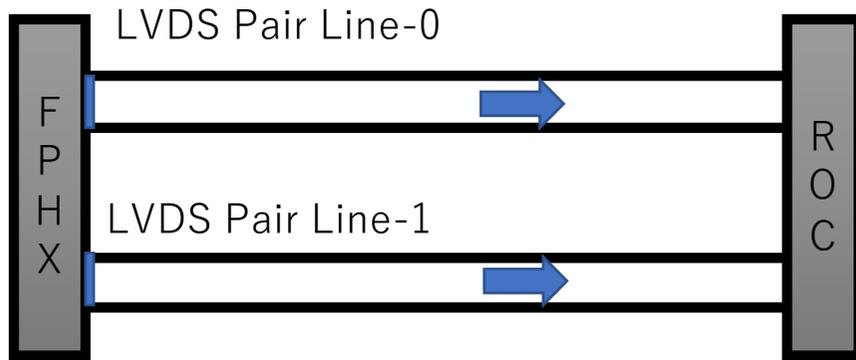Takashi Kondo

Active Probe

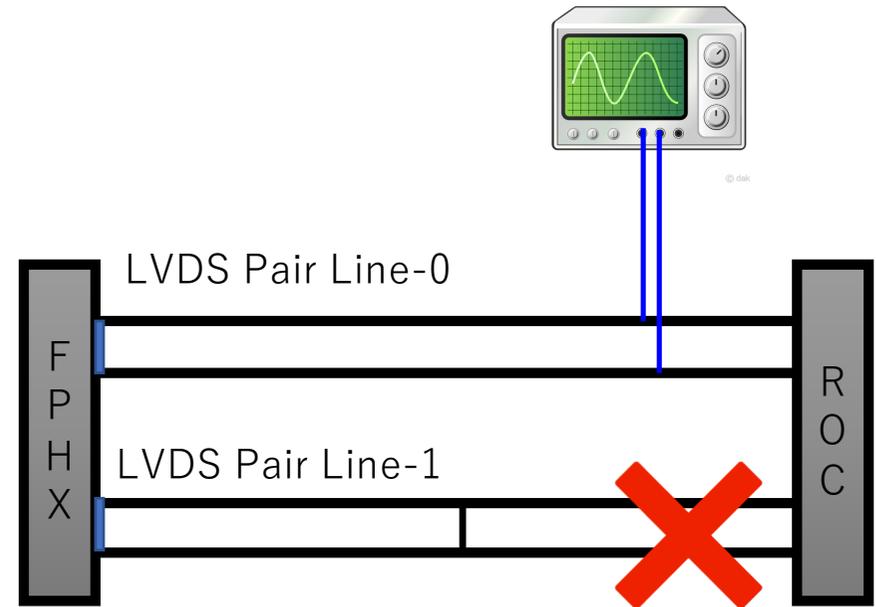The results presenting today are the observation at the back of the ROC board

Possible Scenarios of Transmission Failure

1. Missing Sync Bit & Word Mark
2. Insufficient Signal Amplitude
3. Screwed up Phase (Timing)

Measurement Method

LVDS Pair Line-0

LVDS Pair Line-1

FPHX Data Transmission Concept

FPHX

ROC

LVDS Pair Line-0

LVDS Pair Line-1

FPHX

ROC

Disable opponent LVDS Pair line so that we know the data monitoring are accepted by the ROC

Run Log

Courtesy of μ

Probe Point @ ROC Backplane

CHIP-ID	Line	Transmission	Scope Measurement #		
			Golden	Silver	Bronze
4	0	Success			36
	1	Success			37
7	0	Fail	**32**		
	1	Success	**34**		
8	0	Success	**33A**	33B,C	
	1	Fail	**35**		
19	0	Fail	**38**		
	1	Success		39	

Golden : Perfect control of failure/successful transmission lines.
Silver   : Transmission successful, but data look ugly (ザビザビ).
Bronze : Alternative line was not shorted.

Typical Calibration Results

Probe Point @ ROC Backplane

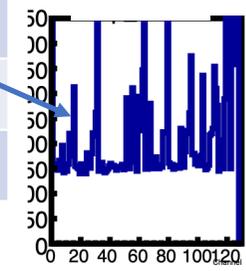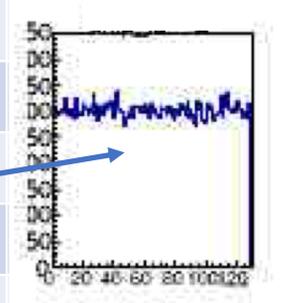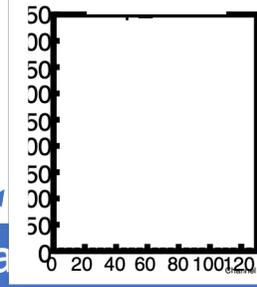| CHIP-ID	Line	Transmission	Scope Mea...		
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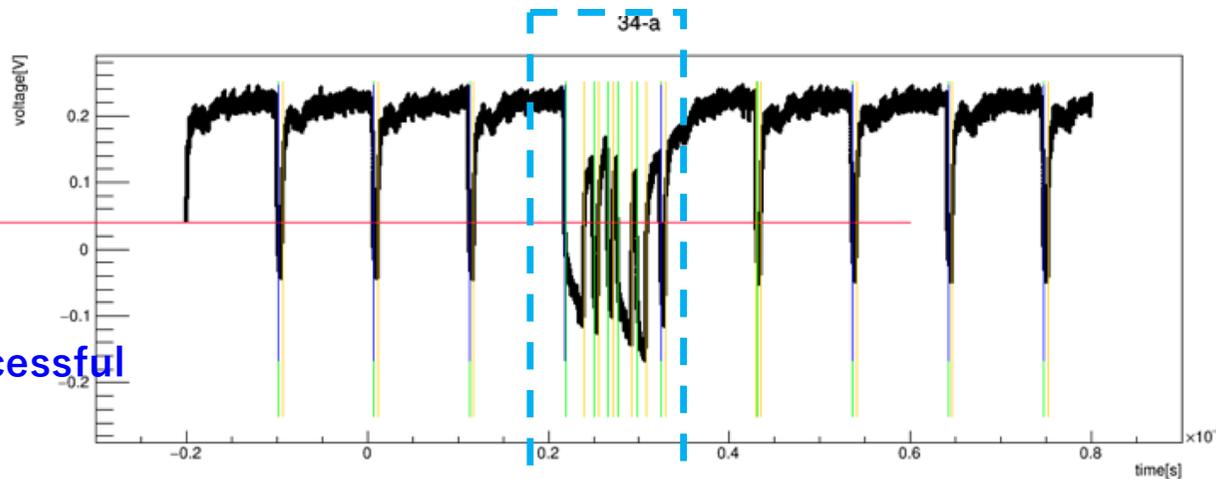Bronze   : Alternative line was not shorted.

Chip-7 Waveform Comparison (Wide)

Transmission Failure
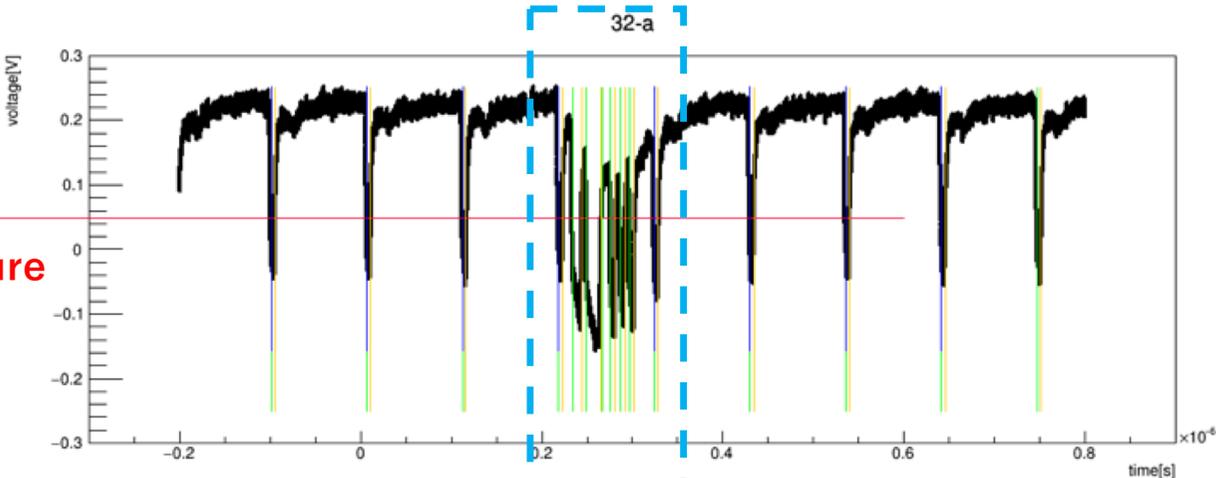
Transmission Successful

Courtesy of Takashi

Zoom in next page
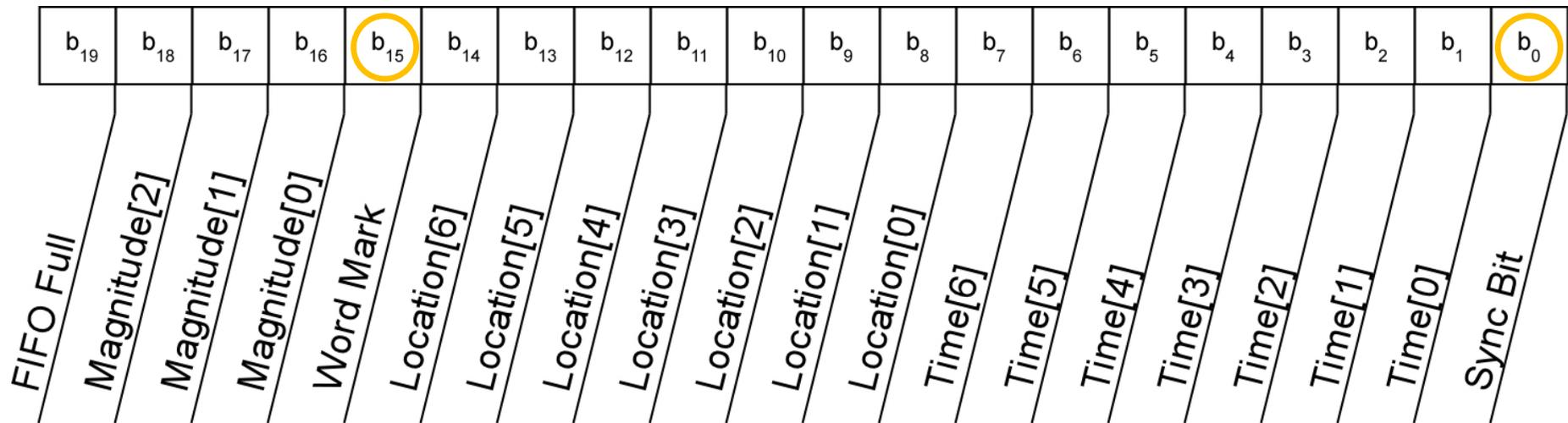
FPHX Data Bit Structure

Figure 5 - The Serial Output Data Word Structure

Serial Words

Each of the FPhx's two serial output words will drive a continuous stream of 20-bit words. Each word will be 1 sync bit followed by 19 data bits. If all 19 data bits are zeros, then that 20-bit word is a Sync Word placed in the data stream to enable the data acquisition hardware to align itself to the data flow from the FPhx chip. If the 19 data bits are NOT all zeroes then that 20-bit word is a Data Word and it contains information on a hit strip. The data is organized as follows:
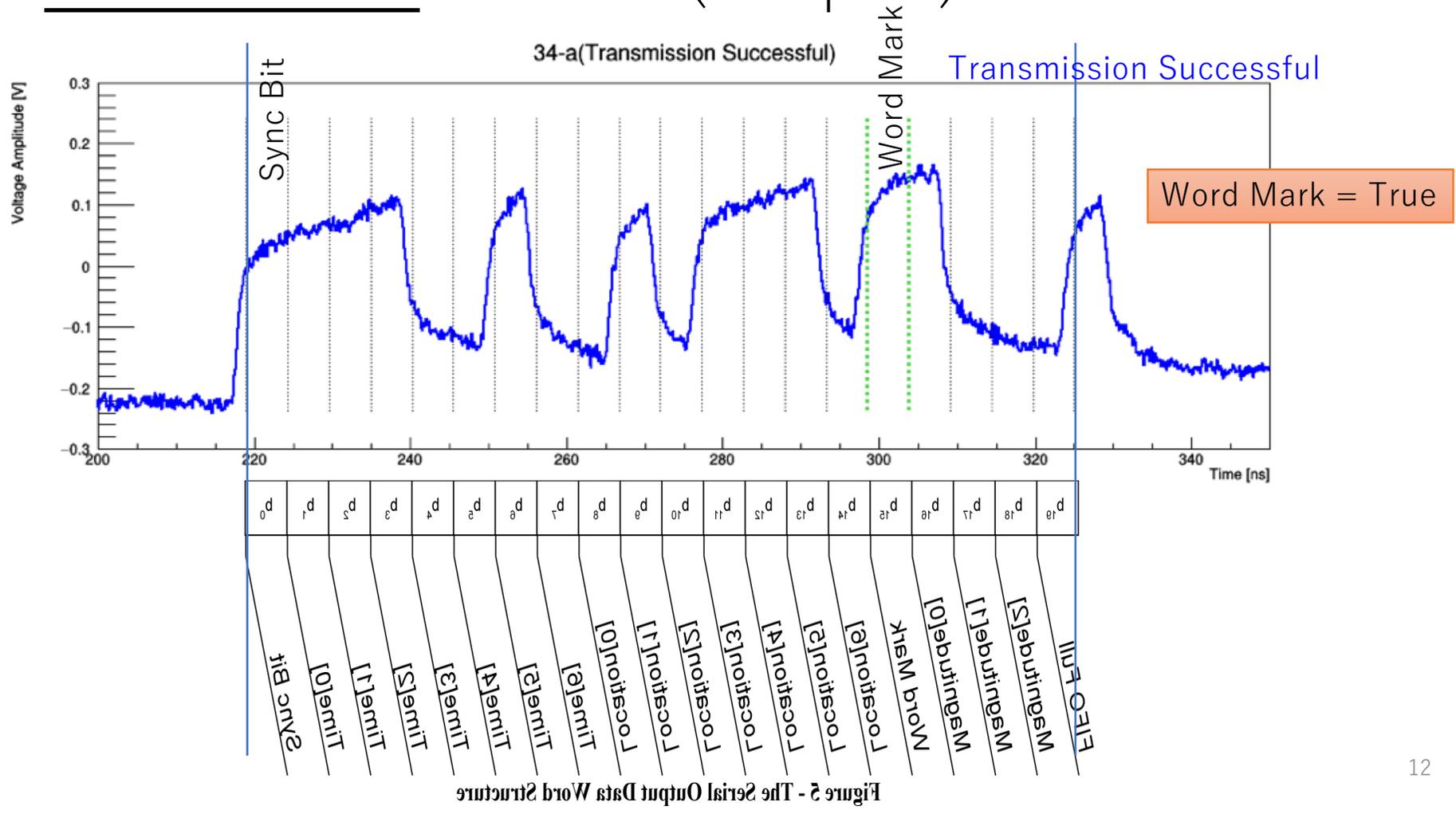
1. Word

Transmission Successful
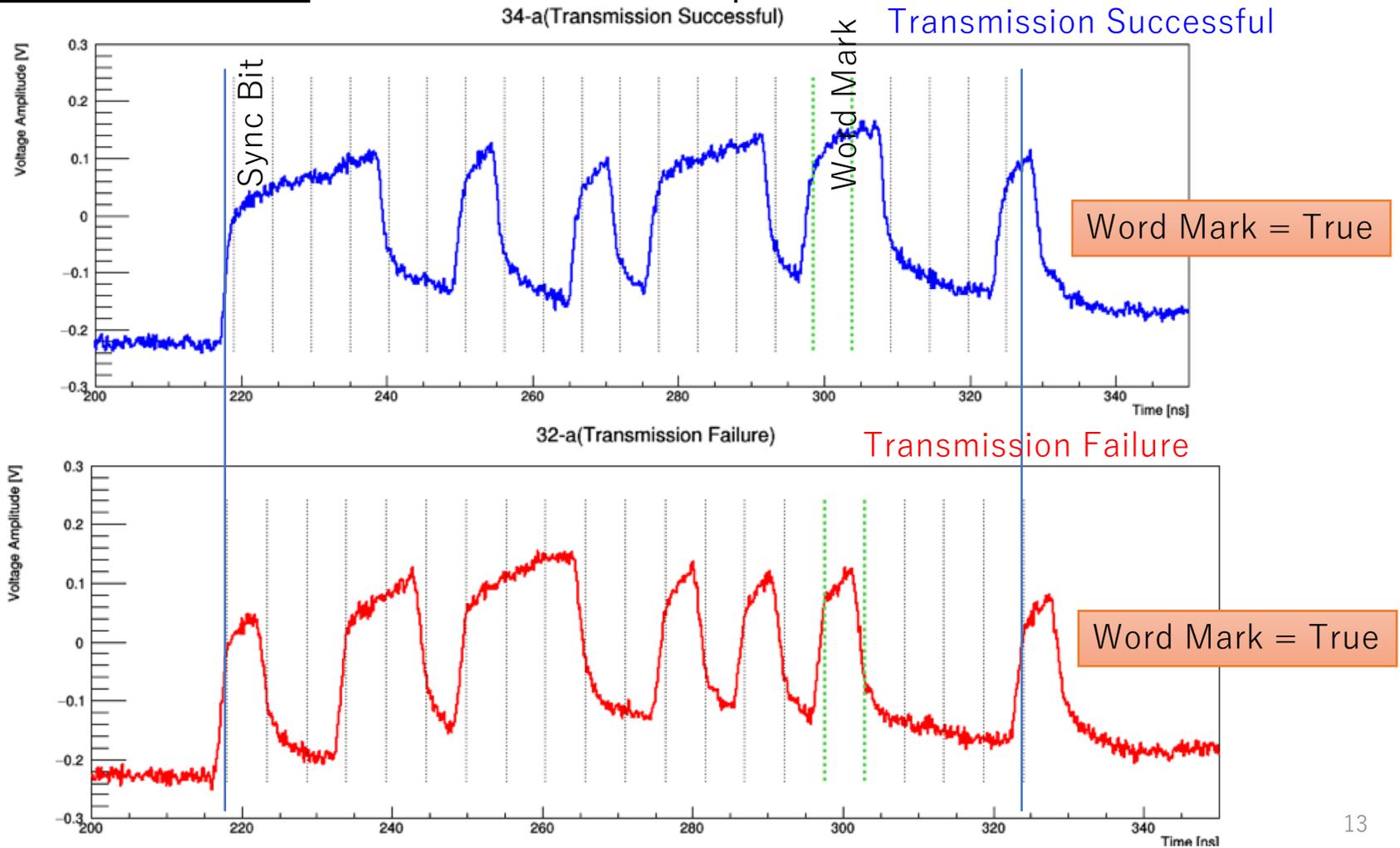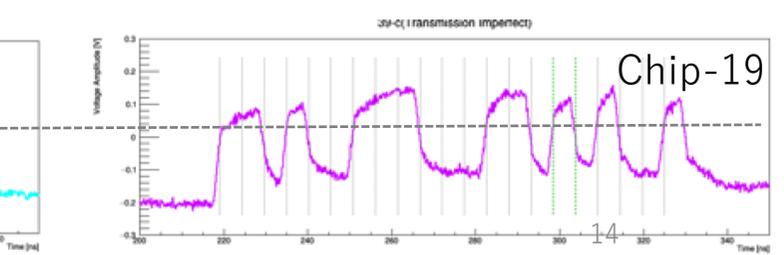
Word Mark = True

Sync Bit
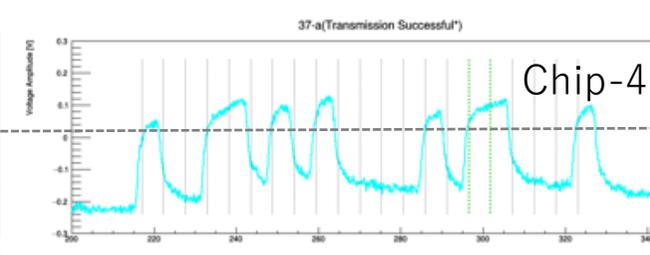
Word Mark

Figure 5 - The Serial Output Data Word Structure

1. <u>Word Mark</u> Check (Chip-7)

Transmission Successful

Word Mark = True

Transmission Failure

Word Mark = True

1. <u>Word Mark</u> Check All
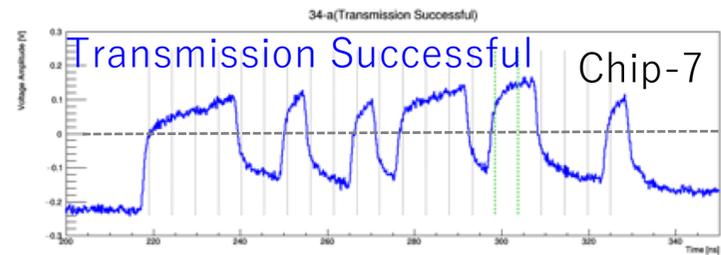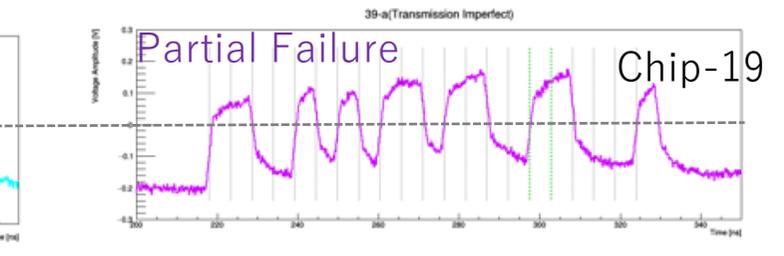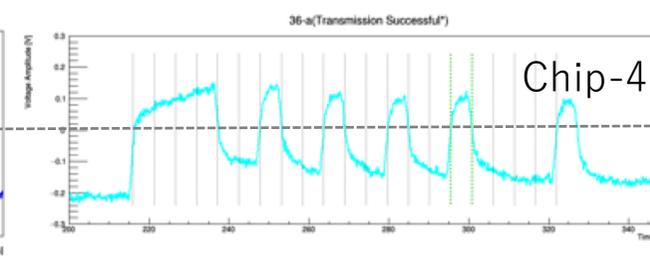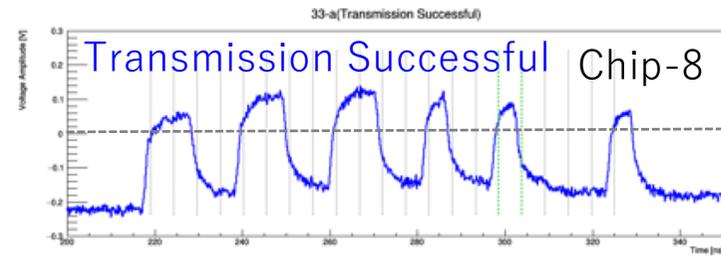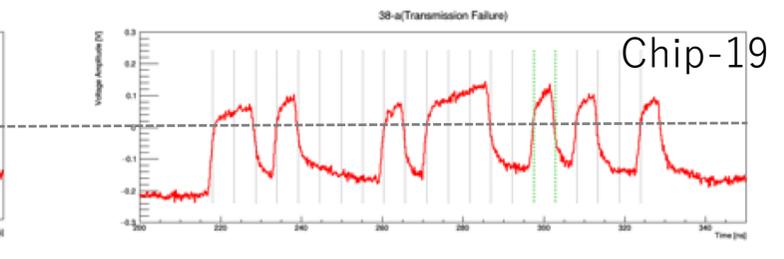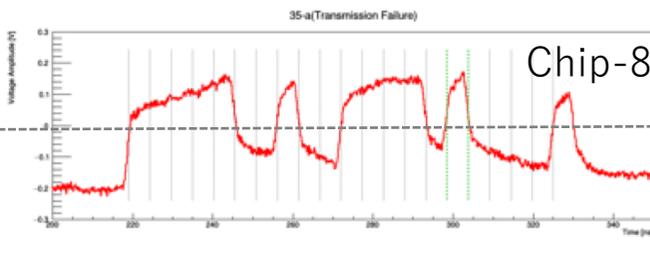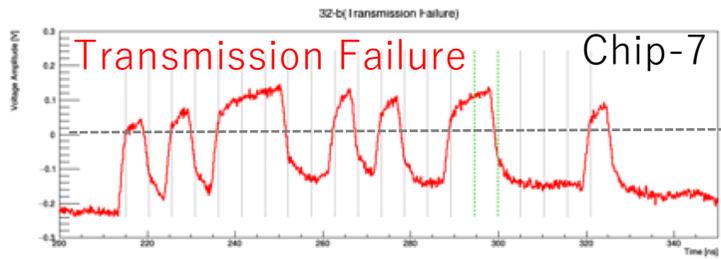
Chip-7 Waveform Comparison (Wide)

Transmission Failure
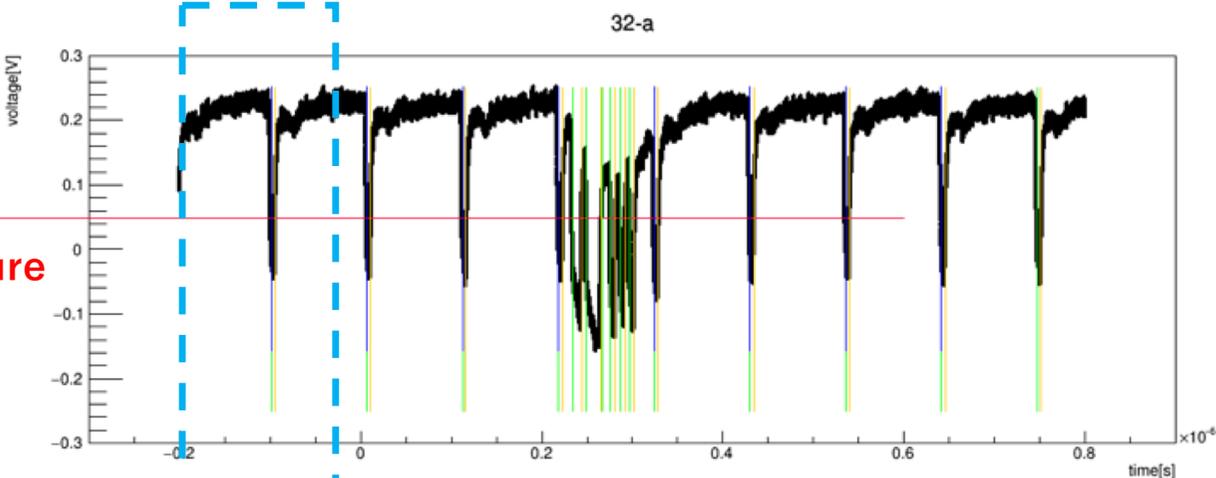
Transmission Successful
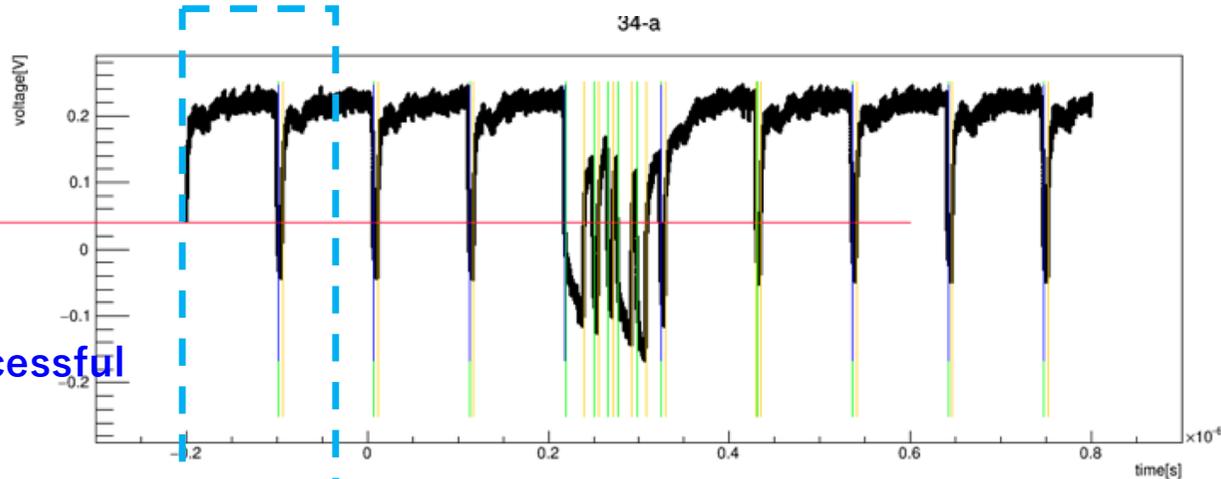
Courtesy of Takashi

Zoom in next page

2. Sync Bit Pulse Shape & Amplitude
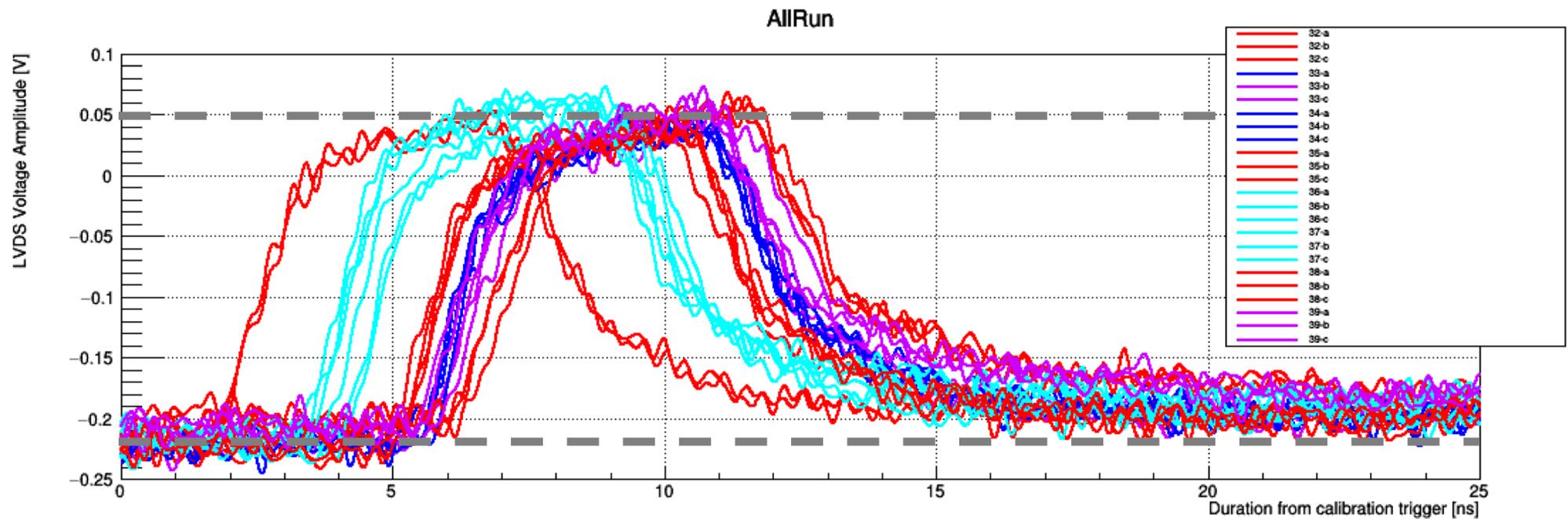
Did not observe obvious distortion of neither the pulse shape nor the amplitude between transmission successful and failure cases.

3. Relative Phase/Timing w.r.t. Trigger (Chip-8)
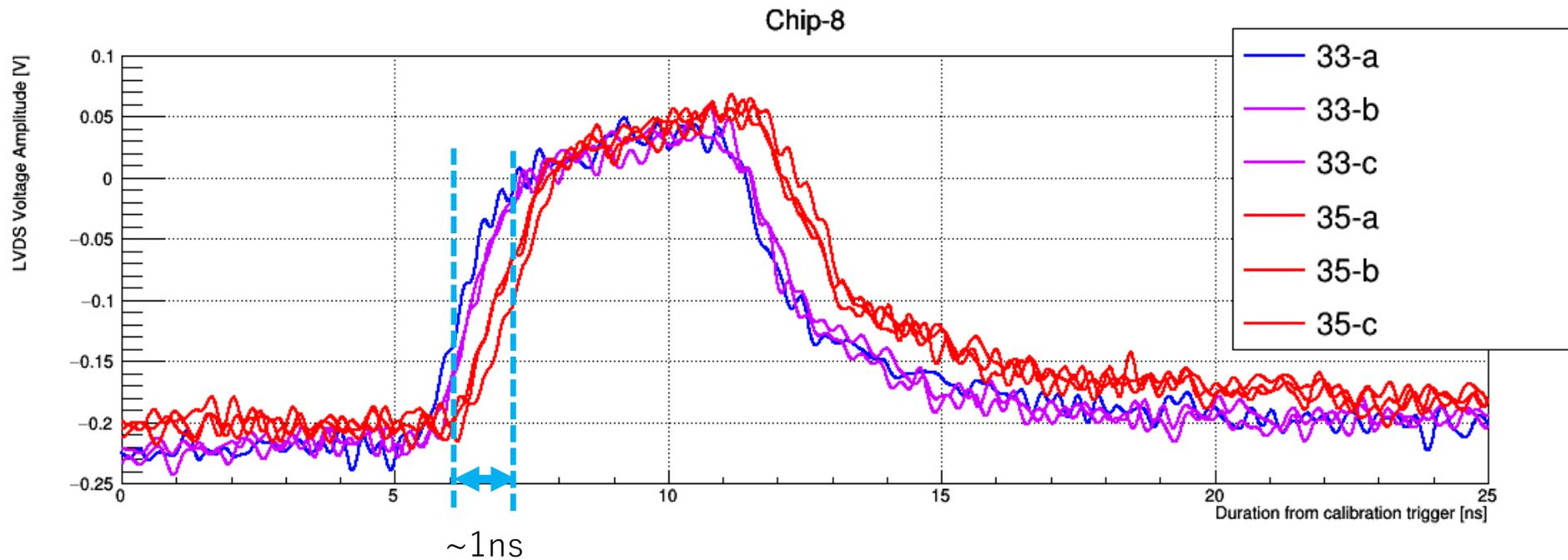
~1ns

The timing is about 1ns late in the transmission failure cases compared to successful cases

3. X-Check with Yasuyuki's Analysis (Chip-8)

Yasuyuki's Analysis

33a (Successful) – 35a (Failure)

~1ns
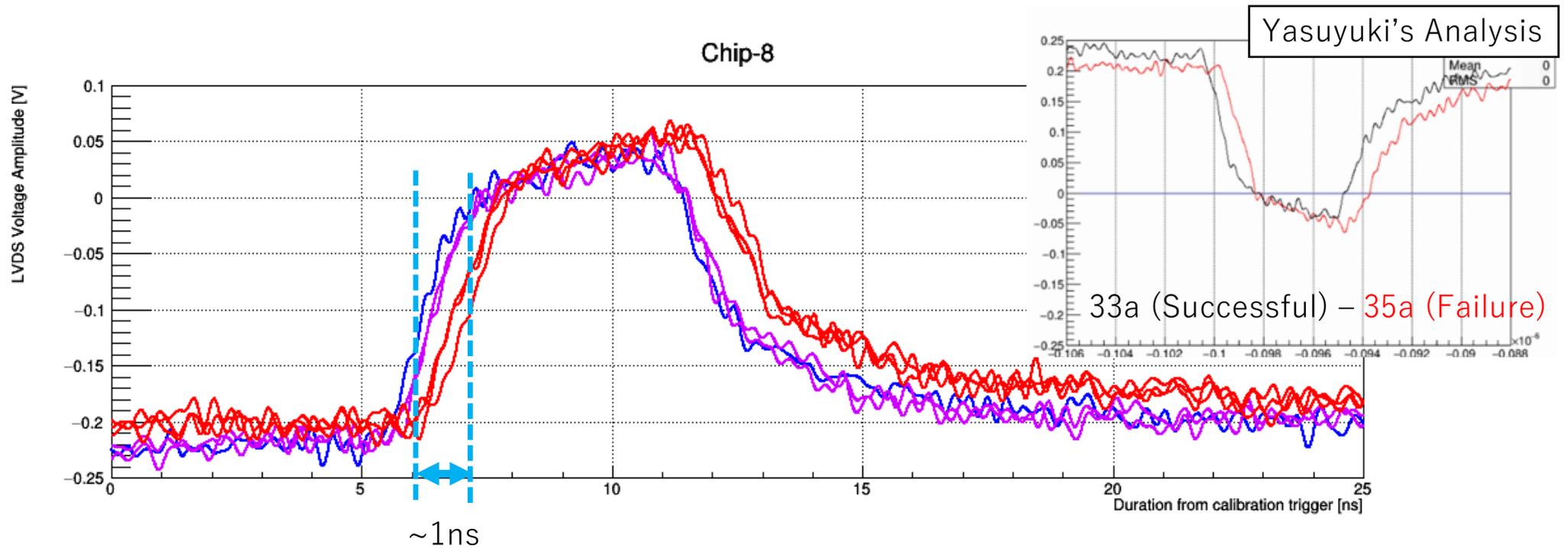
Consistent with Yasuyuki's Analysis

3. Relative Phase/Timing w.r.t. Trigger (Chip-8)
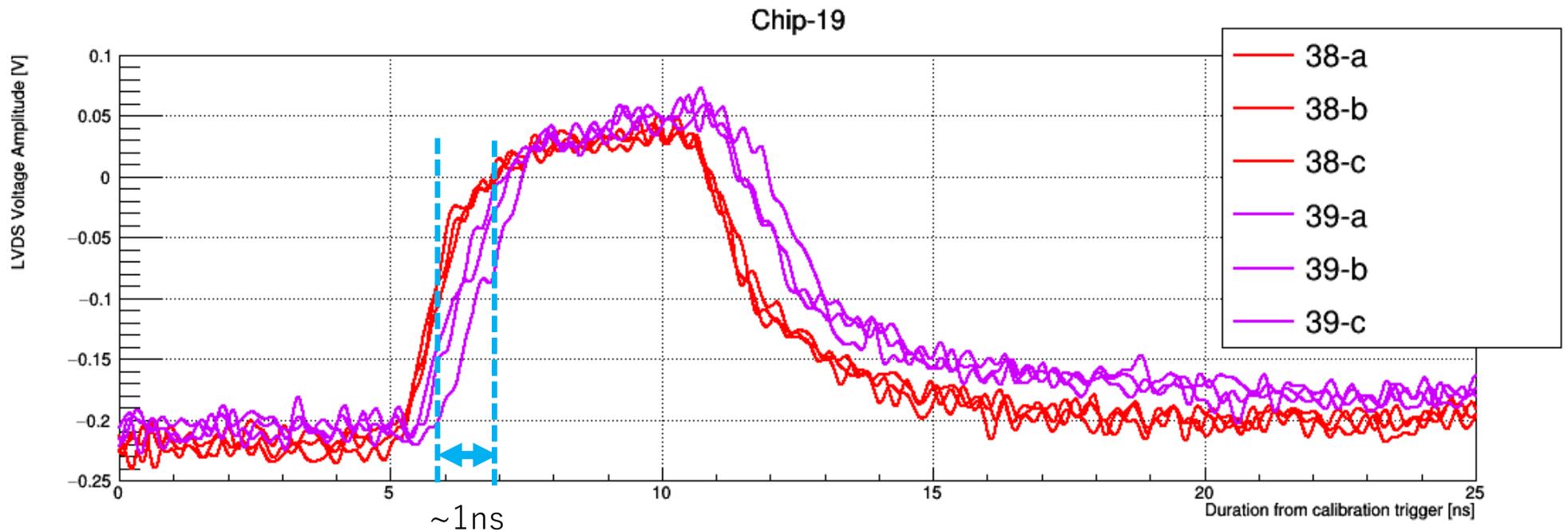
The timing is about 1ns late in the transmission partially failure cases compared to successful cases. Consistent with Chip-8 case.

3. Relative Phase/Timing w.r.t. Trigger (Chip-8)
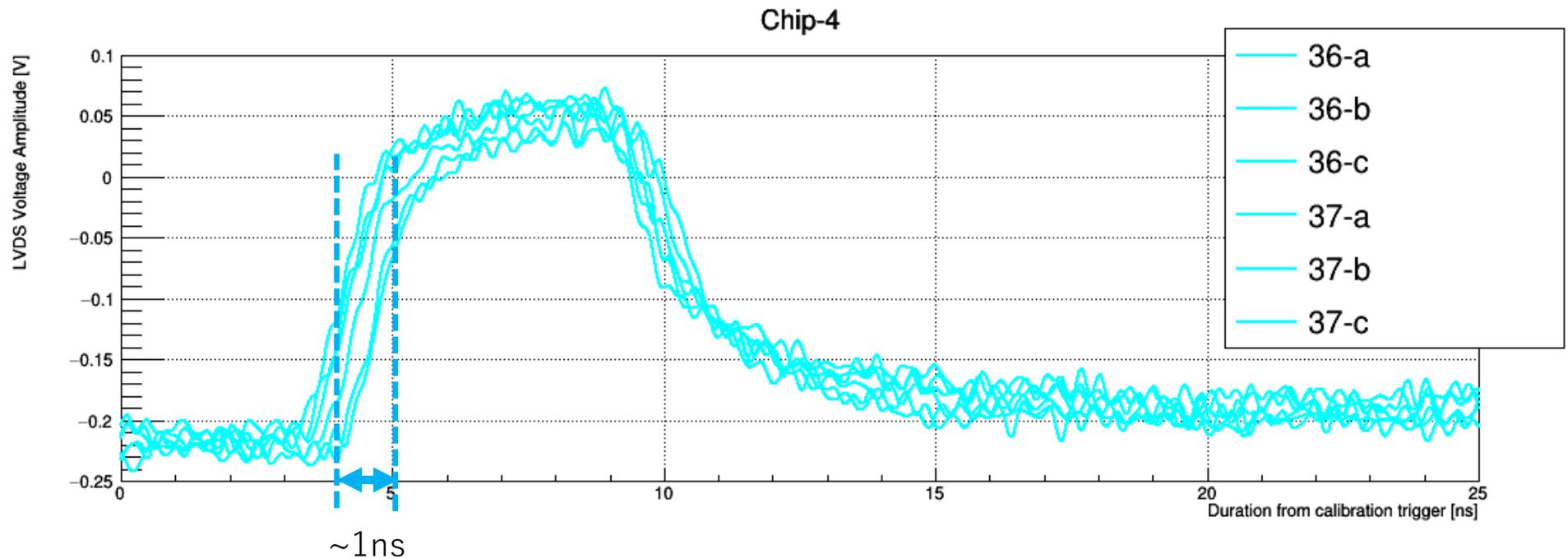
The timing seems to be spread <1ns. Unfortunately, the observation cannot lead to conclusive guidance because these pulse cannot be distinguished between from transmission successful or failure lines.

3.Relative Phase/Timing w.r.t. Trigger (Chip-7)
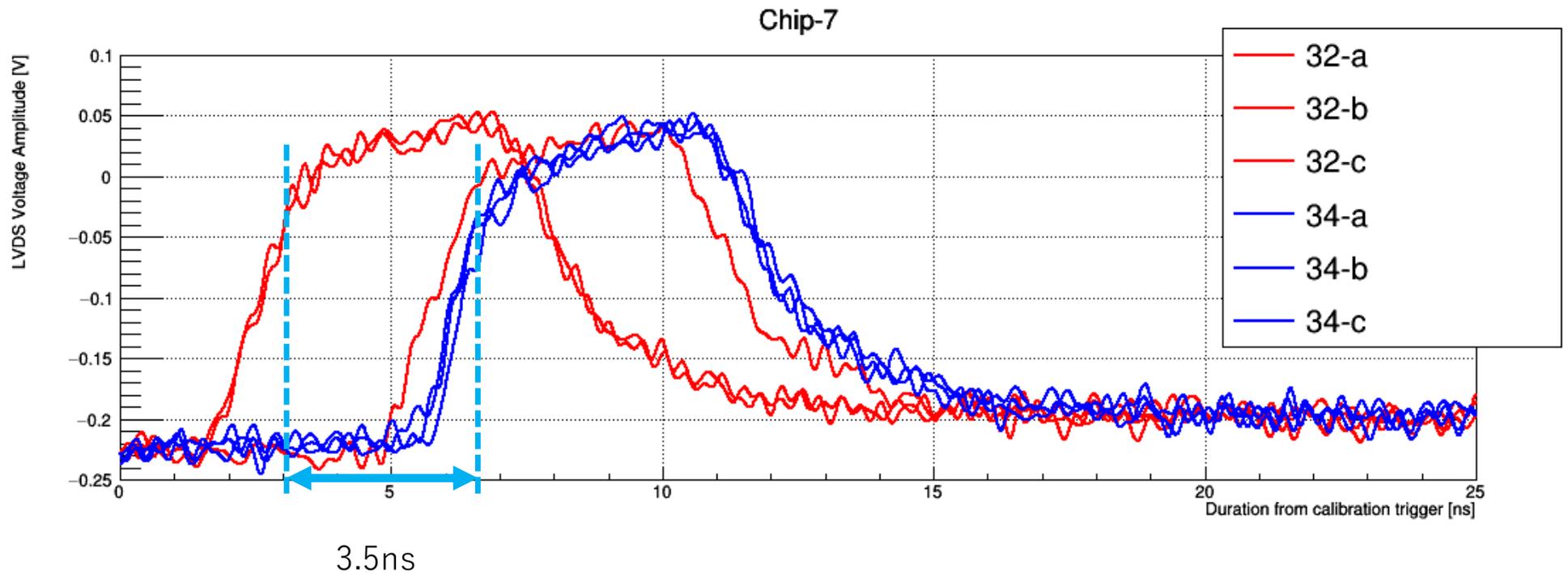
3.5ns

Observed as significant as 3.5ns timing difference between successful and failure transmission cases. However, there is one example (

3.Consistency Between Multi-Measurements

Chip-7
Run 32
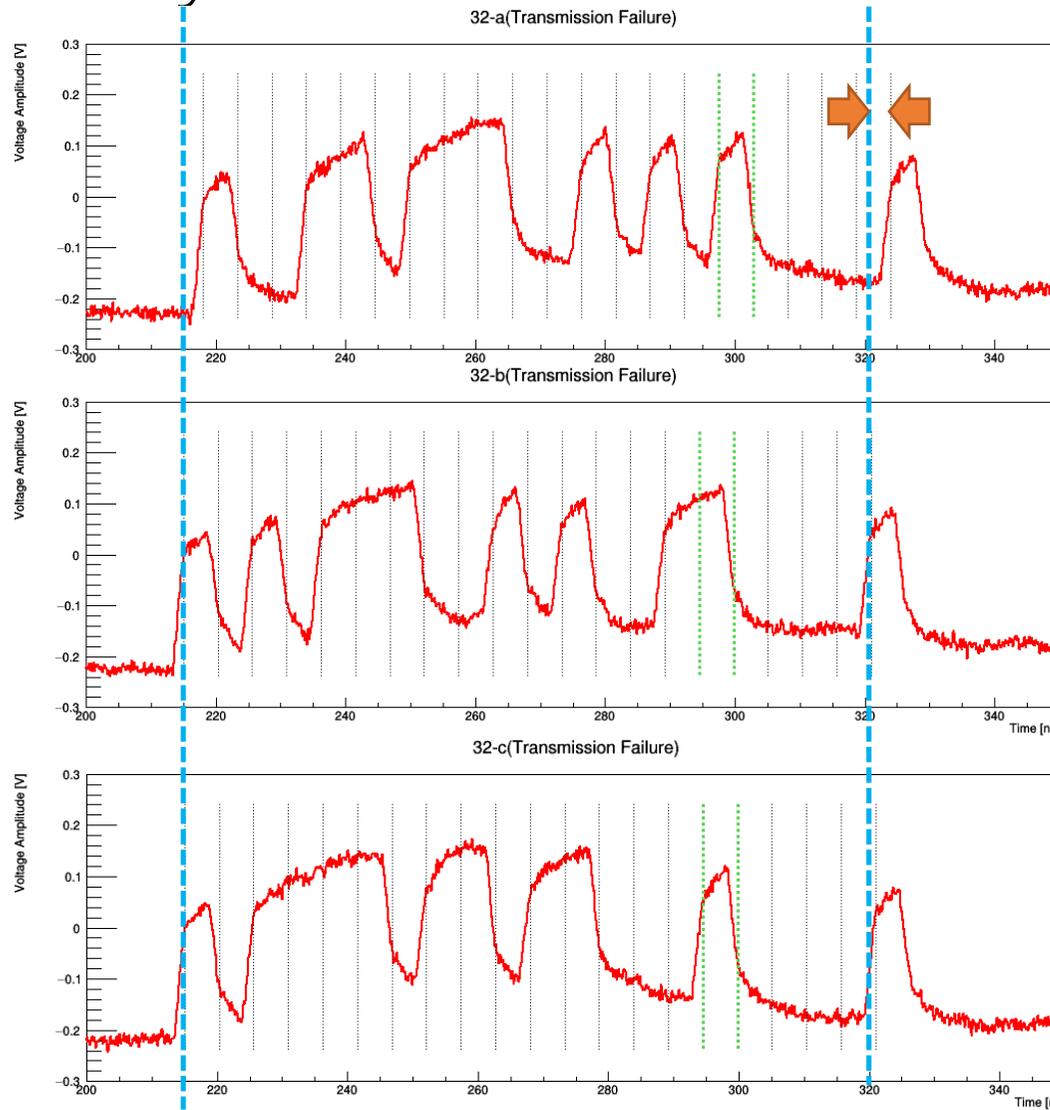
32-b & 32-c are consistent, but 32-a is off a bit

3.Consistency Between Multi-Measurements

Chip-7
Run 34

The timing seems to be quite consistent in all a,b,c measurements.

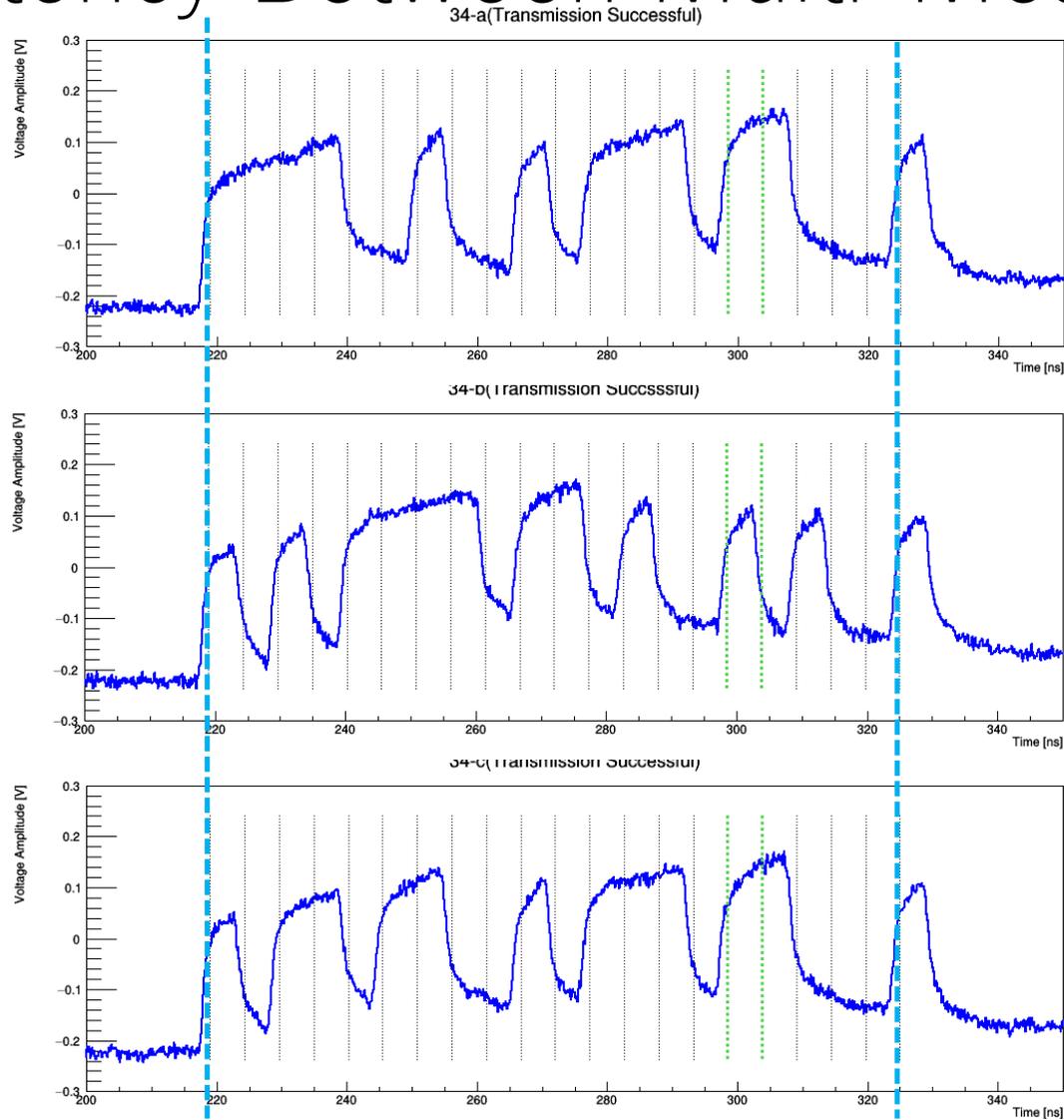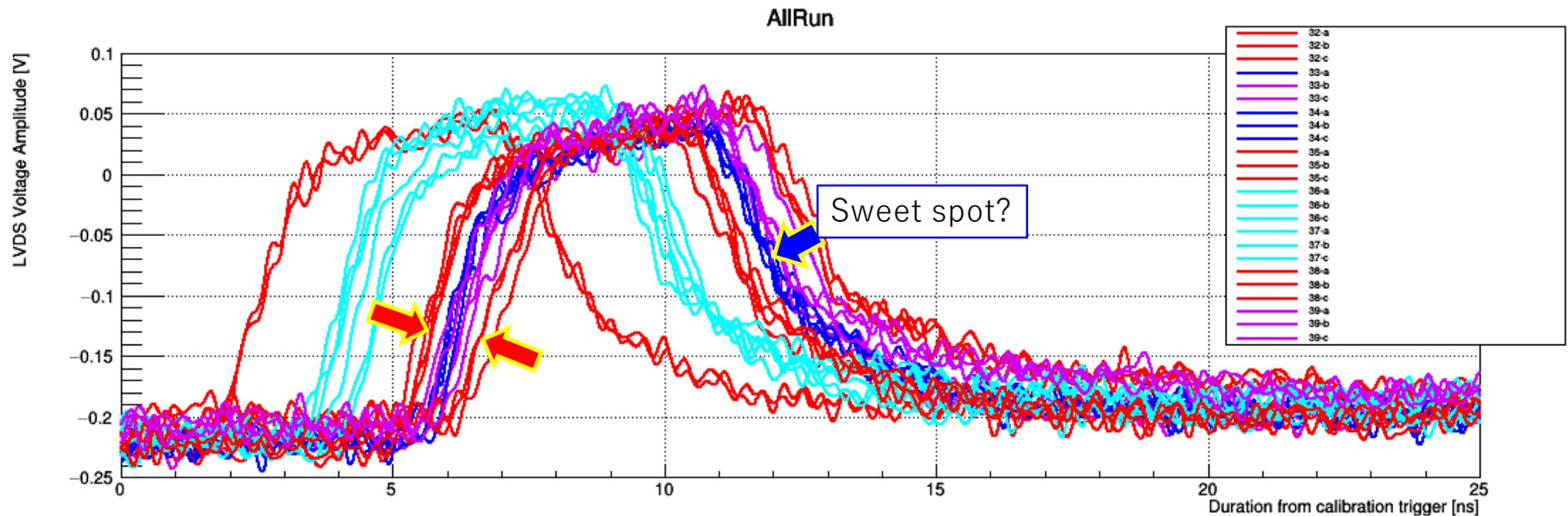# 3. Sync Bit Pulse Shape & Amplitude

- All successful transmission signals 33-a and 34-a,b,c appear in the similar timing. Is this the "sweet spot" of 0.5ns band? However, partially failure measurements 33-b,c and 39-a,b,c appear in similar timing.
- The timing of transmission failure appears both earlier and later sides of the "sweet spot" as indicated by red arrows.
- Hard to conclude that we can expect improvement by the phase tuning unless we can do flexible custom tune chip-by-chip and run-by-run basis which is not feasible.

24

Summary

1. Missing Sync Bit & Word Mark
   - Confirmed these bits are always true regardless of transmission successful or failure. No observation of particularly insufficient amplitude in these bits.

2. Insufficient Signal Amplitude
   - As far as sync bit pulses are inspected, there is no obvious degradation of pulse height or deformation in the transmission failure cases compared to successful cases.

3. Screwed up Phase (Timing)
   - Observed somewhat visible timing difference between transmission successful and failure cases. However a few cases doesn't necessarily follow the symptom. It is hard to draw consistent scenario to explain all phenomena at once.
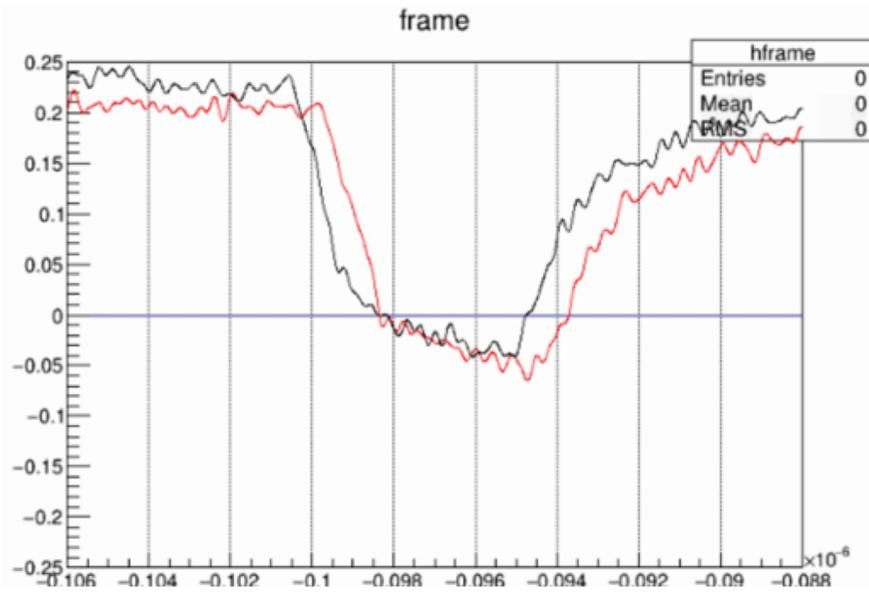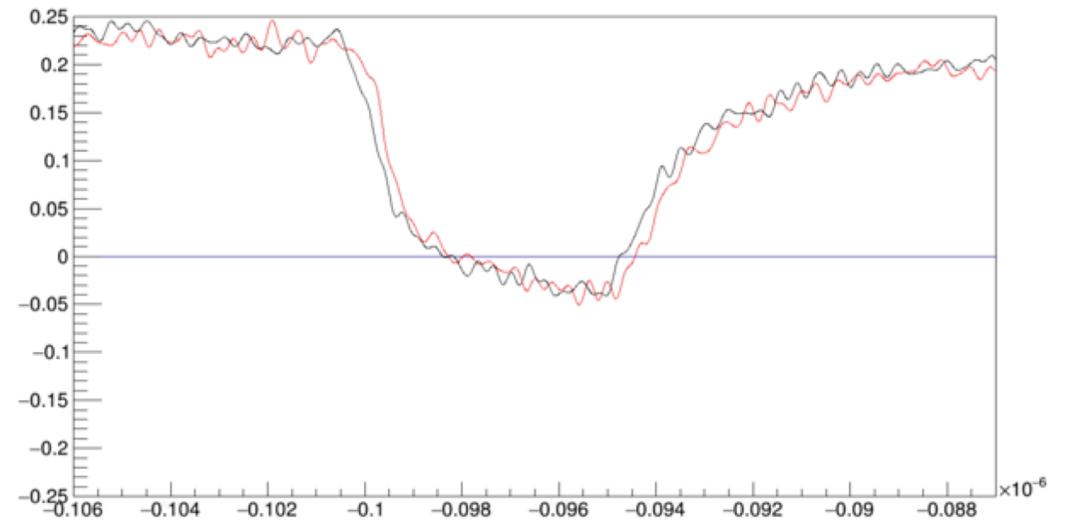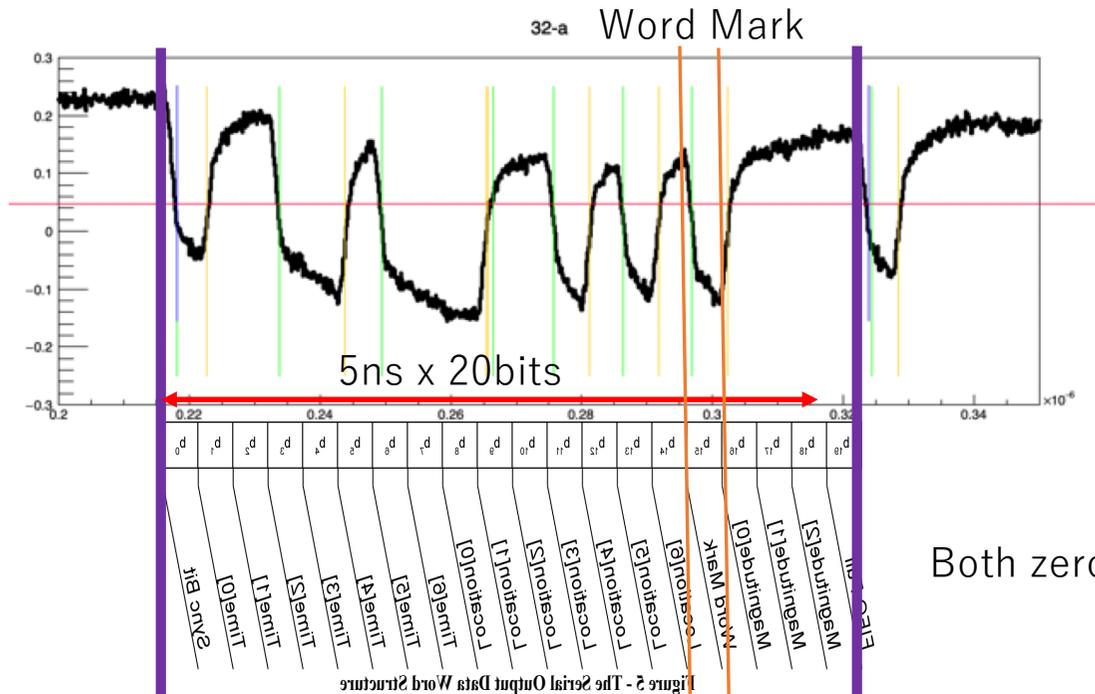
Backup

Zoom Up

33a (Successful) – 35a (Failure)

Yasuyuki's Analysis
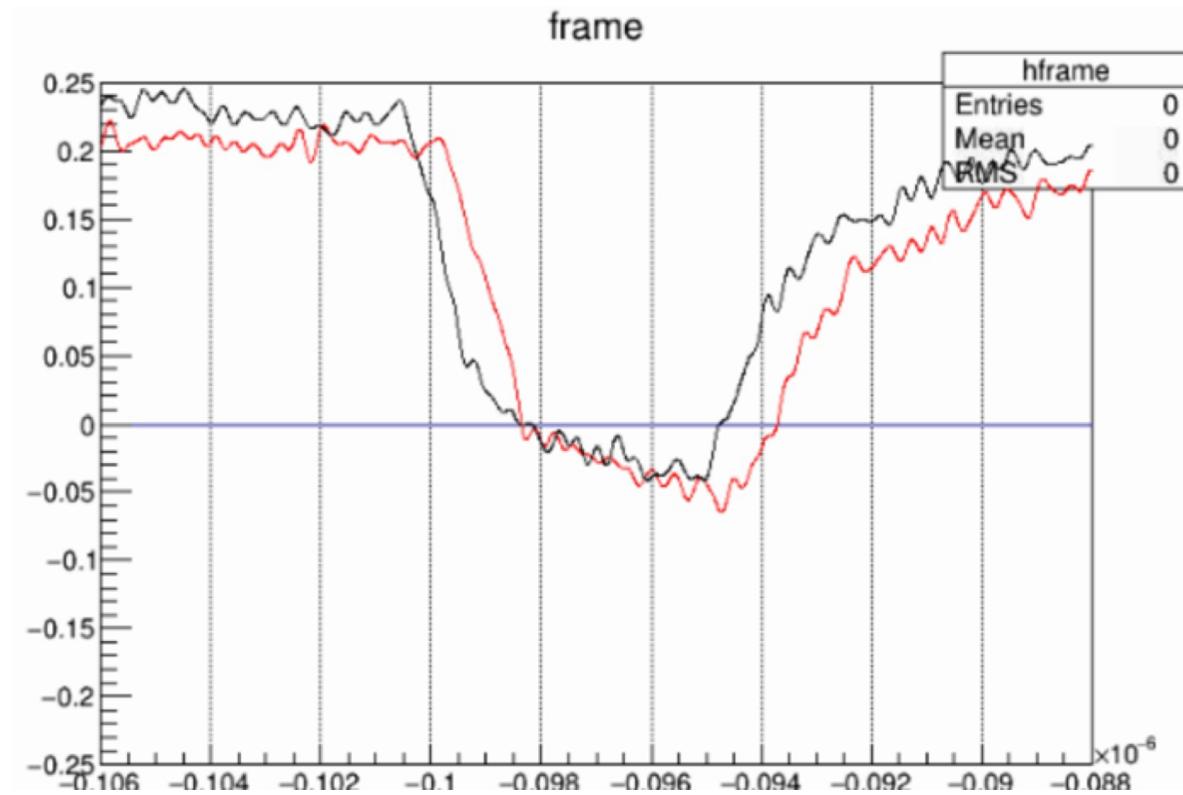
Zoom Up

33a (Successful) – 35a (Failure)

33a (Successful) – 34b (Successful)

Data Word

Transmission Failure

5ns x 20bits

Word Mark

Both zero?

Transmission Successful

Courtesy of Takashi