Activities at NWU : Half entry issue Source test

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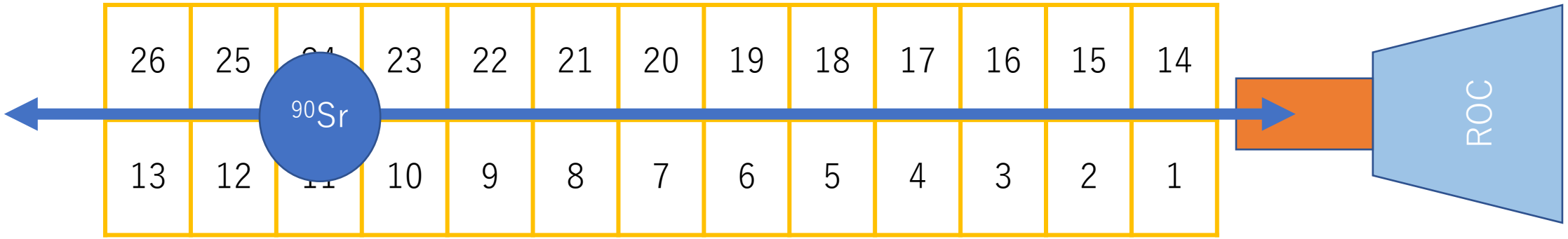
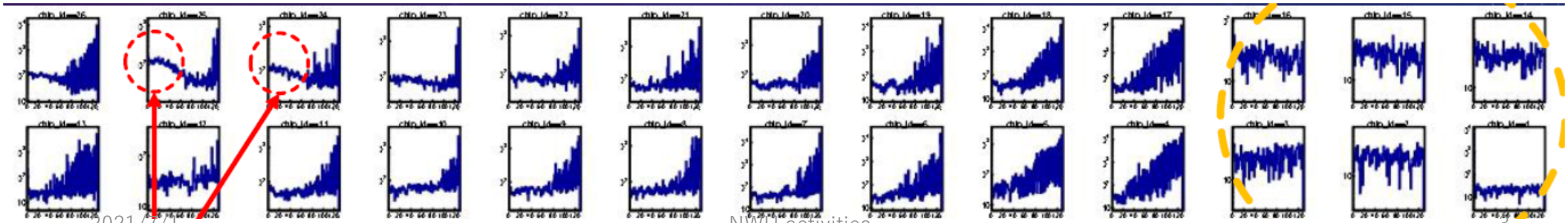
Introduction

- Source test status
- Half entry issue
- A concern related to slow control

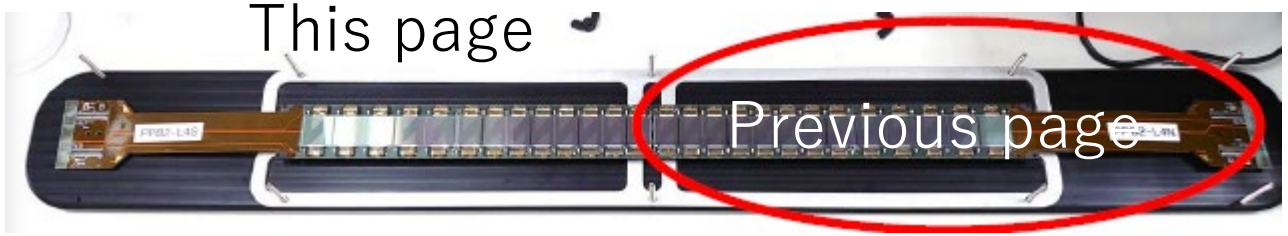
Source test

- Reported the source test issue last week
  - Flat shape in hit channel at Chip1-3 and 14-16 and some slope in other chips.
  - Trigger counter is placed (not used as trigger)

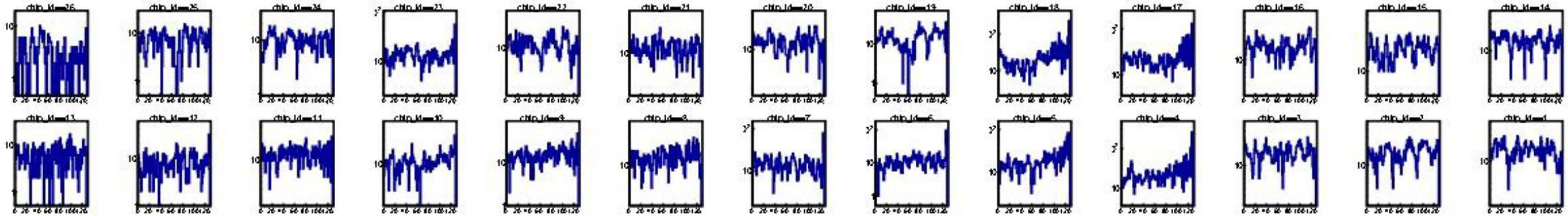




Source test 1

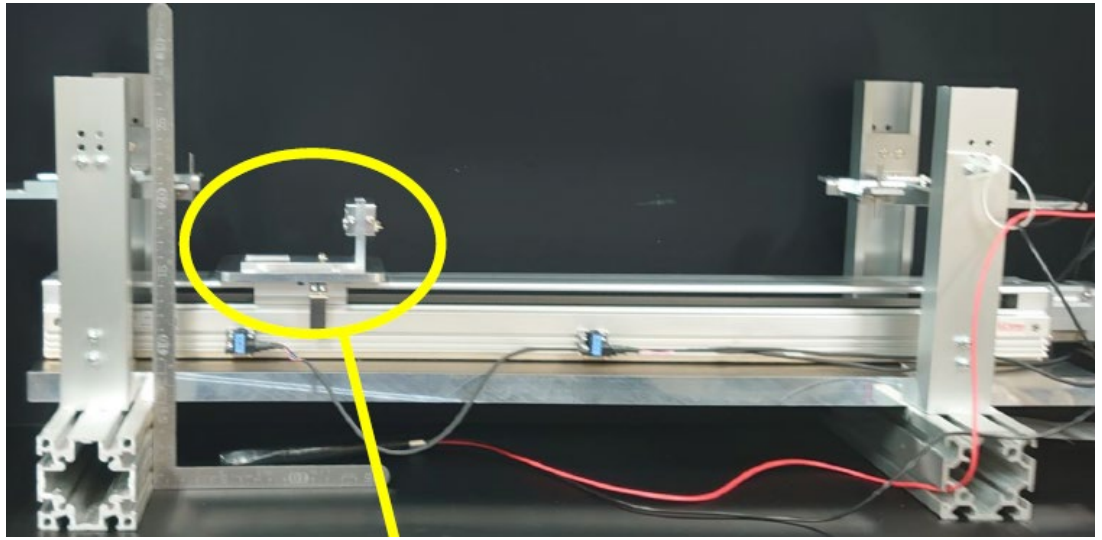


- To see if this is caused by this ladder, we tested other side.
- Setup slightly changed
  - Used the trigger counter
- Result : flat distribution for basically all chips
  - Some chip still have slopes

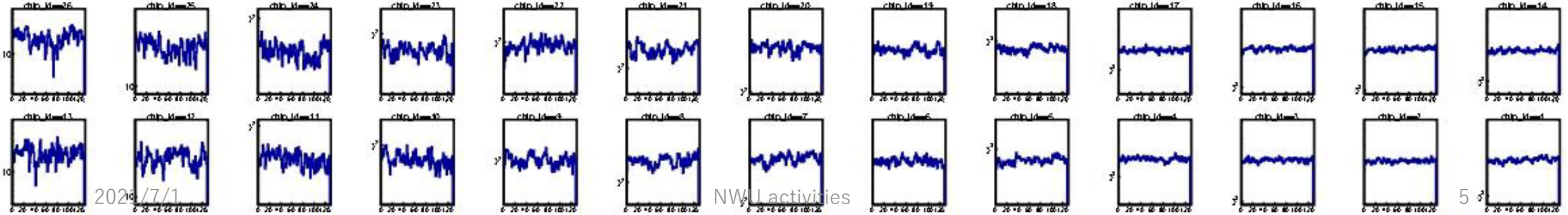


Source test 2

- To further investigate, we removed the counter holder on the movable stage

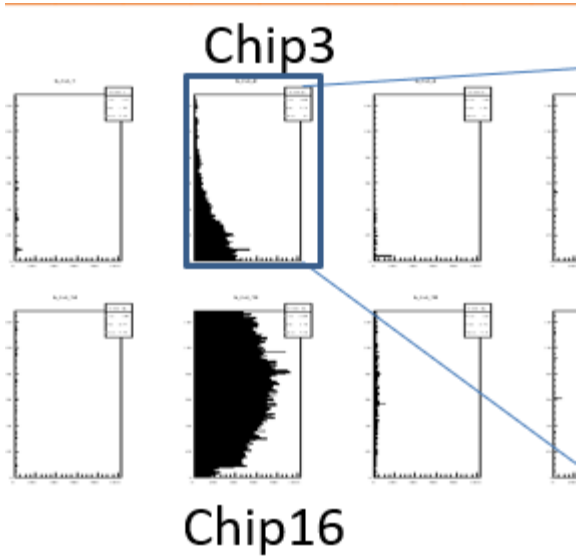


- Result :
  - All chips show flat.
- Indicated
  - the holder produced the noise hit, probably due to the unexpected radiations from the reflection or scattering by the holder

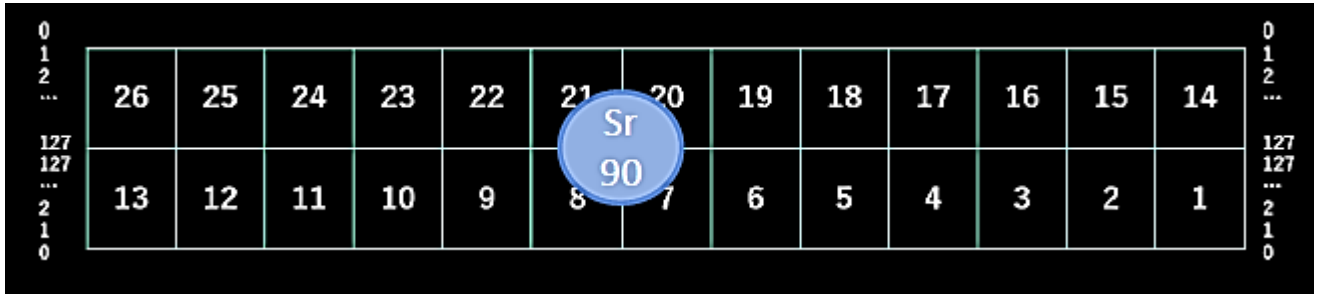


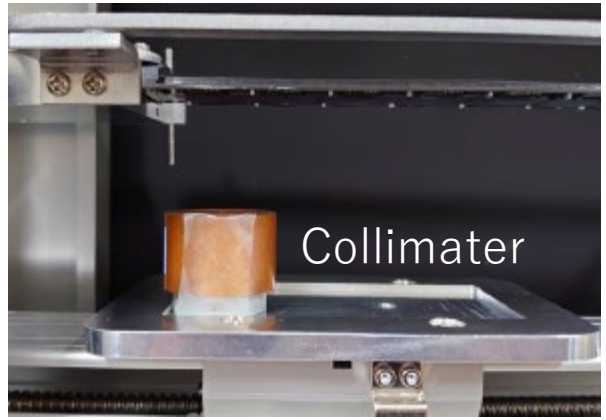
Source test 3

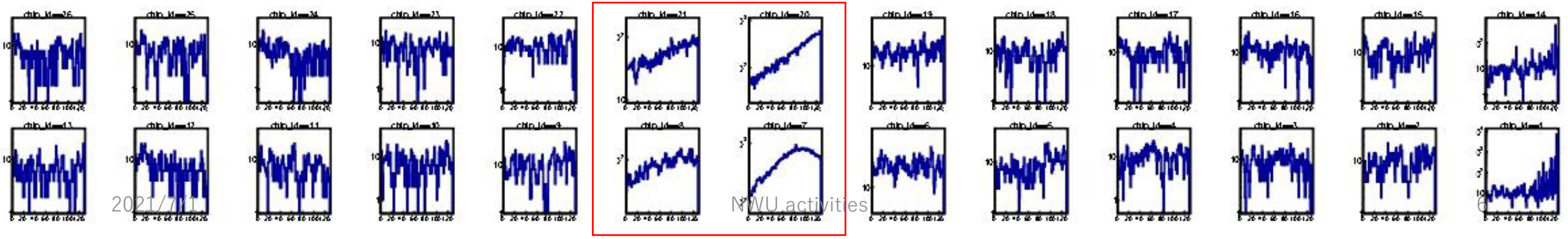
Source test from the previous half ladder



- Collimater is used to see how the distribution looks like.
- Hit distribution shows the peak structure.
  - beta ray is emitted to the smaller solid angle.
  - This is effectively same with the source get closer to the ladder

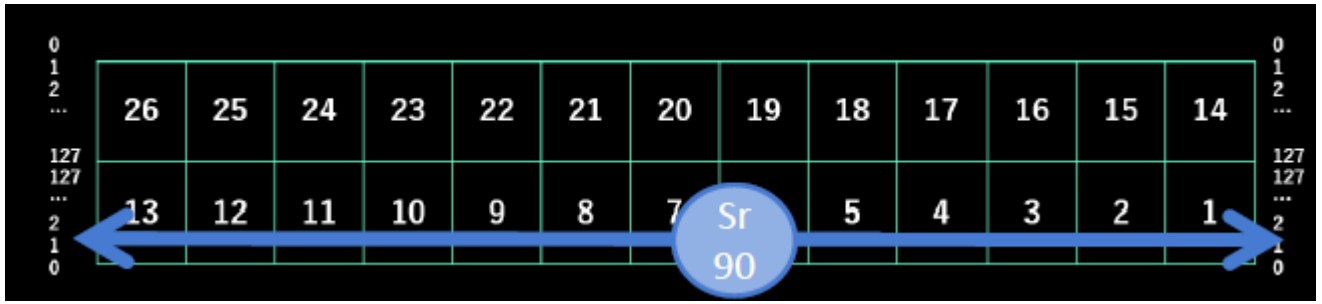


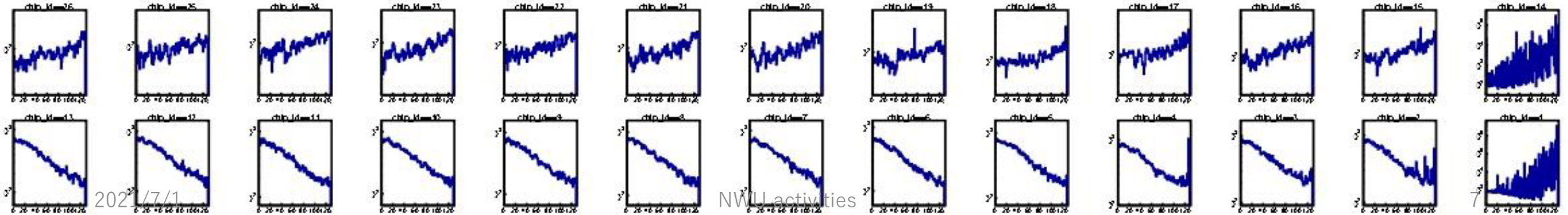




Source test 4

- Source test with moving stage.
  - Source is placed at Ch1 region
- All chips except chip1 and 14 shows the clear peak structures at ch-1.
  - More noise in ch 1 and 14.
  - Need more investigation. (issue on this ladder or other causes?)





Half entry issue

- Genki and RIKEN people tried to reproduce the half entry issue using the test bench at RIKEN. But it is not successful.
  - Half entry rate at RIKEN = ~2%, NWU = ~23%

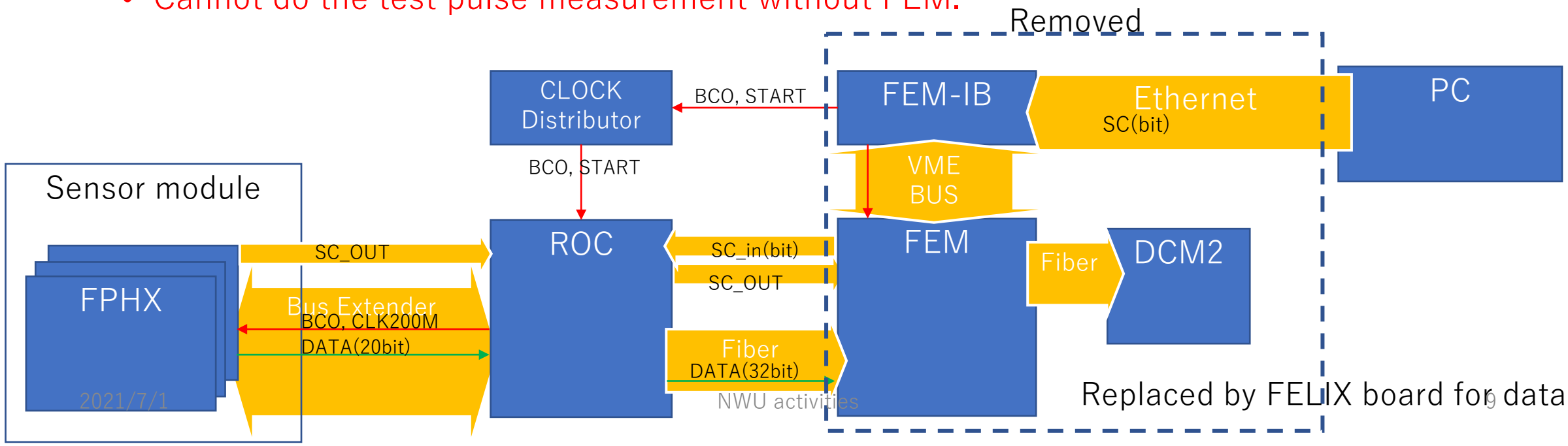
- RIKEN test bench could be better condition.
  - Check difference between them.
  - NWU bench follows their setup

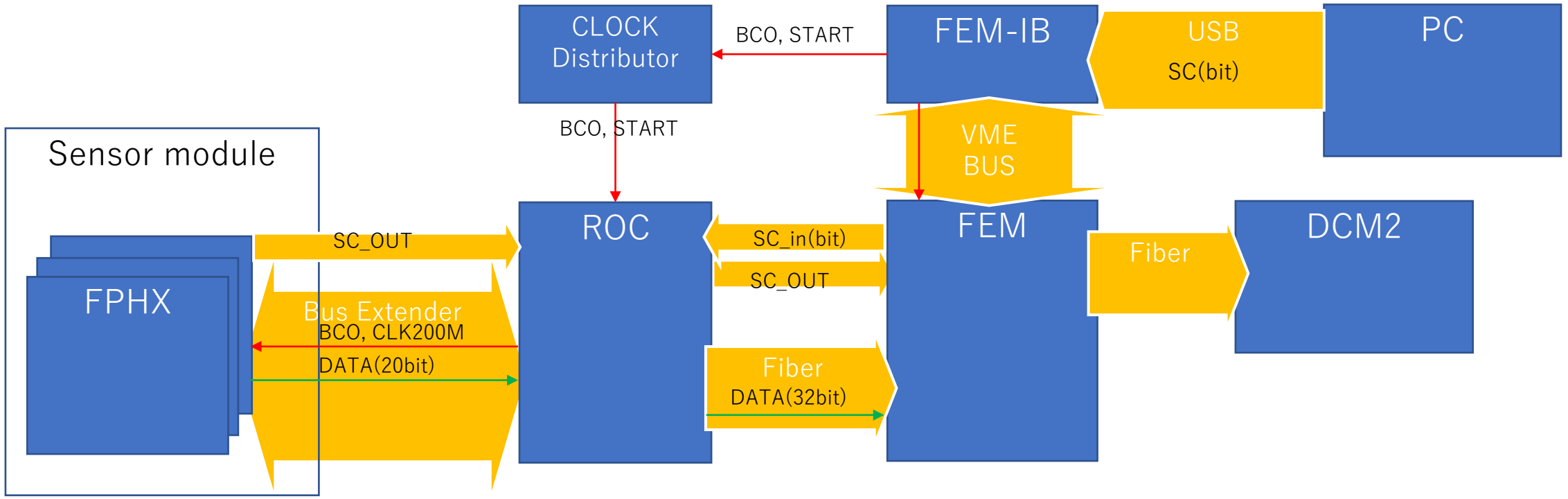
	NWU	RIKEN
Power supply	1 switching, all other series	all series
Supply voltage	6.3V for optics	6.6V
ROC type	Test bench	1008 ver. (FPGA code might be different)
Ladder	Full from BNL	Full from BNL

- As Yasuyuki's comment last week, we are preparing the bench to send "Synchronization" command multiple times

One concerns

- How we send the slow control commands using new DAQ system with FELIX?
  - We expect FEM-IB and FEM are not used for FELIX-DAQ system. If so, how we send the slow control command?
    - Can FELIX board be used for SC?
  - FEM, FEM-IB provide : Slow control, BCO clock, SC readback
    - Readback is also used to receive the amplitude information for the test pulse measurement.
    - Cannot do the test pulse measurement without FEM.




CLOCK
Distributor
BCO, START
FEM-IB
USB
SC(bit)
PC
BCO, START
VME
BUS
Sensor module
ROC
FEM
DCM2
SC_OUT
SC_in(bit)
Fiber
FPHX
SC_OUT
Bus Extender
BCO, CLK200M
DATA(20bit)
Fiber
DATA(32bit)