SMU R&Ds for HEP Detector Front-end Data Transmission

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Content

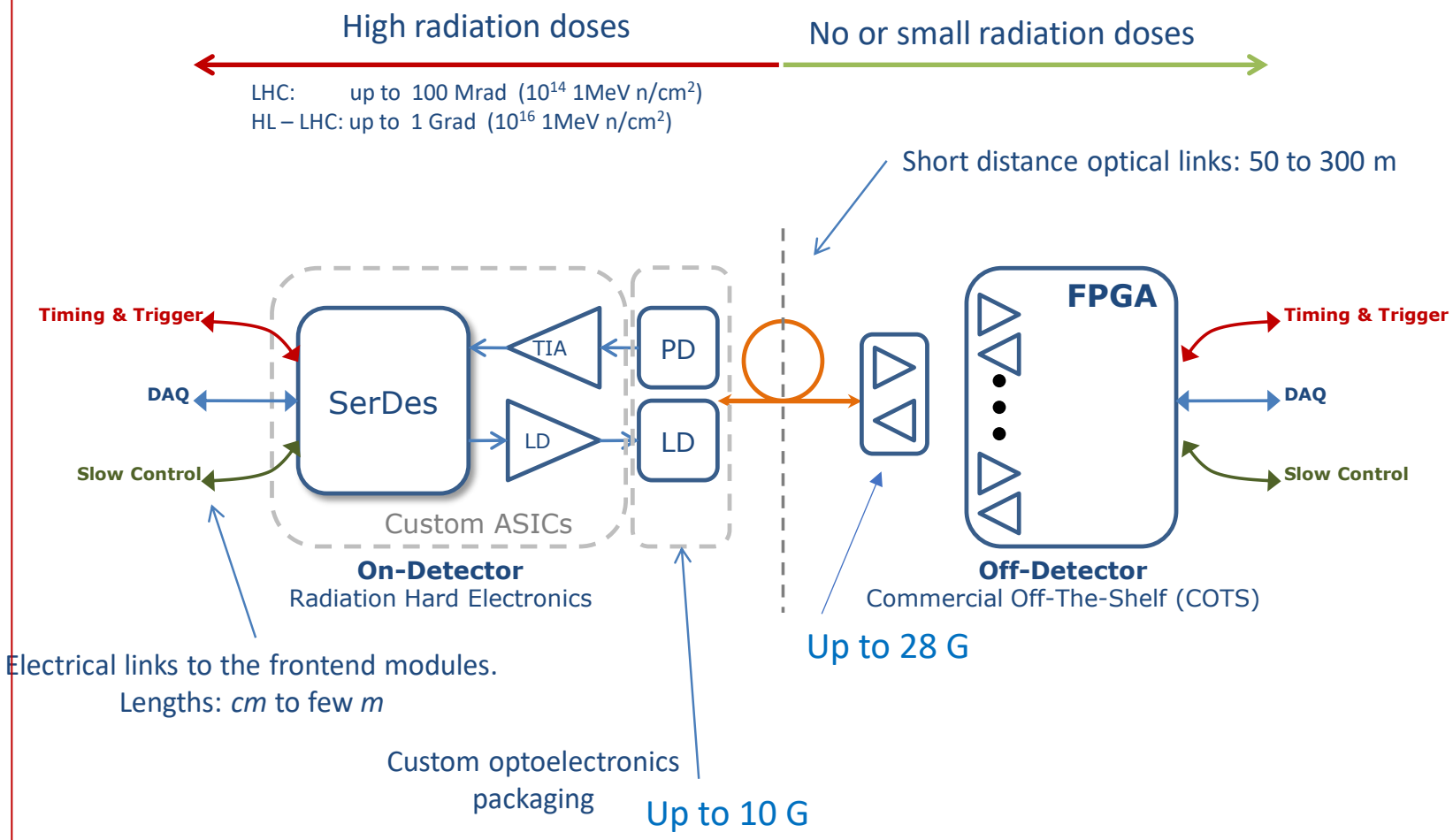
- A very brief overview of ASICs and optical modules that we have developed or have been using since 2000.
- Going forward what's on the horizon (my understand of it).
- Zoom in on R&Ds at SMU (in collaboration with CERN and IPAS):
  - GBS20 and GBT20 to push to 20 Gbps per fiber.
  - cpVLAD and QLDD to cope with extreme use conditions, example: inner tracker.
  - QTIA to explore ideas that may mitigate the p-i-n diode degradation in radiation,
  - QTRx, the first attempt on a 4Tx+4Rx optical module
- Summary.

Today's typical HEP Link Architecture

Challenges:

- Radiation, in detectors on both pp and ee machines.
- Reliability, especially the link to the detector, and the radiation induced SEUs and degradation in photo diode.
- High channel/data density and throughput from detector
- Low power, low mass and small formfactor (of the module)

Not included here is the electric link over low mass FLEX PCBs and cables for data from near the IP. This is the case for ATLAS ITK-pixel, as well as a direction in R&D due to the use of ultra low mass transmission media.



Slide from Paulo Moreira, CERN EP workshop on R&D, 2019/10/24

Detector data links in LHC experiments

Current LHC detectors

↓ ~ 10 yrs

For Phase-I upgrades

↓ ~ 10 yrs

Some for Phase-II upgrades

Generation/Speeds		(AS)ICs	OMs (Optical Modules)
1,	1.6 Gbps	G-Link (the only COTS, bipolar, high power) GOL (0.25 um CMOS, CERN ASIC)	OTx, ORx (COTS based custom optical modules) SC or ST type of COTS transceiver
2,	4.8 Gbps	GBTx, GBLD, GBTIA, LOCx2-130 (ASICs using 130 nm CMOS)	VTRx (optical module, CERN common project)
	5.12 Gbps	LOCx2, LOCld (ASICs 0.25 um SOS)	MTx, MTRx (specially for LAr, 6 mm height)
3,	5.12 /10.24 Gbps 7*1.28 Gbps	lpGBT, LDQ DLAS10, cpVLAD (65 nm CMOS) GBCR, a cable receiver for electrical transmission over meters	VTRx+ (4 Tx + 1 Rx array), MTx+, MRx+, MTRx+ (LC optical coupler based) QTRx (4Tx + 4Rx, MT fiber coupler)

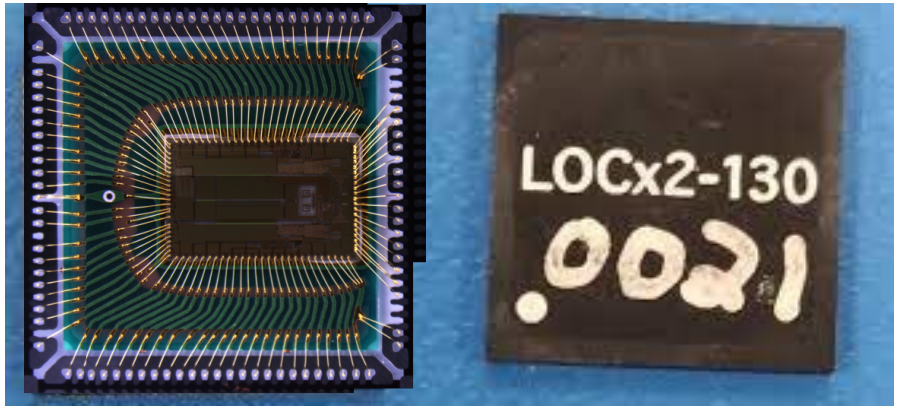
lpGBT 1st prototype

* Blue: work from SMU; in the case of lpGBT, with SMU contributions.
* list incomplete: not included custom modules in tens of Mbps developed for inner trackers.
* System level studies were carried out by the Versatile Link common project. It is important to point out that current tera-bit-per-second systems need system level specs to ensure reliability.

LTDB

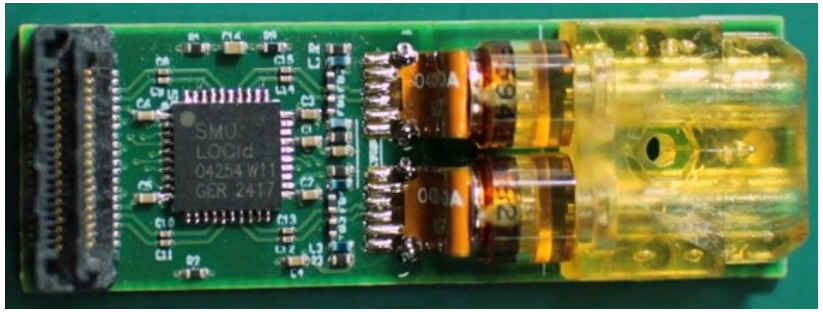
double sided

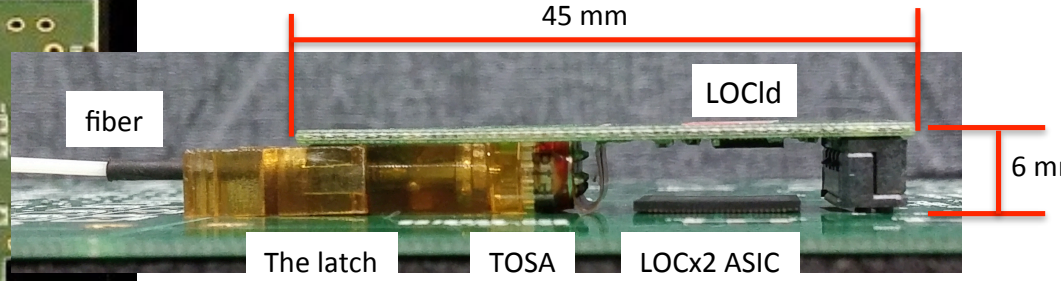
Example in ATLAS LAr phase-1



12 × 12 mm²

MTx





LOCx2 and MTx on LTDB

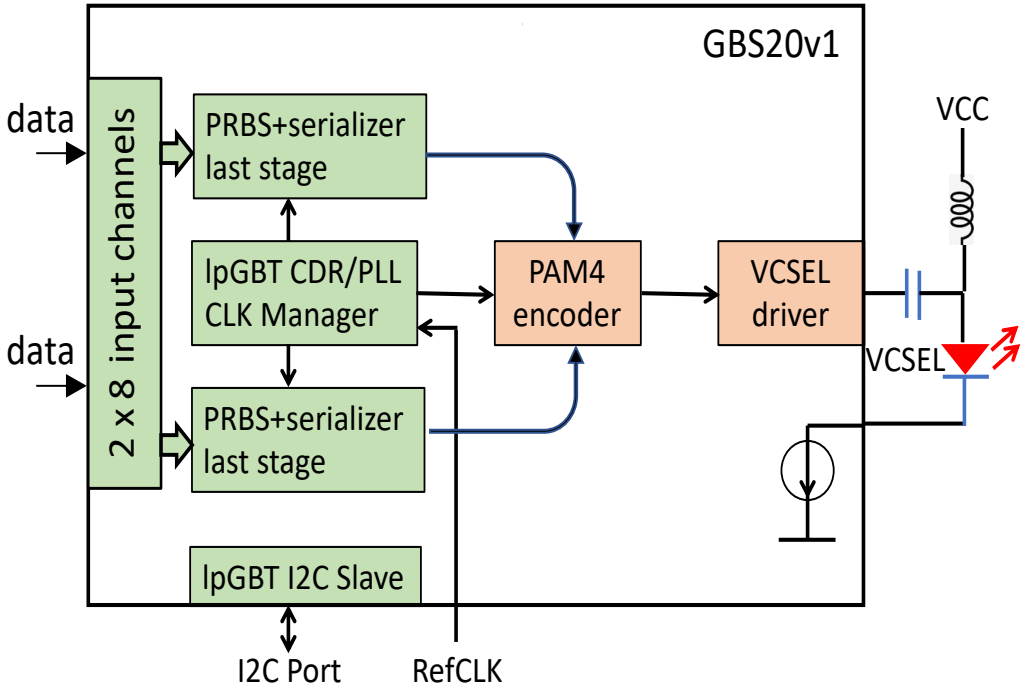
Looking forward

- Not trying to do any advertisement for CERN, but I would like to point out the following developments that I know:
  - CERN EP R&D program and the WG6 on Fast Links: ASICs on high data rates, optoelectronics drivers and low-mass electrical cable transmission; FPGA-based system testing and emulation; Silicon photonics (chip, packaging and system, and next-generation VCSEL-based optical modules). On ASIC, one goal is 28 nm CMOS based 28 Gbps NRZ and 56 Gbps PAM4 transmitters.
  - Task Force 7 reports (March 25, 2021) in the the ECFA Detector R&D Roadmap Symposia cover ASICs and Links for detector front-end electronics, including data links.
- Some R&Ds on links at SMU.

GBS20

- GBS20 is an ASIC that uses many design blocks from lpGBT (65 nm CMOS), plus a PAM4 encoder + driver, for a data rate at 20.48 Gbps per fiber.
- Innovation: the highspeed clock drives the two serializers and the PAM4 encoder, greatly simplifies the link transmitting circuit implementation.
- Potential: double the lpGBT data transmission rate, open doors for physics and/or significant savings on readout electronics.

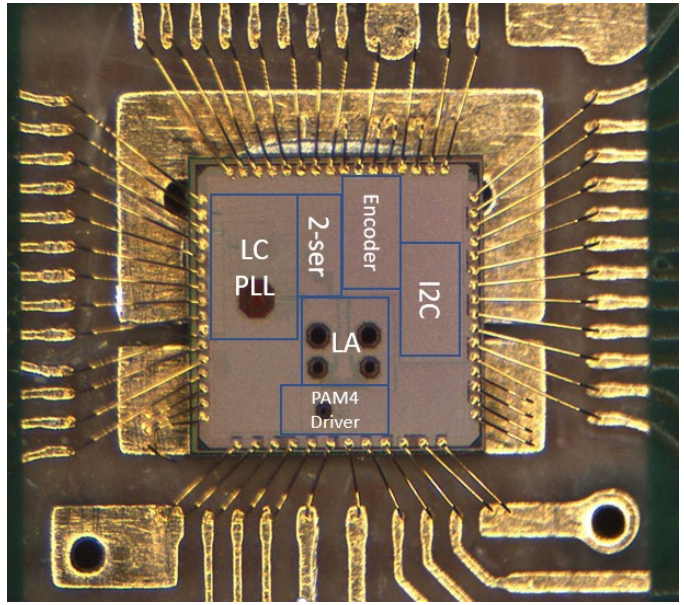
Top level diagram of GBS20 prototype version 1

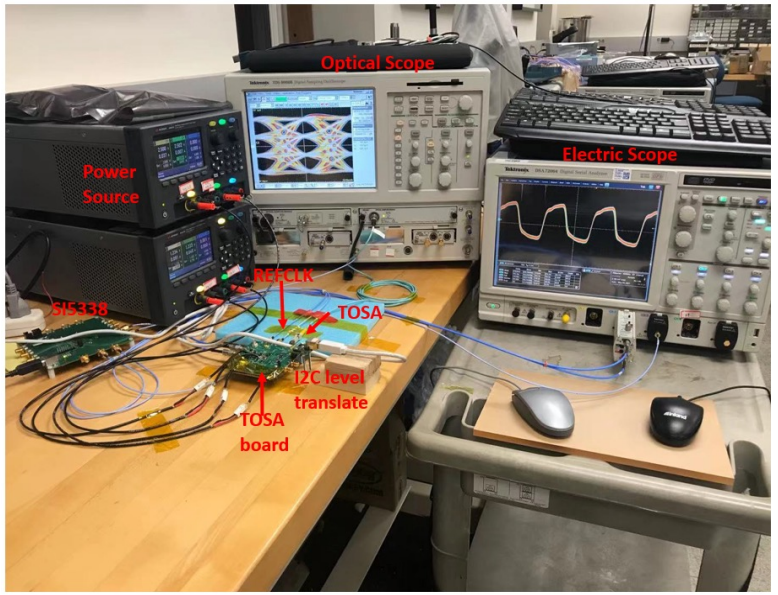


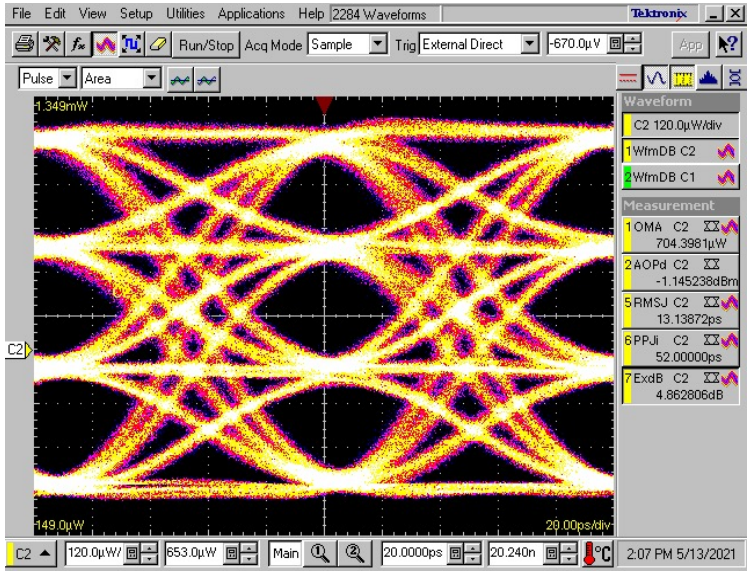
- The R&D provides experience in PAM4 + VCSEL for future designs in 28 nm PAM4 which will be a lot more expensive than 65 nm.
- Going to 28 Gbps NRZ or 56 Gbps PAM4 will need more studies on fibers (OM4 and OM5). Fiber must be rad-tol as well.

GBS20 and GBT20

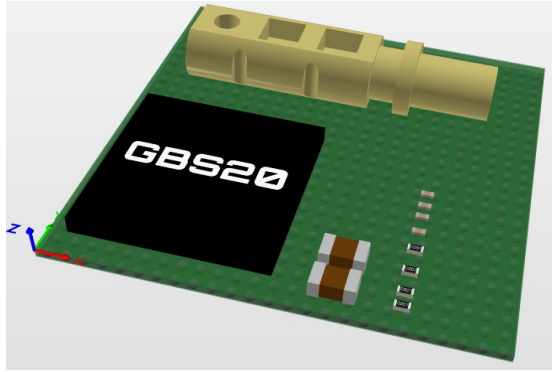
- Test results of GBS20 version 0 were reported at RT2020, Tests of version 1 are on-going and planned to be reported at TWEPP this year.





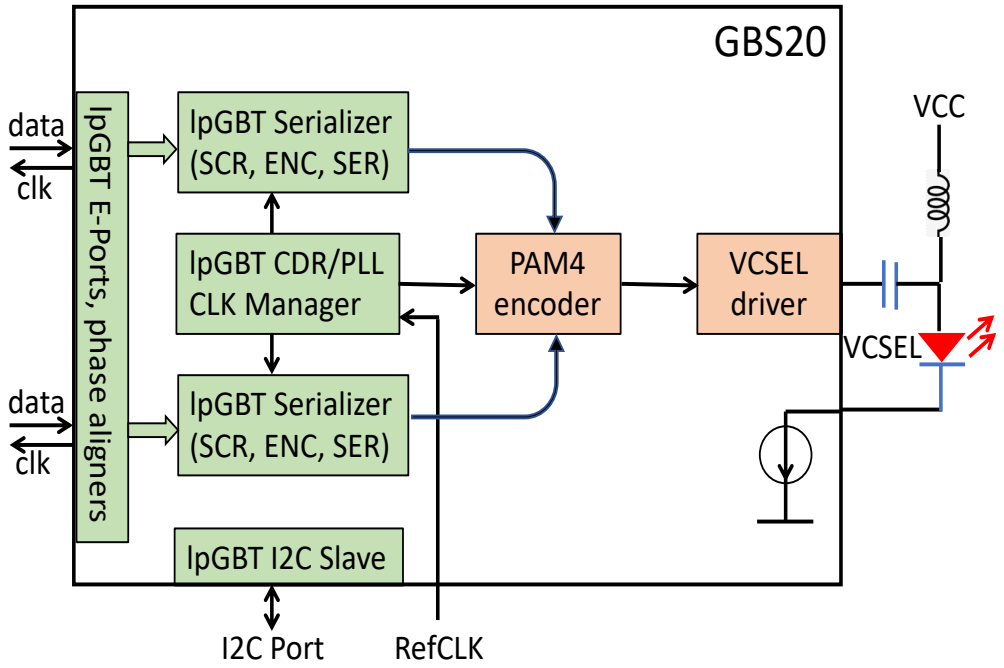


- The final goal pf GBS20 is to implement the full lpGBT transmitter (and the link protocol), and to develop the optical transmitter, GBT20, as a mezzanine, to fit into the lpGBT ecosystem, and to spare system developers the trouble of dealing with fast (10G) PCB layout and expensive PCB materials.



20 Gbps per channel in lpGBT ecosystem

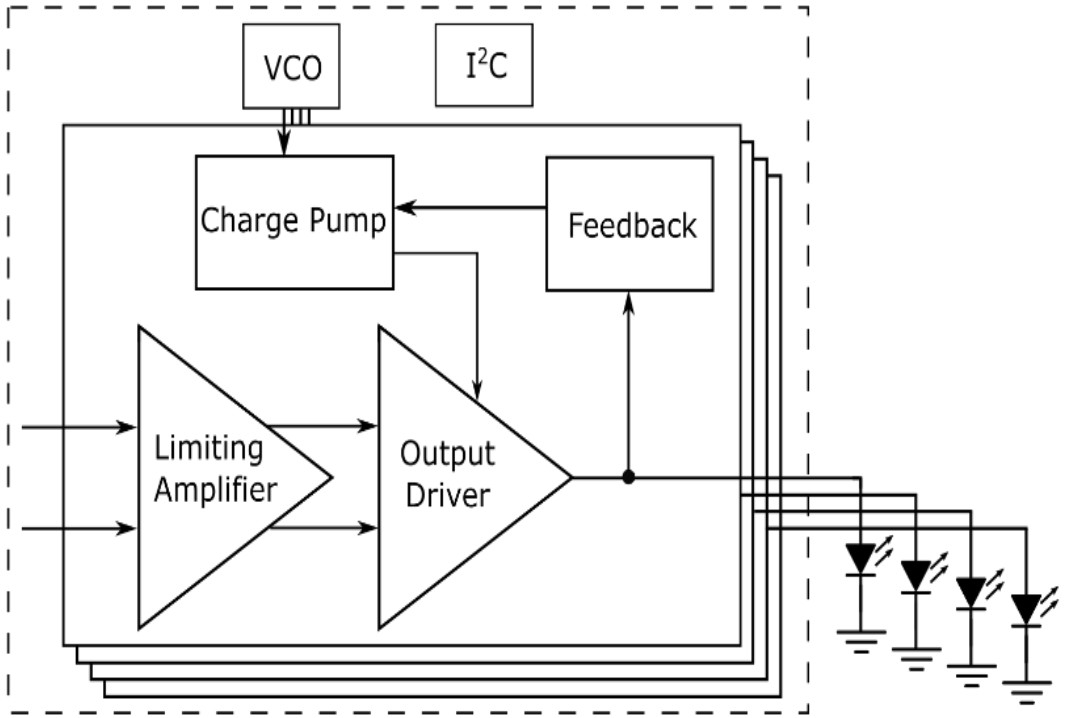
- The final GBS20 ASIC will use the complete transmitter of lpGBT with the same ePort and user interface. It may use the same C4-BGA package (a way to cut down cost).
- As we failed to find a COTS optical receiver with PAM4 at 20 Gbps (they are all at 56 Gbps for the moment), we decide to look into a receive circuit for the receiver this year (before TWEPP).
- The plan is that we will conclude this effort as R&D at GBS20v1, with 2 ~ 3 papers in 2021/22.



- If there is interest in the community to continue, dedicated resource will need to be identified for future ASIC and system prototypes.

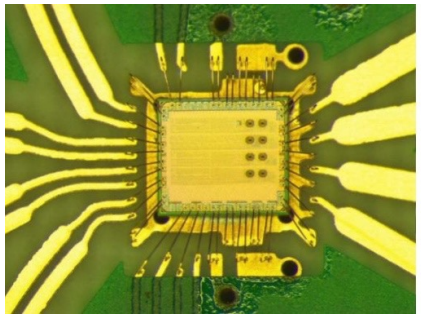
cpVLAD and QLDD

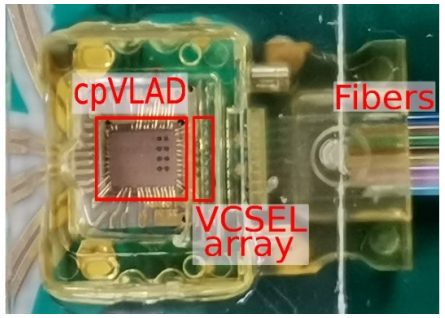
- cpVLAD and QLDD are a 4 lane, 10 Gbps each, VCSEL array driver developed to address the issue that VCSEL forward voltage increases under ultra high radiation and low temperature. This increase will cause problem of array optical transmitters in the current 1.2 and 2.5 V powering scheme.
- cpVLAD is the R&D version. QLDD is the production ready design.

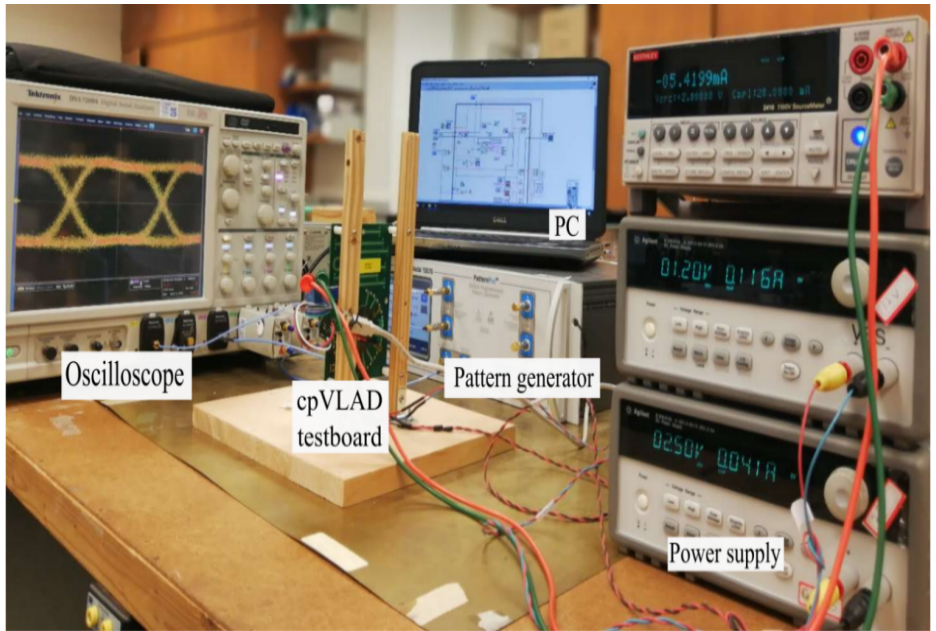


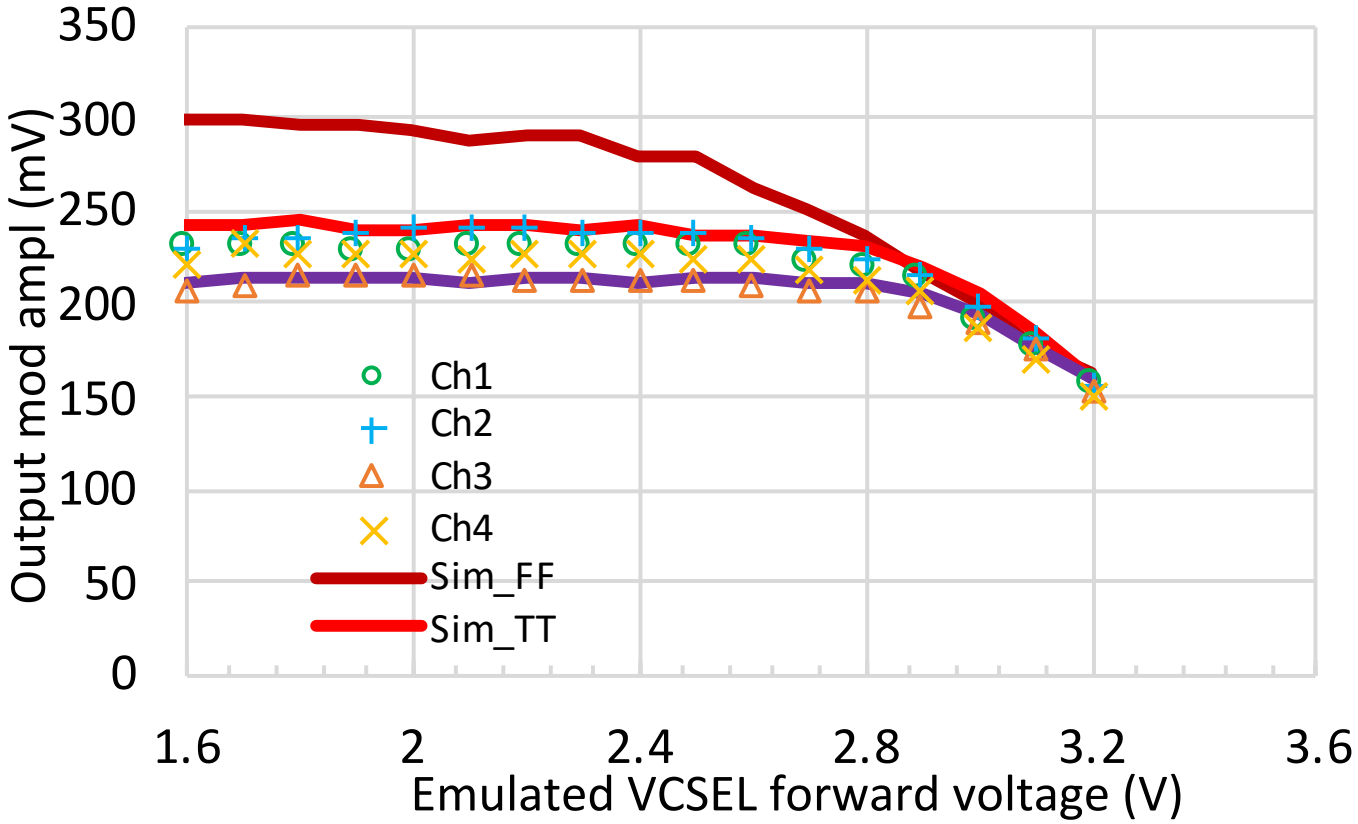
Test results

- cpVLAD has been fully tested and reported (TWEPP and JINST). QLDD is being tested. The results are submitted to TWEPP this year.



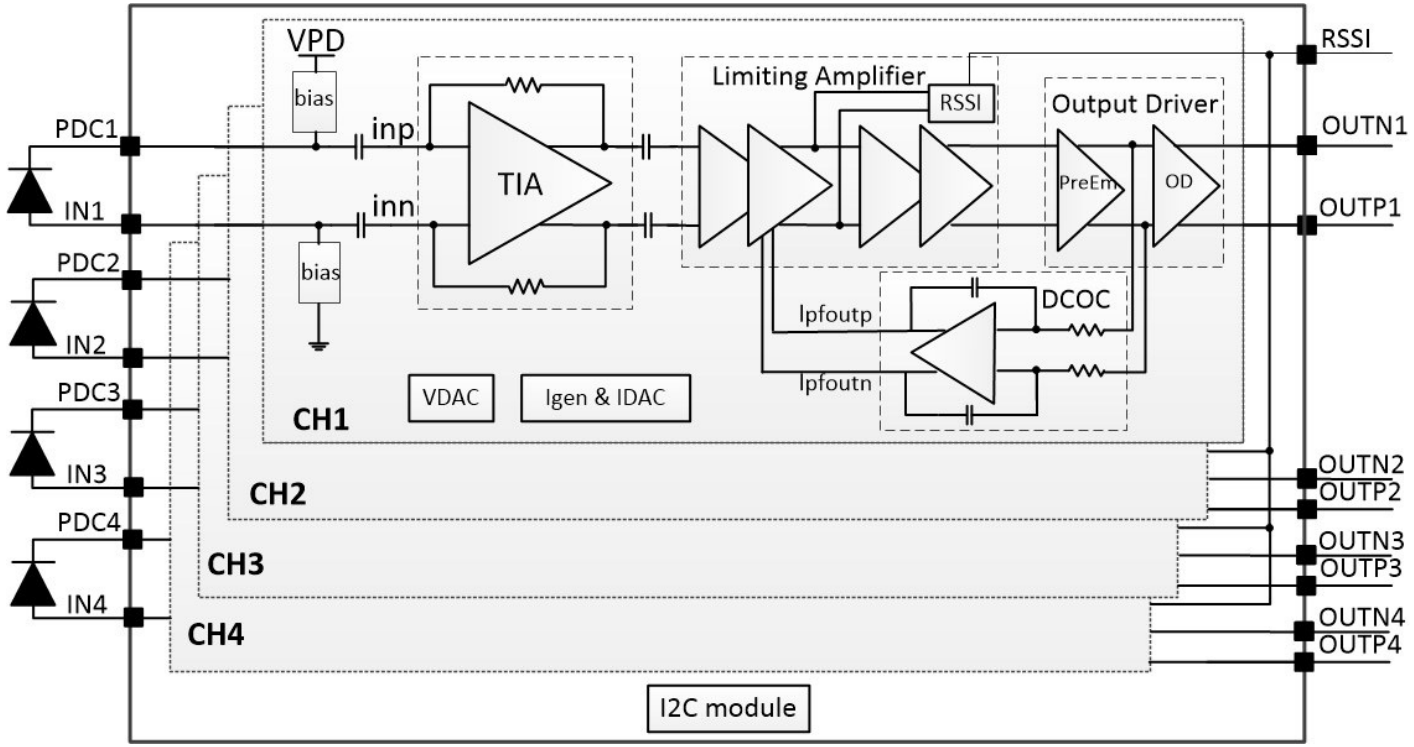






QTIA

- QTIA is a 4 lane array p-i-n diode (GeAs or InGeAs) TIA + LA. The speed is selectable to be 2.56 and 10 Gbps. Different diode biasing schemes, with one that has a charge pump to raise the bias voltage, are designed in the 4 channels to search for mitigation to radiation induced performance degradation of the diodes.

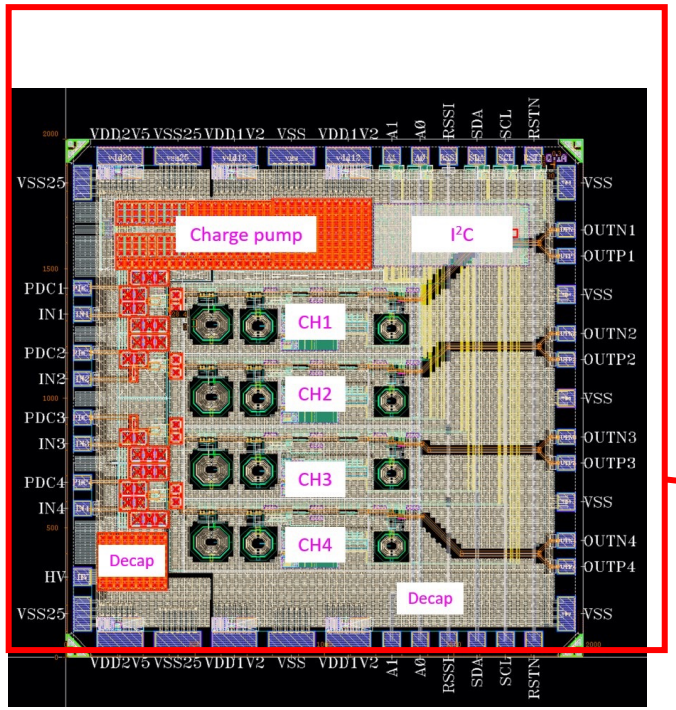


Other than testing the TIA + LA, we will test different biasing condition to the diode to mitigate responsivity loss due to radiation.

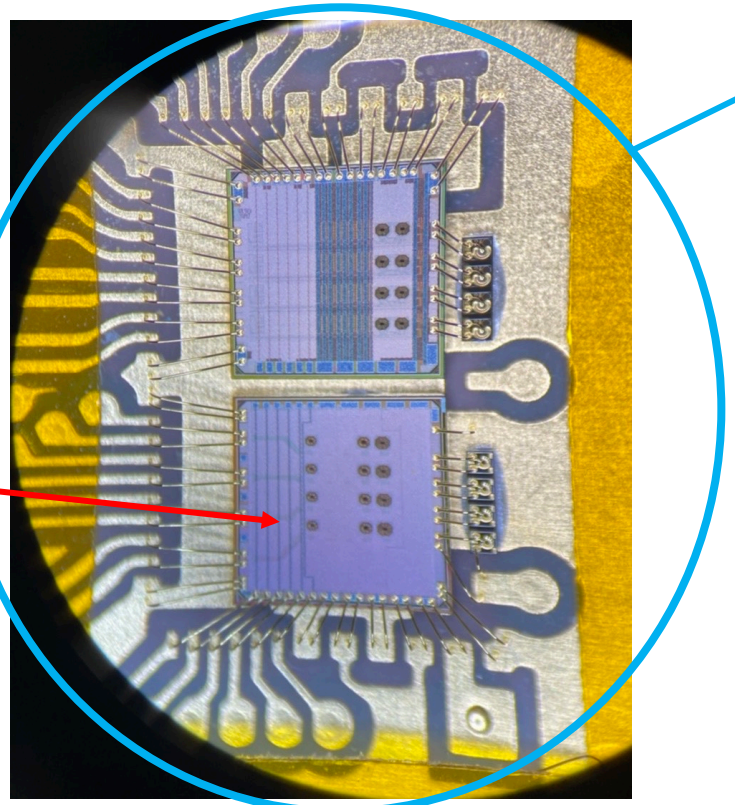
- ❑ CH1: charge pump + PD bias UP & Down
- ❑ CH2: (VDD25) + PD bias UP
- ❑ CH3: (VDD25) + PD bias Down
- ❑ CH4: HV (external) + PD bias UP & Down

QTIA, QLDD and QTRx

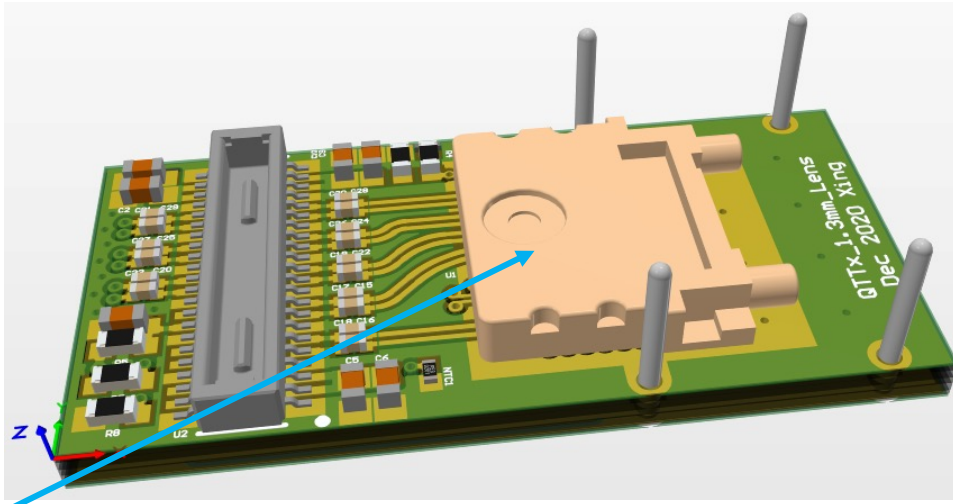
- Tests of the prototype chips are on-going.
- The final goal of this ASIC is for the 4Tx+4Rx optical module QTRx, with QLDD as the VCSEL driver. The report on QTRx is submitted to TWEPP.

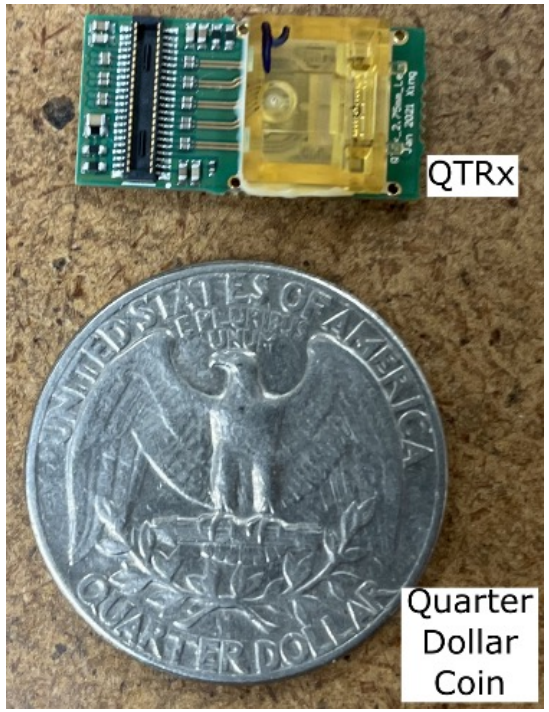


QTIA



QTRx optical module, 10 mm x 20 mm
4 Tx + 4 Rx, each up to 10 Gbps





Summary

- We progressed from 1 Gbps (15 – 20 yrs ago) to 5 Gbps (deploying now, and for ATLAS LAr phase-1) and are reaching 10 Gbps (for LAr phase-2) for detector data transmission. In data rate 10 Gbps per fiber is the state-of-the-art.
- For link systems, many ASICs and Optical Modules have been developed, and the community is adapting to the lpGBT ecosystem (transmission protocol and forward error correction for SEUs).
- While the GBT and lpGBT ecosystems from the common projects are vital for future detector data transmission systems, ASICs may still be needed for applications that have special needs, example: low and fixed latency in trigger channels.
- To push the speed further up, there are plans of R&Ds to reach 28 Gbps NRZ and 56 Gbps PAM4, through 28 nm CMOS. This will be difficult + expensive and in future.
- In collaborations with CERN and IPAS, SMU is carrying out R&Ds on a few ASICs and optical modules to address difficult issues in detector data transmission, and has demonstrated 20 Gbps per fiber using PAM4 and the 65 nm CMOS.