

Progress Report

RIKEN/RBRC

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Proposed New INTT Meeting Time

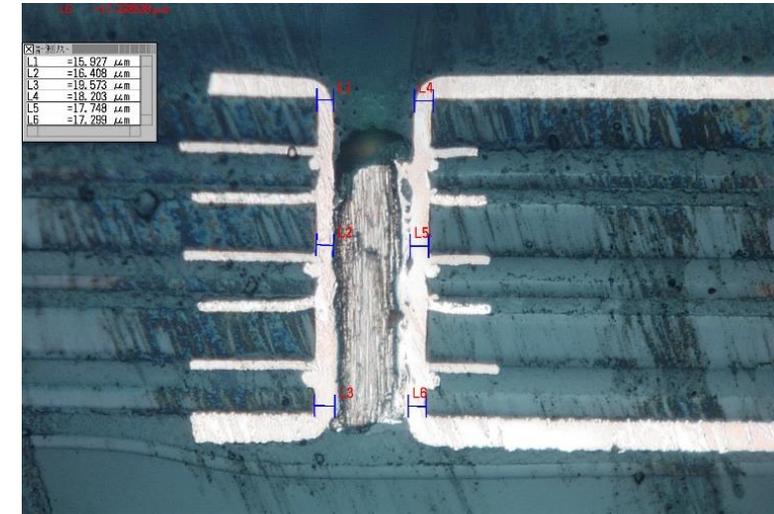
- Tuesday 9PM in BNL time = Wednesday 10AM in Japan = Wednesday 9AM in Taiwan
- The new meeting schedule is to be reflected from July 6th (July 7th in Asia).

Please speak up if you cannot manage your schedule with this proposal.

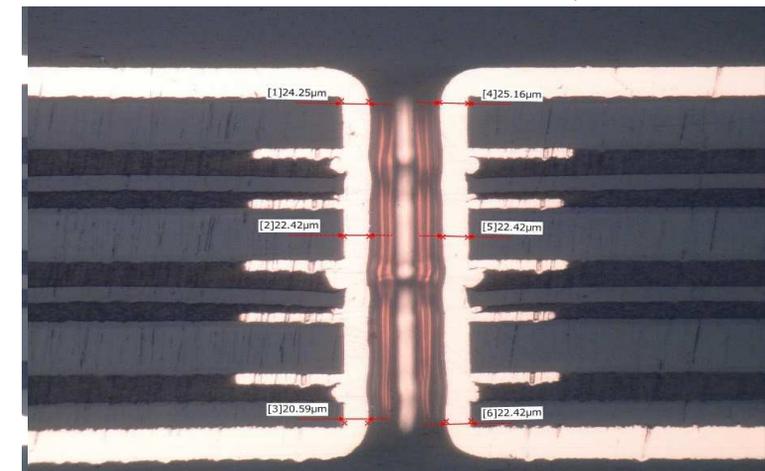
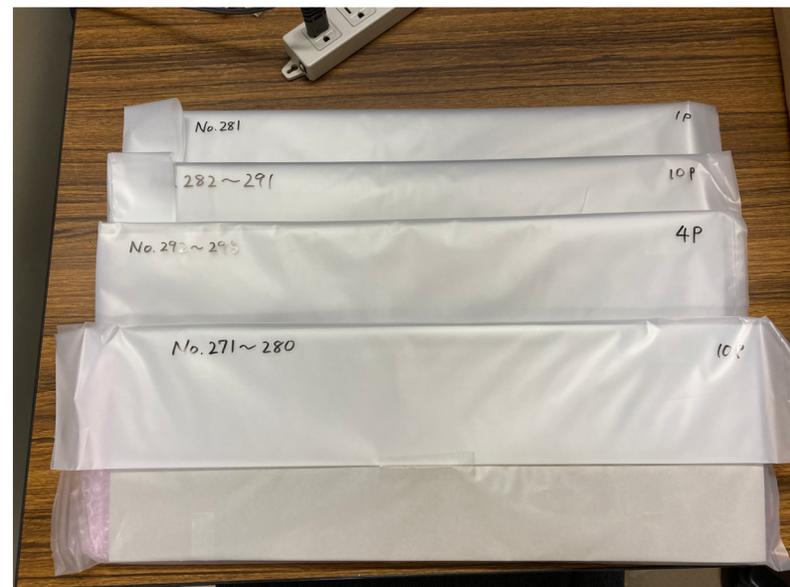
3rd Batch HDI

- June.28th : 11 HDIs were delivered on.
- July 6th : 14 HDIs were delivered.
- July 12th : 25 HDIs are to be shipped to BNL.
- July 19th : Another (upto) 20 HDI's to be delivered.

Thickness:15~18 μ m



Thickness:20~25 μ m



Delivery Day	Batch	Order #	LOT #	Quantity	HDI Serial No.		Incremented Quantity	Inspection	Result	Shipped to Taiwan	
2019/1/23	Preproduction	349670	302382	6							
2019/2/6		349670	302725	4							
2019/9/11		350963	306716	20							
2019/11/20		Exchanged	307469	1							
2020/4/2	Batch-1A	352075	310184	9	1	9	9				
2020/4/2		352075	310185_1	7	10	16	16				
2020/4/2		352075	310185_2	13	17	29	29				
2020/4/2		352075	310186	30	30	59	59	50	Good?		
2020/4/28	Batch-1B	352075	310188	17	60	76	76	70	bad		
2020/4/28		352075	310189	24	77	100	100	80, 94	bad		
2020/6/8		352075	311139	2	101	102	102				
2020/6/8		352075	311587_1	7	103	109	109	105		6	
2020/6/17		352075	311587_2	2	110	111	111				
2020/6/17		352075	311614	15	112	126	126	122		14	
2020/6/24		352075	311615	21	127	147	147	127		20	
2020/7/9		352075	312095	20	148	167	167	-160			
2020/7/9		352075	312096_1	6	168	173	173				
2020/7/21		352075	312096_2_1	7	174	180	180				
2020/7/28		Batch-1A	Exchanged	312096_2_2	1	24	24	180			
2020/9/28		Batch-2	353110	312532	20	181	200	200			
2020/9/28			353110	312533	16	201	216	216			
2020/9/29			353110	312534	7	217	223	223	-220		
2020/9/29			353110	312535	14	224	237	237			
2020/9/29			353110	312536	7	238	244	244			
2020/10/27	353110		313304	24	245	268	268	265		3	
2020/11/27	353110		313673	2	269	270	270			2	
2021/6/28	Batch-3			317333_2_2	11	271	281	281			
2021/7/5			317338	14	282	295	295				

Readbacker Test in RIKEN Test Bench

- Takashi&Runa's readbacker has been tested in RIKEN test bench.
- Readback values are somehow not exact.
- Looks like readback data is shifted by 1 bit in many cases but not all cases.
- This response is common to all parameters.

With Bus Extender

The screenshot shows a table of registers with columns for 'Reg', 'Desc', 'To Chip', 'From Chip', and 'Chip Command'. The 'To Chip' and 'From Chip' columns are highlighted with a yellow dashed box. The 'Chip Command' column is split into 'Read', 'Write', 'Set255', 'Reset', and 'Default'. To the right of the table is a grid of red buttons labeled with register numbers from 0 to 116.

Reg	Desc	To Chip	From Chip	Chip Command					
*	Wild	0		Read	Write	Set255	Reset	Default	Display/Modify Configur
1	Mask	0		Read	Write	Set255	Reset	Default	
2	Dig Ctrl	5	15	Read	Write	Set255	Reset	Default	
3	Vref	1		Read	Write	Set255	Reset	Default	
4	DAC0	8	16	Read	Write	Set255	Reset	Default	
5	DAC1	16	32	Read	Write	Set255	Reset	Default	
6	DAC2	30	60	Read	Write	Set255	Reset	Default	
7	DAC3	35	71	Read	Write	Set255	Reset	Default	
8	DAC4	40	80	Read	Write	Set255	Reset	Default	
9	DAC5	45	91	Read	Write	Set255	Reset	Default	
10	DAC6	50	100	Read	Write	Set255	Reset	Default	
11	DAC7	55	111	Read	Write	Set255	Reset	Default	
12	N1Sel <3:0>	6		Read	Write	Set255	Reset	Default	
	N2Sel <7:4>	4							

input readback

Readbacker Test in RIKEN Test Bench

- Readback Values are now consistent with write values.
- Consistent observation with NWU.

Reg	Desc	To Chip	From Chip	Chip Command				Display/Mem	
				Read	Write	Set255	Reset		Default
*	Wild	0		Read	Write	Set255	Reset	Default	
1	Mask	0		Read	Write	Set255	Reset	Default	
2	Dig Ctrl	5	5	Read	Write	Set255	Reset	Default	
3	Vref	1	1	Read	Write	Set255	Reset	Default	0 1
4	DAC0	16	16	Read	Write	Set255	Reset	Default	0 1
5	DAC1	24	24	Read	Write	Set255	Reset	Default	16 17
6	DAC2	32	32	Read	Write	Set255	Reset	Default	32 33
7	DAC3	36	36	Read	Write	Set255	Reset	Default	48 49
8	DAC4	42	42	Read	Write	Set255	Reset	Default	64 65
9	DAC5	44	44	Read	Write	Set255	Reset	Default	80 81
10	DAC6	57	57	Read	Write	Set255	Reset	Default	96 97
11	DAC7	80	80	Read	Write	Set255	Reset	Default	112 113
12	N1Sel <3:0>	6	6	Read	Write	Set255	Reset	Default	
	N2Sel <7:4>	4	4						
13	FB1Sel <3:0>	4	4	Read	Write	Set255	Reset	Default	
	.eakSel <7:4>	0	0						0 15 0 1
14	P3Sel <1:0>	1	1	Read	Write	Set255	Reset	Default	1 15 0 1
	P2Sel <7:4>	4	4						2 15 0 1
15	GSel <2:0>	2	2	Read	Write	Set255	Reset	Default	3 15 0 1
	BWSel <7:3>	8	8						4 15 0 1
16	P1Sel <2:0>	5	5	Read	Write	Set255	Reset	Default	5 15 0 1
	InjSel <5:3>	0	0						6 15 0 1
17	LVDS Current	8	8	Read	Write	Set255	Reset	Default	7 15 0 1
18	Resets	n/a		Read	Write	Set255	Reset	Default	

Without Bus Extender

Readback debugging in progress

- Will trace back SC data from FEM-IB to FPHX to locate where the bit is screwed up.
- The ROC in RIKEN is one of the ROCs took out from the FVTX big wheel.

