EIC Calorimetry WG Meeting

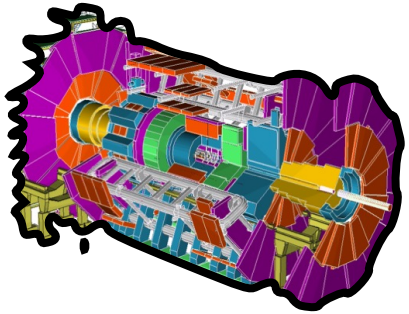
Argonne NATIONAL LABORATORY

AstroPix for EIC Calorimetry

ANL EIC Calorimetry Team
W. Armstrong, S. Joosten, J. Kim, J. Metcalfe, Z.E. Meziani, C. Peng, M. Scott, M. Żurek

U.S. DEPARTMENT OF ENERGY Argonne National Laboratory is a U.S. Department of Energy laboratory managed by UChicago Argonne, LLC.

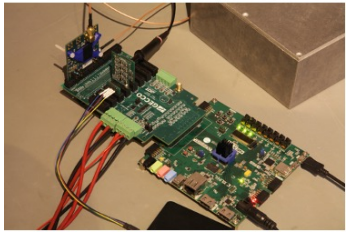
07/06/2021



CMOS detector
Designed for ATLAS experiment
Tested for high-radiation environments

ATLASPix
Final version of detectors for ATLAS experiment

Modify design for low power, better energy resolution, etc. (larger pixel size, slower)



Space-based CMOS detector
Designed for gamma-ray detection

AstroPix APS

AstroPix_v1
Engineering Development from ATLASPix

Changes to increase fidelity, optimize pixel size, readout architecture

Space-based CMOS detector
Designed for AMEGO-X

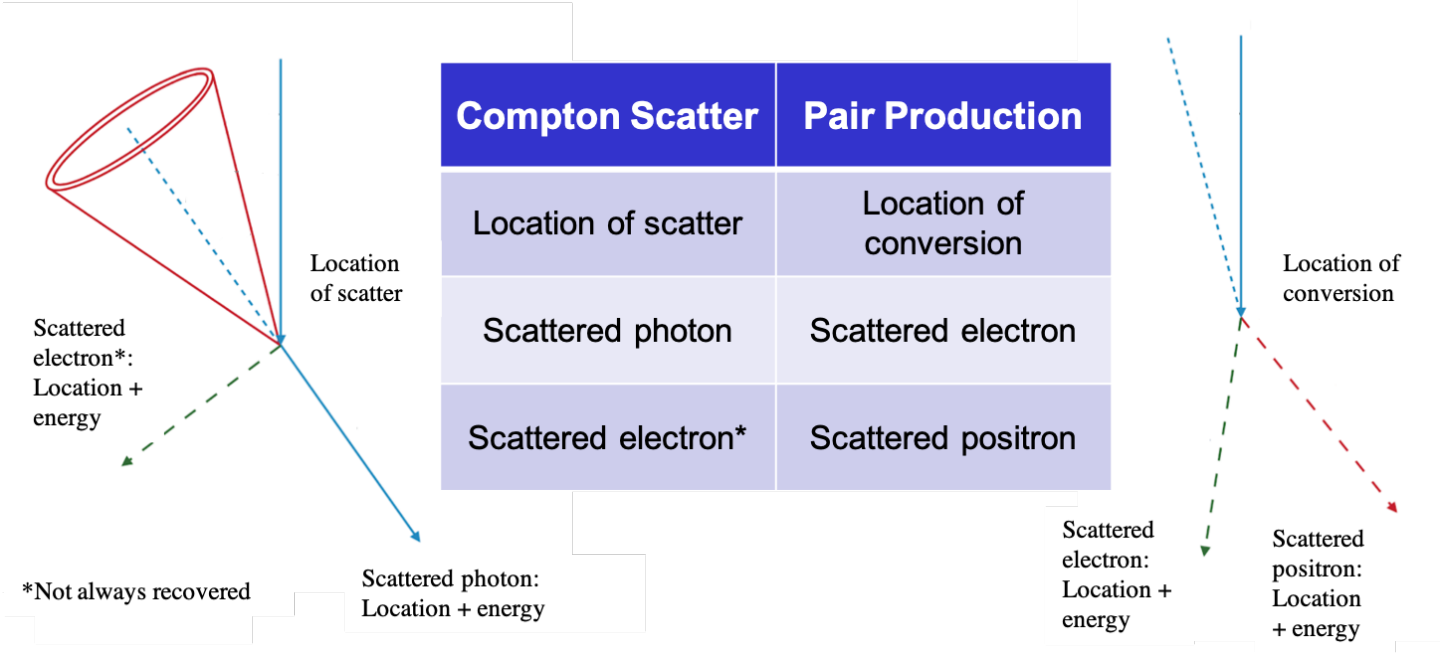
AMEGO-X APS

AstroPix
Engineering Development from AstroPix

AMEGO-X

And of course, it detects MIPS

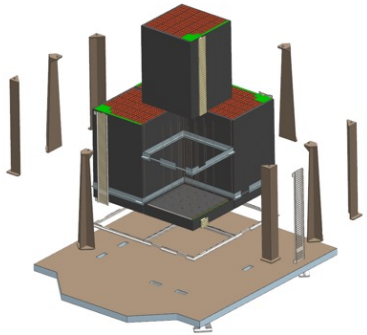
- **Photons in this energy range:**
  - **Interact via Compton scattering and pair production**
- **Gamma rays are detected via either Compton scattering or producing electron-positron pairs in the detector material**

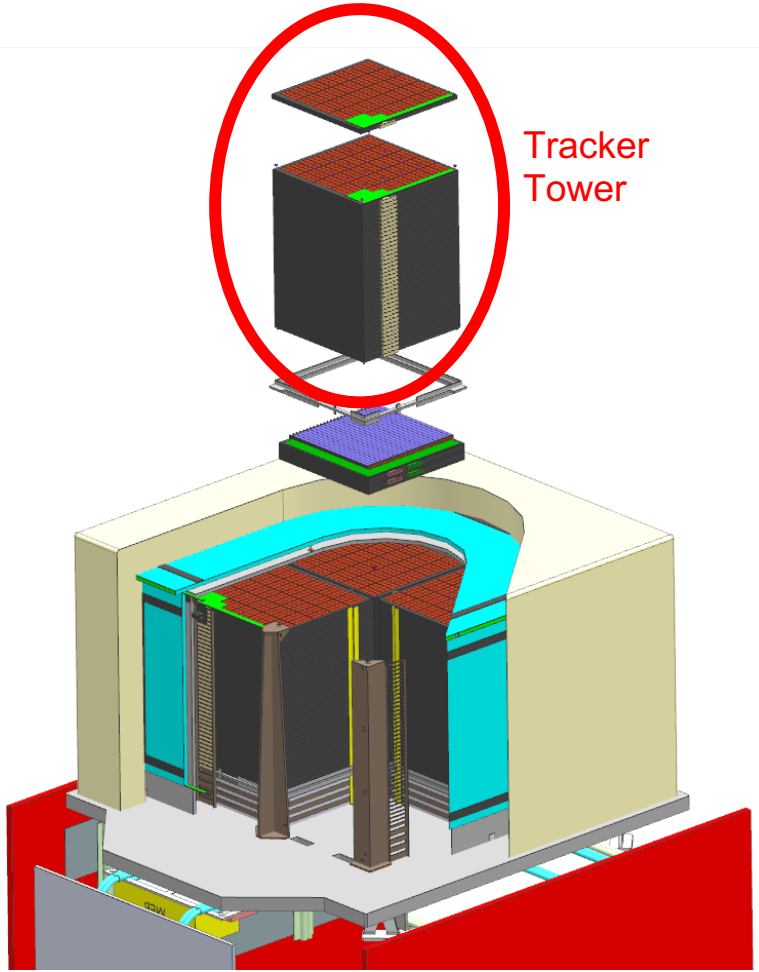


Compton Scatter	Pair Production
Location of scatter	Location of conversion
Scattered photon	Scattered electron
Scattered electron*	Scattered positron

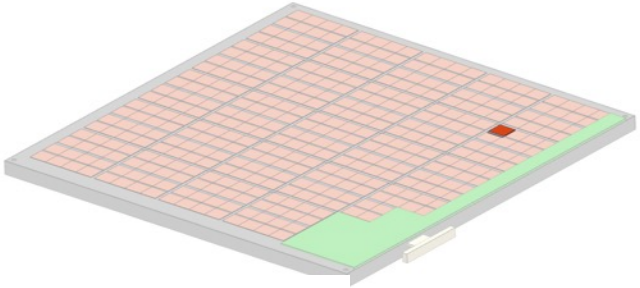
AMEGO-X

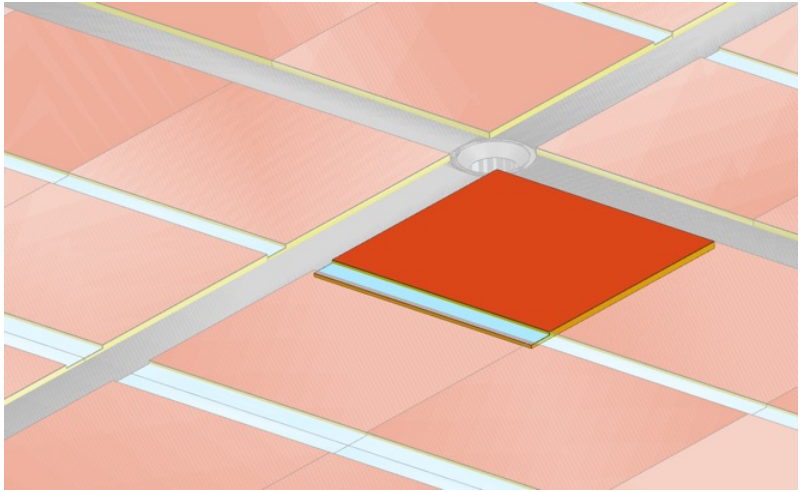
Gamma-ray detector
- 4 towers
- 40 layers
- 160 segment frames
- 95 AstroPix quad modules per segment frame
  - 15,200 AstroPix quad modules
  - 60,800 front-end read-outs

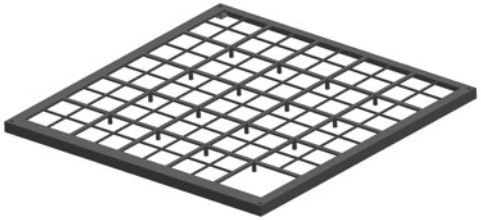


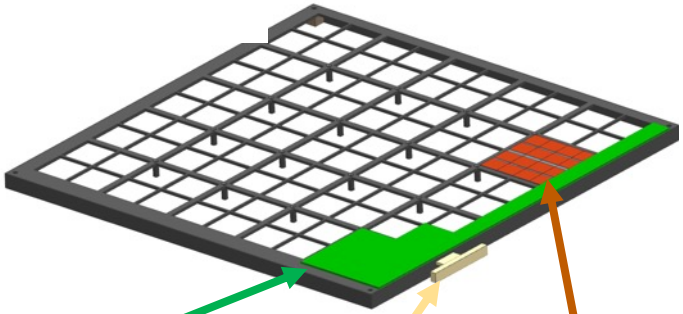


AMEGO-X Tracker



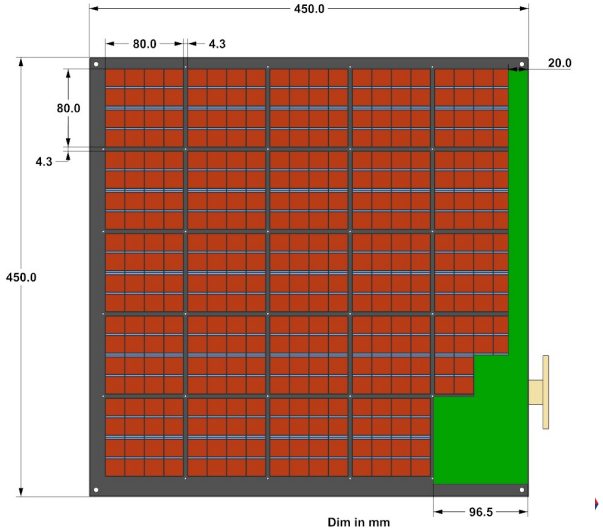






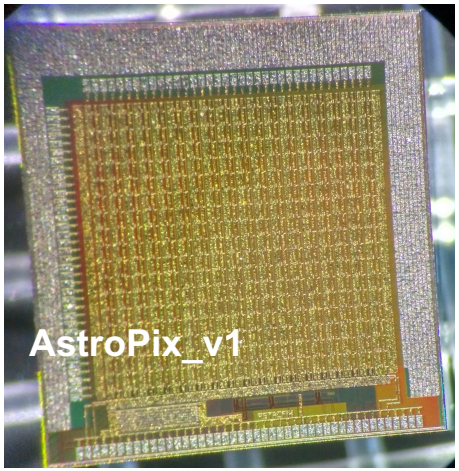
Single piece carbon fiber frame
- 0.45 m x 0.45 m
- Low dead material

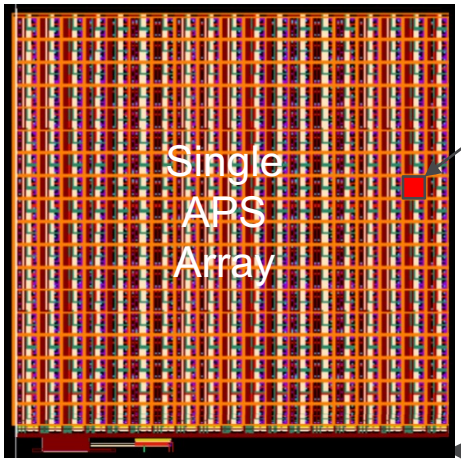
FPGA board, heat sink, model array
- Passive cooling only
- V1 measured 0.95 mW/cm^2
- V2 expect ~0.75 mW/cm^2

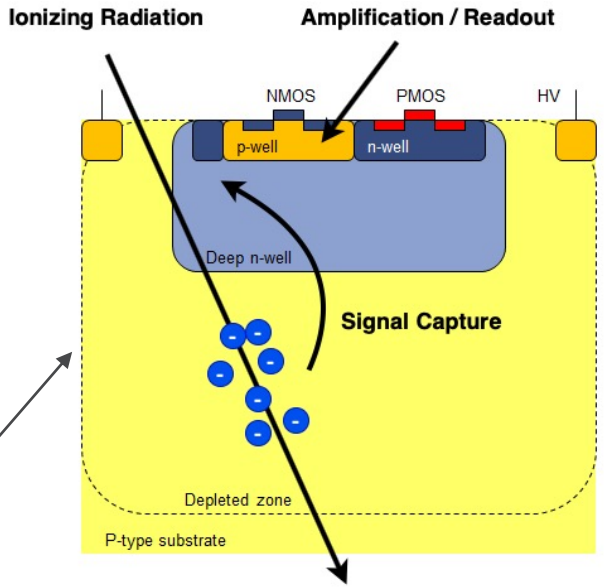


AstroPix

- AstroPix is a monolithic CMOS sensor
  - Collects via drift
  - 180 nm CMOS
- Technology grant from NASA for the development
  - Collaboration between Argonne, NASA Goddard, Karlsruhe Institute of Technology
- Baseline technology for AMEGO-X space instrument proposal



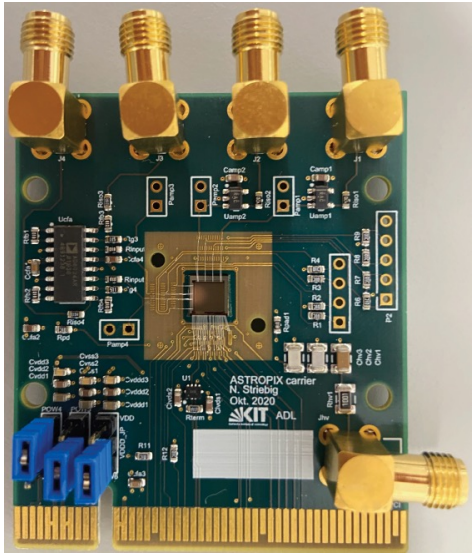




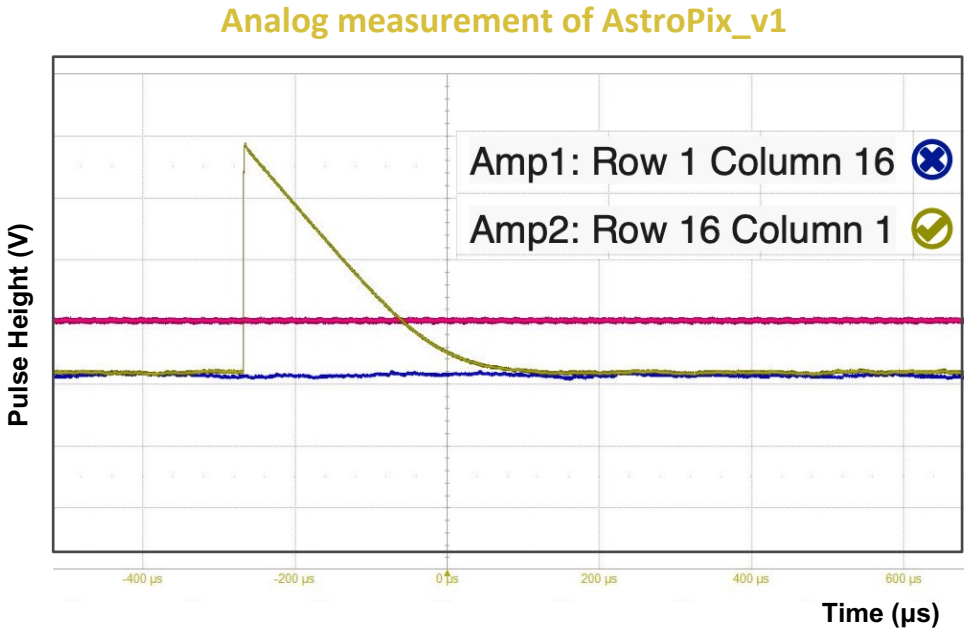
Parameter	Value	Unit
Min energy collectable	25	keV
Max energy collectable	700	keV
Power (per APS)	3	mW
Mass (per APS)	0.468	g
Voltage Bias	-120 V (configurable)	V

AstroPix

- 10 bit time-over-threshold and 12 bit time stamp from AMEGO-X energy resolution and timing req.
- easy to redesign for EIC if you don't use it out-of-the-box
- Quad SPI interface to enable chip-to-chip I/O
- Rise time < 10 ns

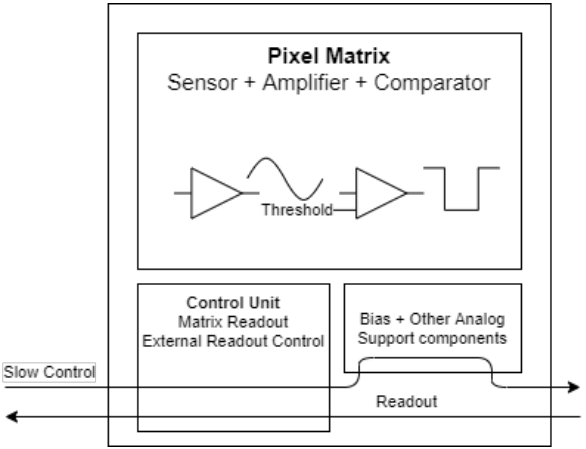


AstroPix_v1 in carrier board



AstroPix

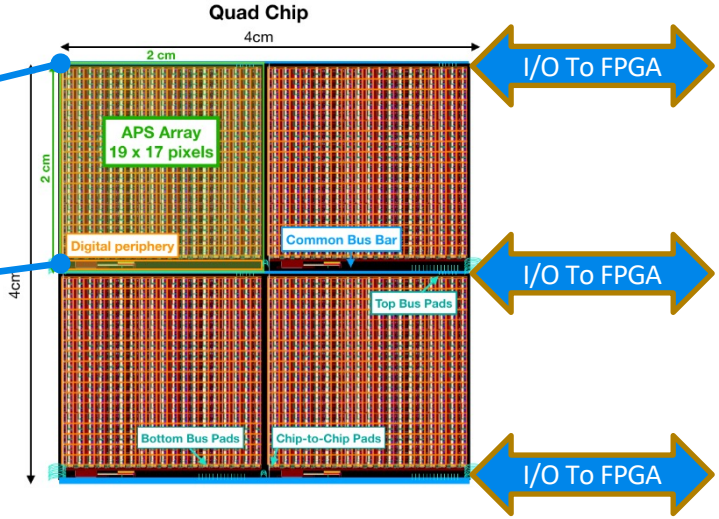
- Read out scheme is event driven by a pixel notifying the digital CMOS section that a hit occurred → self-triggered
  - Charge is amplified in pixel by a CTIA (Capacitive Trans Impedance Amplifier)
  - One signal goes to identify the column and one goes to identify the row of the pixel that was hit
  - The hit also causes the time over threshold (TOT) clock to start
    - Threshold levels are determined on the ground during calibration and testing
    - This will be adjustable/programmable
  - The energy deposited in the silicon is directly proportional to the TOT
    - Energy range and # of bits could be modified as needed
- The signal is passed on a bus from chip-to-chip until it reaches the fpga
  - Done to minimize dead material, hence gamma conversion in non-active material



AstrPix

Top Buses
4 Voltage + 2 grnd =
6 total

Bottom Buses
8 Voltage, 2 grnd, 2 clks,
1int, 1 hold = 14 total



- The six top buses are common for all arrays in one row
  - All 6 will be common for all arrays in a segment
- 14 bottom buses common for all arrays in one row
  - The 2 clocks and 1 hold will be common for all arrays in a segment = 3 per segment
  - Each row will have a unique interrupt = 20 interrupts per segment
  - 8 voltages: These should also be common for all arrays in a segment
  - Additionally, the 6 lines in the top bus and 6 in the bottom bus should be the same for each APS = 8 per segment
- 5 chip to chip SPI I/O lines common for all arrays in one row (daisy chained)
  - The SPI I/O should be unique to each row in the segment, but just 2 SPI clocks. This gives us 2 clocks + 4*20 = 82 unique lines per segment
- The SPI and TOT clocks are differential requiring two lines each = 3 more unique lines

Summary

- AstroPix designed for space-based applications
- Optimized for low mass, low power
- Could be re-optimized for EIC if needed or used out-of-the-box
- Low cost:
  - 56 chips/wafer * 70% yield = 156 cm^2
  - Wafer cost
  - Wafers: $115k + $1.6k/wafer
    - Includes wafer + process cost
  - 10 m^2 → 65 wafers → $219k
    - +$104k for each additional 10 m^2
    - ~$1.2M for 100 m^2

Backup