July/13/2021 INTT meeting

Investigation of the half entry issue at the RIKEN testbench

RIKEN, RBRC
Y. Akiba, I. Nakagawa, **G. Nukazuka**
Rikkyo Univ.：
H. Imai, Y. Nakamura, G. Nakano

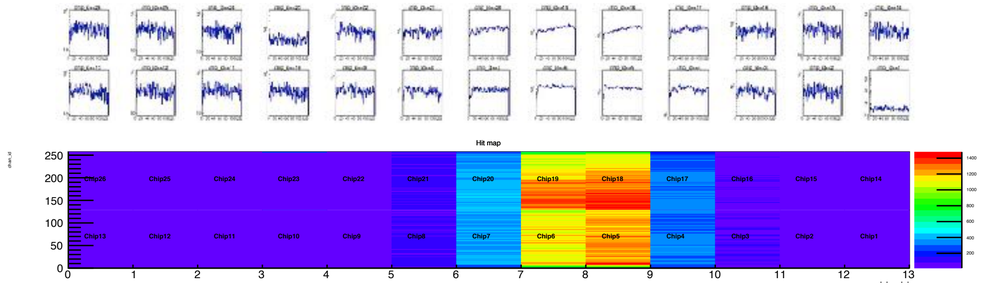
What was done after launching

Calibration tests

- delay configuration: 5 was found to be the best
- mass measurements with various conditions:

β-ray measurement

- successfully performed with/without an external scintillator trigger in June



Cosmic ray measurement

- successfully performed with/without an external scintillator trigger in June

What was done after launching

Calibration tests

- delay configuration: 5 was found to be the best
- mass measurements with various conditions:

ROC
NW1
SW5
#7

×

ROC port
A1, A2, A3
C1, C2, C3

×

Conversion cable
small #8
large #3

×

Bus extender
not used
new2 (know as bad)
1.2 m Preproduction #3
1.2 m Preproduction #4

×

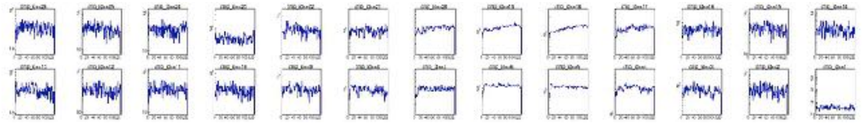
Ladder
#2
PPB2-L4N
PPB2-L4S

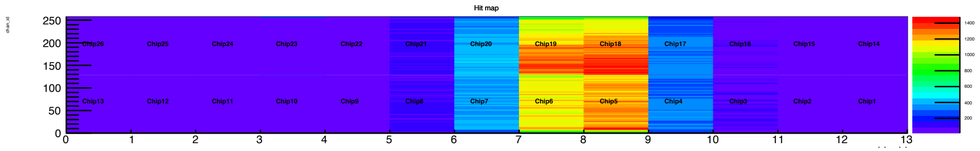
×

LVDS
from 1mA
to 8 mA

β-ray measurement

- successfully performed with/without an external scintillator trigger in June





Cosmic ray measurement

- successfully performed with/without an external scintillator trigger in June

What was done after launching

Calibration tests

- delay configuration: 5 was found to be the best
- mass measurements with various conditions:

one of lines for chip24 and chip26 are shorten

ROC
NW1
SW5
#7

regulators replaced
for 2.8 V and 3.0 V outputs

×

ROC port
A1, A2, A3
C1, C2, C3

×

Conversion cable
small #8
large #3

×

Bus extender
not used
new2 (know as bad)
1.2 m Preproduction #3
1.2 m Preproduction #4

×

Ladder
#2
PPB2-L4N
PPB2-L4S

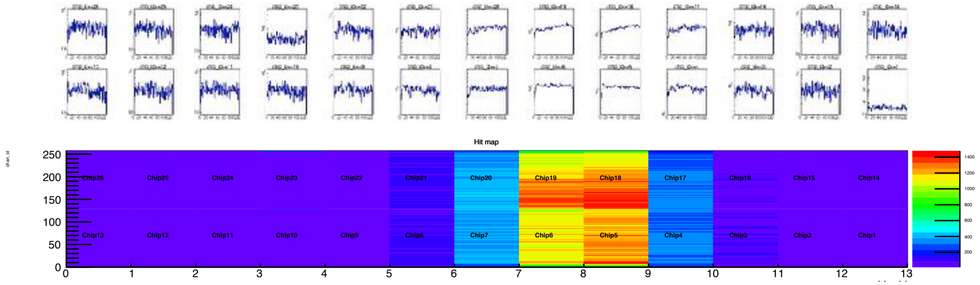
×

LVDS
from 1mA
to 8 mA

61 combinations, ~1800 meaningful data taken

β-ray measurement

- successfully performed with/without an external scintillator trigger in June



Cosmic ray measurement

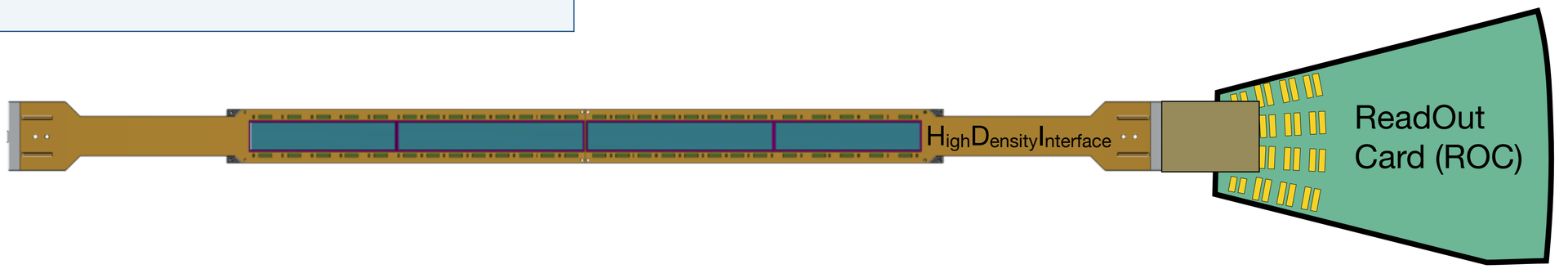
- successfully performed with/without an external scintillator trigger in June

Calibration tests without a bus extender

Measurements were performed without any major problems.

Performance of ROC ports

	A1	A2	A3	C1	C2	C3
7	Good except chip25	no data	Good except chip1-5	Good except chip15	Good	Good
NW1	no data	no data	no data	Good	Good	Good
SW5	Good	Good	Good	Good	Good	Good



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NW1	no data	no data	no data	Good	Good	Good
SW5	Good	Good	Good	Good	Good	Good

Setup
- Ladder: PPB2-L4S
- ROC, port: SW5, C3
- Conversion cable: small 8
- Bus extender: 1.2 m Prepro3

Performance of ROC SW5 port C3

Quality / LVDS (mA)	Perfect	Fine	Bad/Dirty	Half entry, lost channels	Total
1	46 92%	2 4%	2 4%	0 0%	50 100%
2	54 100%	0 0%	0 0%	0 0%	54 100%
4	48 96%	0 0%	2 4%	0 0%	50 100%
8	96 93%	5 5%	1 1%	1 1%	103 100%
Total	244 381%	7 9%	5 9%	1 1%	257 400%

Calibration tests without a bus extender

Setup

- Ladder: PPB2-L4S
- ROC, port: SW5, C3
- Conversion cable: small 8
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Performance of ROC SW5 port C3

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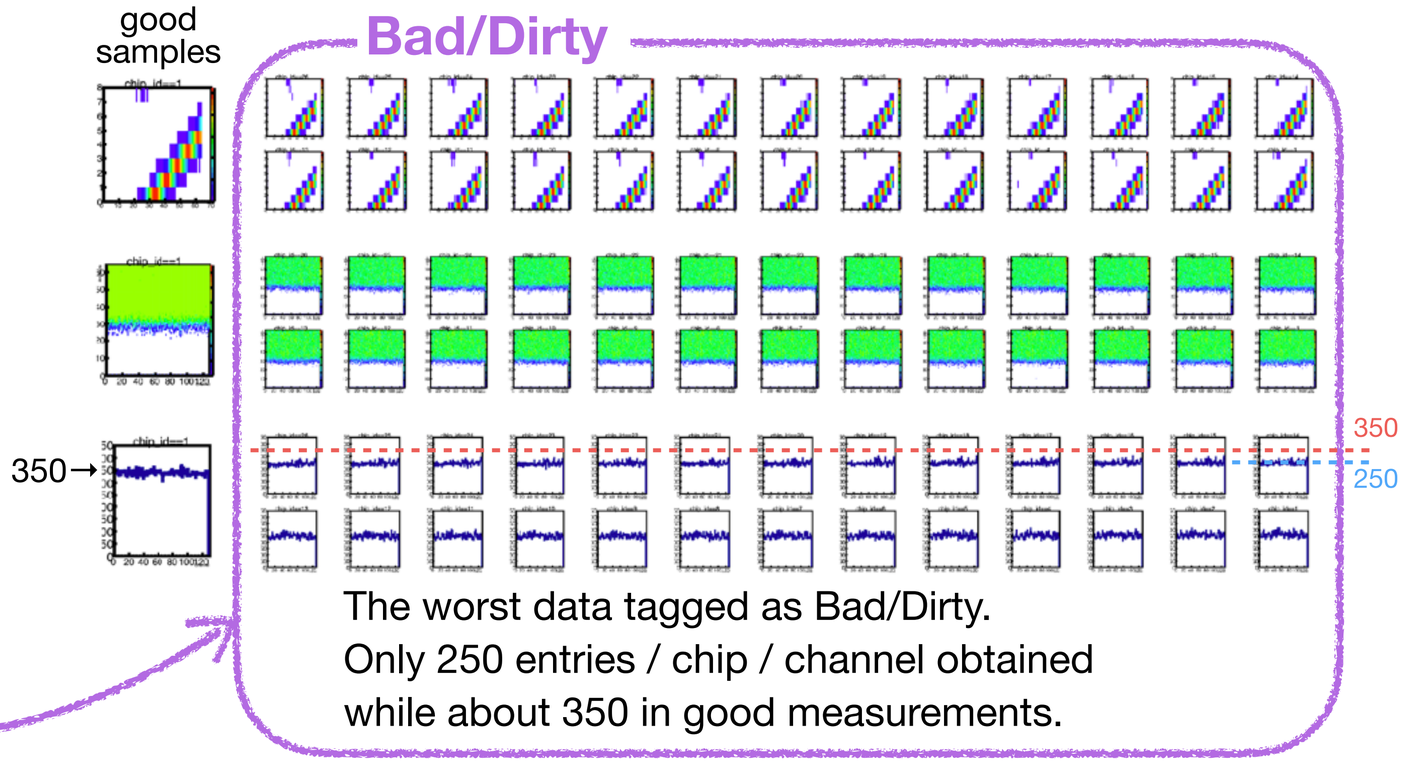

Calibration tests without a bus extender

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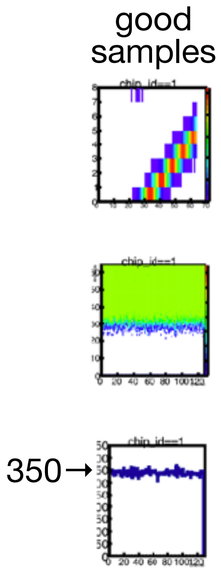
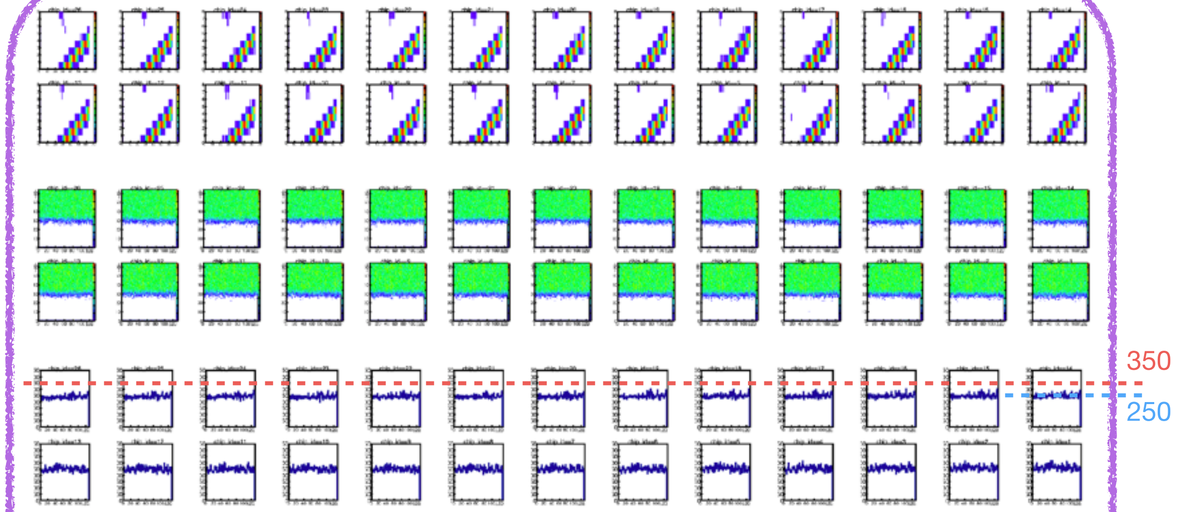
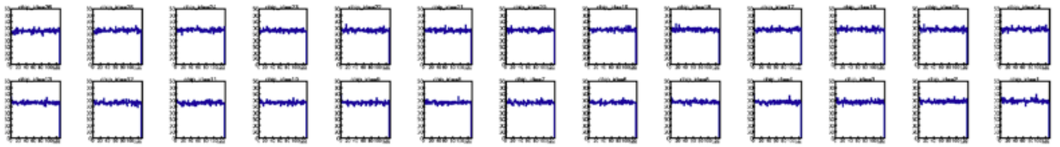


Bad/Dirty



The worst data tagged as Bad/Dirty.
Only 250 entries / chip / channel obtained
while about 350 in good measurements.

Fine



Data tagged as Fine.
300 entries / chip / channel obtained
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Calibration tests without a bus extender

Setup
- Ladder: PPB2-L4S
- ROC, port: SW5, C3
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Performance of ROC SW5 port C3

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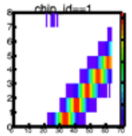
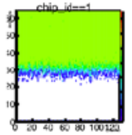
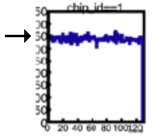
good samples

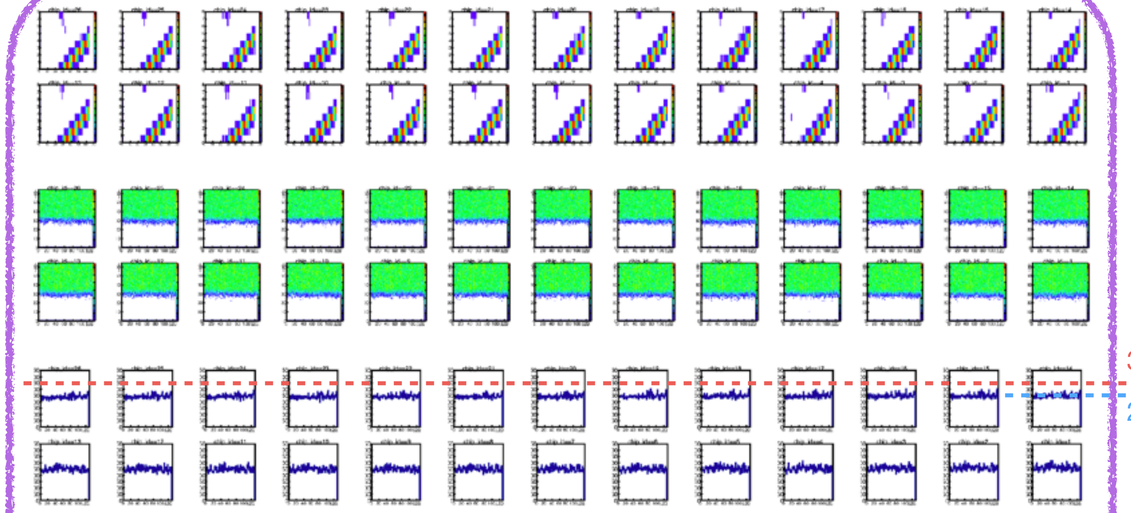




350→



Bad/Dirty



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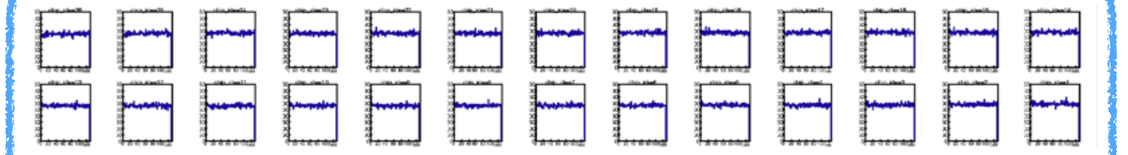
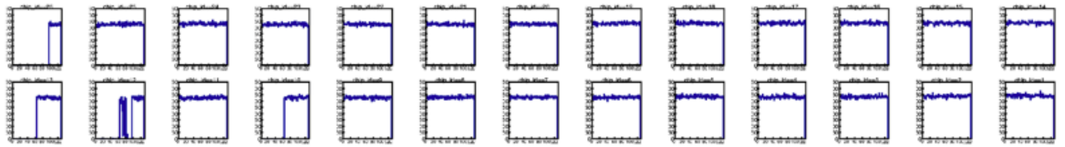
Fine



Data tagged as Fine.
300 entries / chip / channel obtained
while about 350 in good measurements.

lost channels



The only run with missing channels (20210712-2140).

Calibration tests without a bus extender

Setup

- Ladder: PPB2-L4S
- ROC, port: SW5, C3
- Conversion cable: small 8
- Bus extender: not used

Performance of ROC SW5 port C3

Quality / LVDS (mA)	Perfect	Fine	Bad/Dirty	Half entry, lost channels	Total
1	46 92%	2 4%	2 4%	0 0%	50 100%
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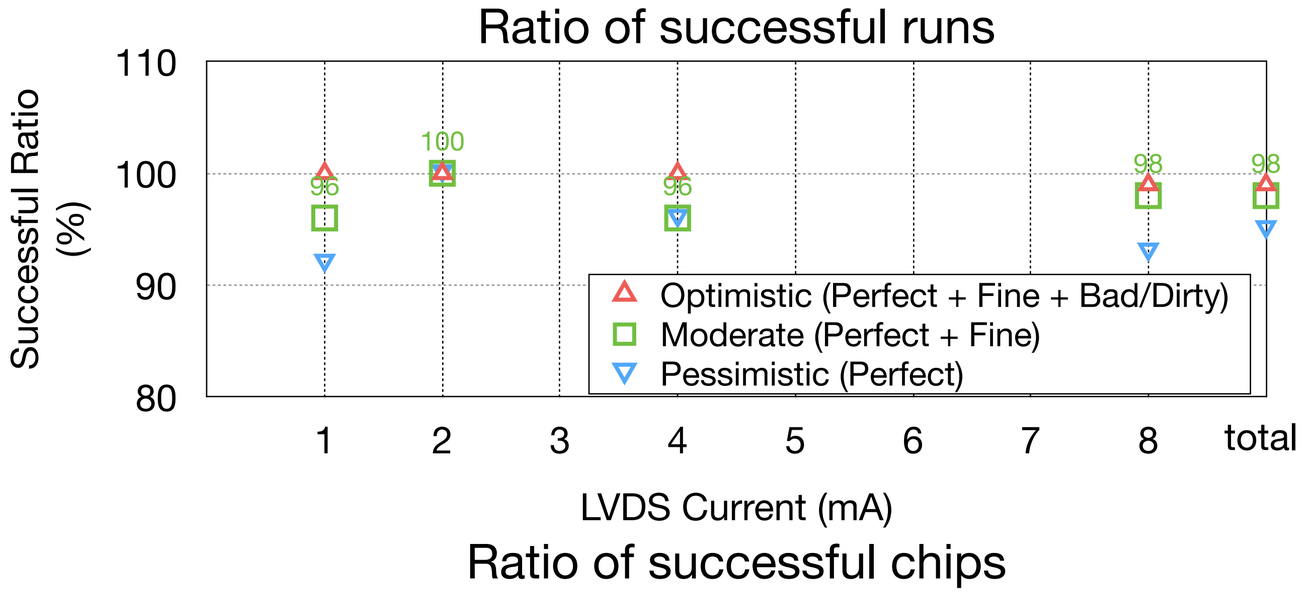

Calibration tests without a bus extender

Setup

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Performance of ROC SW5 port C3

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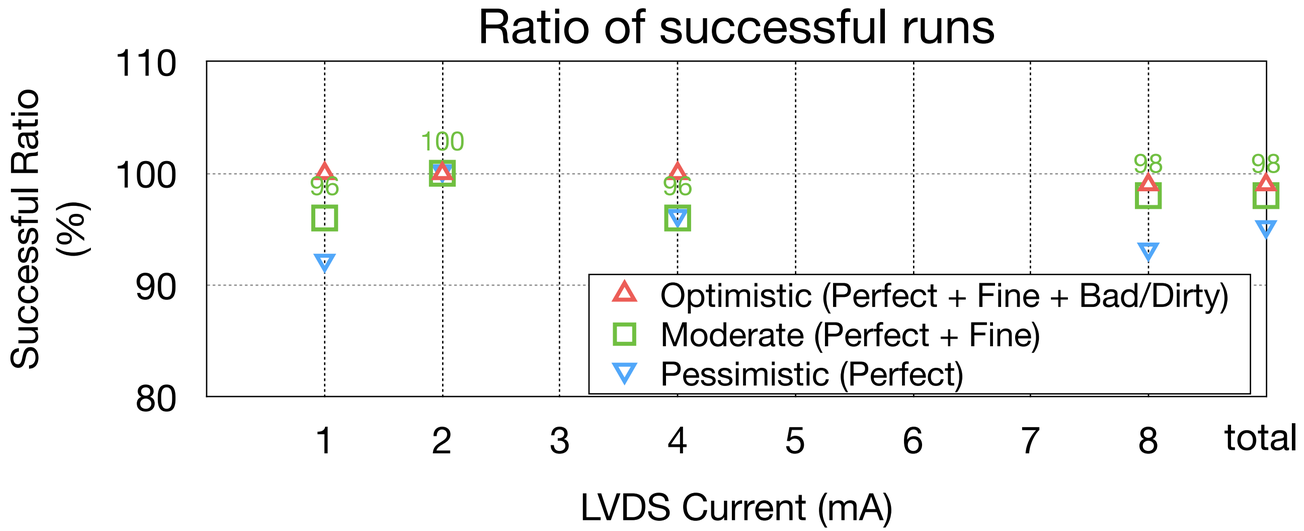
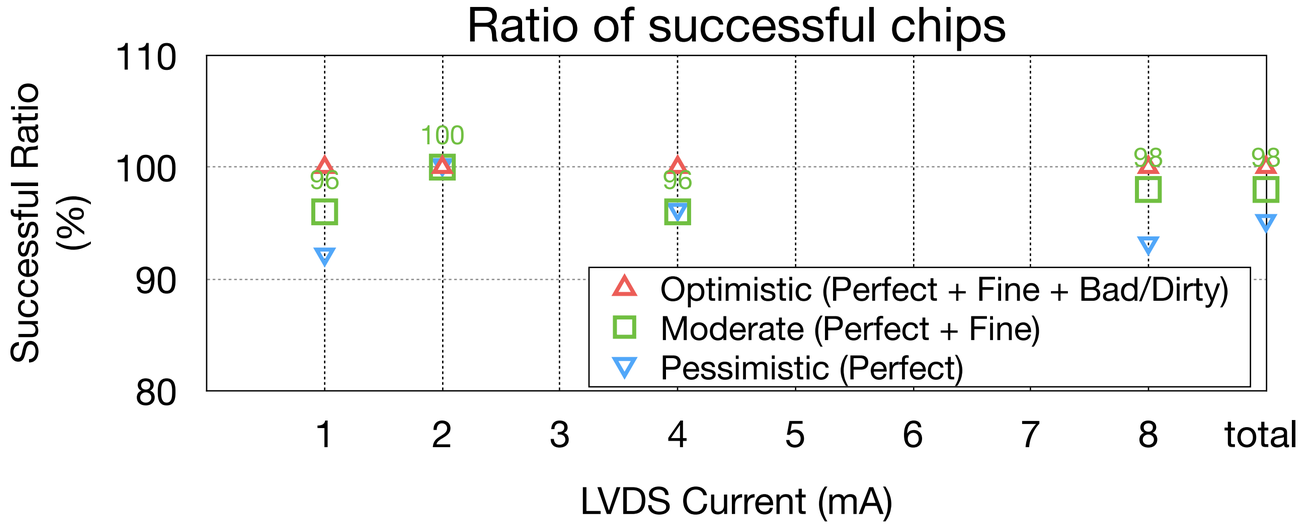
Total	244 95%	7 3%	5 2%	1 0%	257 100%

Performance of ROC SW5 port C3 (chip-wise)

Quality / LVDS (mA)	Perfect	Fine	Bad/Dirty	Half entry, lost channels	Total
1	1196 92%	52 4%	52 4%	0 0%	1300 100%
2	1404 100%	0 0%	0 0%	0 0%	1404 100%
4	1248 96%	0 0%	52 4%	0 0%	1300 100%
8	2496 94%	130 5%	26 1%	4 0%	2656 100%
Total	6344 95%	182 3%	130 2%	4 0%	6660 100%





Calibration tests without a bus extender

Setup

- Ladder: PPB2-L4S
- ROC, port: SW5, C3
- Conversion cable: small 8
- Bus extender: not used

Performance of ROC SW5 port C3

Quality / LVDS (mA)	Perfect	Fine	Bad/Dirty	Half entry, lost channels	Total
1	46 92%	2 4%	2 4%	0 0%	50 100%
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Performance of ROC SW5 port C3 (chip-wise)

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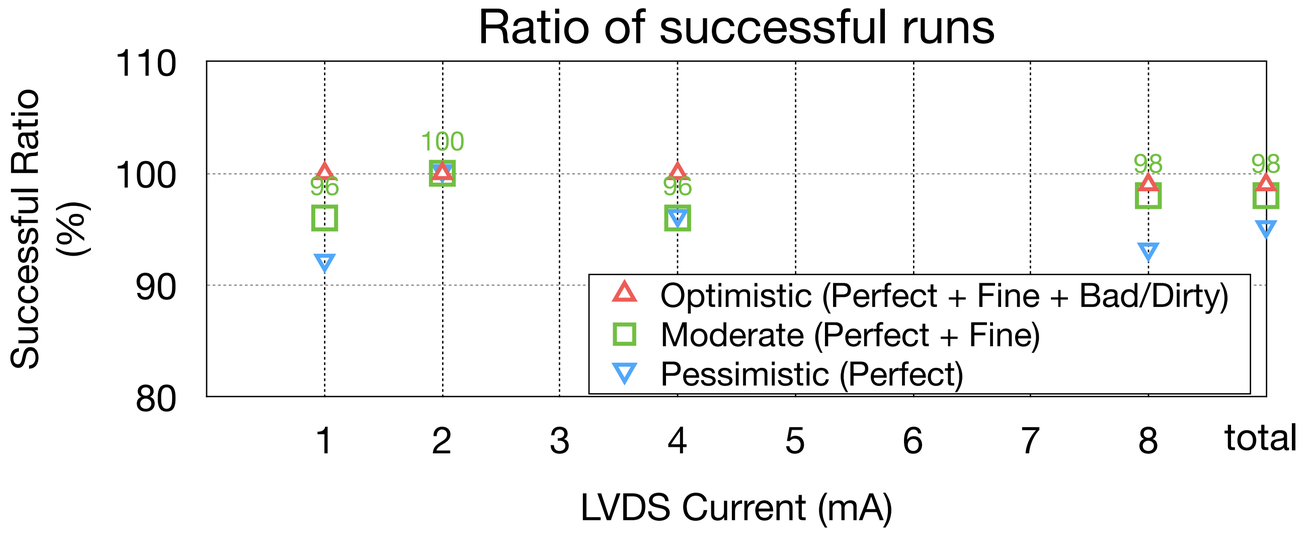
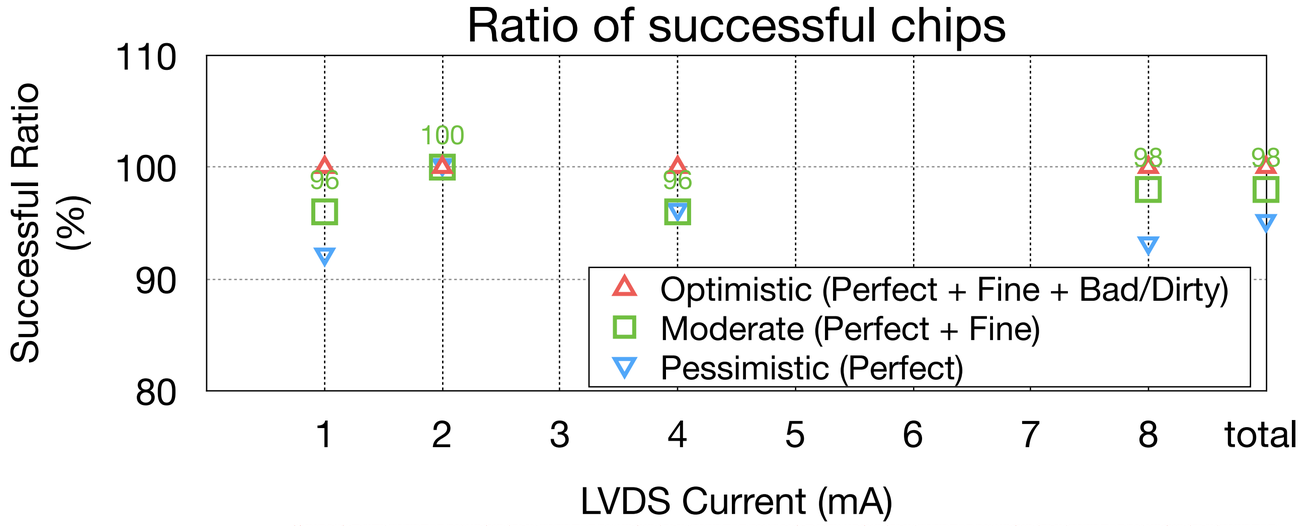




Very stable and reliable operation with the setup without a bus extender achieved.

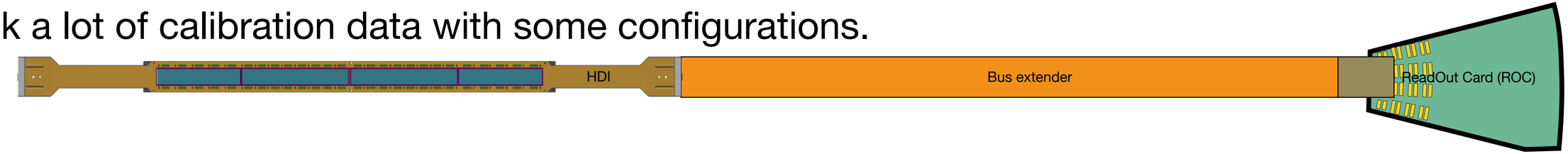
Ratios of successful runs and chips are independent from LVDS current.

Calibration tests with a bus extender

Performance of ROC ports without a bus extender

	A1	A2	A3	C1	C2	C3
7	Good except chip25	no data	Good except chip1-5	Good except chip15 1.2m Prepro4 (130)	Good	Good
NW1	no data	no data	no data	Good new2 (120)	Good new2 (110) 1.2m Prepro3 (40)	Good new2 (170) 1.2m Prepro4 (40)
SW5	Good	Good 1.2m Prepro3 (230)	Good	Good	Good	Good 1.2m Prepro3 (600)

We took a lot of calibration data with some configurations.



Calibration tests with ROC SW5 port-C3 and a bus extender

Setup

- Ladder: PPB2-L4S
- ROC, port: SW5, C3
- Conversion cable: small 8
- Bus extender: 1.2 m Prepro3

Ratio of successful runs with the bus extender (ROC SW5-C3)

LVDS (mA) \ Quality	Perfect	Fine	Bad/Dirty	Half entry	Total
1	17	3	0	45	65
	26%	5%	0%	69%	100%
2	46	3	0	17	66
	70%	5%	0%	26%	100%
3	100	2	1	12	115
	87%	2%	1%	10%	100%
4	152	9	0	3	164
	93%	5%	0%	2%	100%
5	109	4	1	1	115
	95%	3%	1%	1%	100%
6	13	0	0	1	14
	93%	0%	0%	7%	100%
7	14	1	0	0	15
	93%	7%	0%	0%	100%
8	60	4	0	0	64
	94%	6%	0%	0%	100%
Σ_4^8	348	18	1	5	372
	94%	5%	0%	1%	100%

Calibration tests with ROC SW5 port-C3 and a bus extender

Setup
- Ladder: PPB2-L4S
- ROC, port: SW5, C3
- Conversion cable: small 8
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Ratio of successful runs with the bus extender (ROC SW5-C3)

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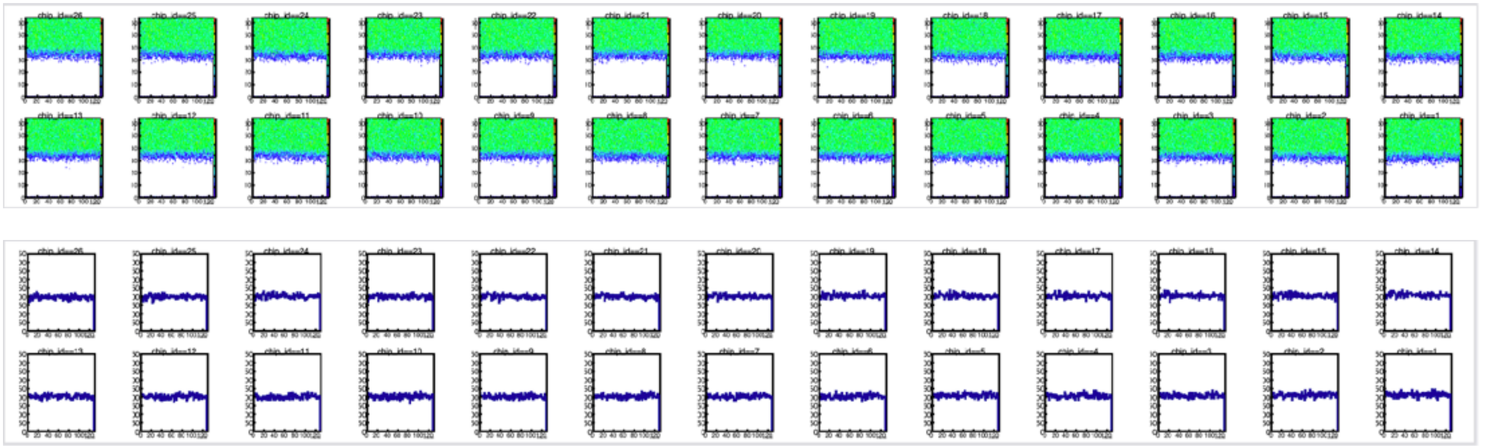
	94%	6%	0%	0%	100%
Σ_4^8	348	18	1	5	372
	94%	5%	0%	1%	100%

riken_fphx_raw_20210710-2136_0.dat (LVDS=5mA)



only ~200 entry/ch/chip（normally ~300 entry/ch/chip）was obtained

Calibration tests with ROC SW5 port-C3 and a bus extender

Setup

- Ladder: PPB2-L4S
- ROC, port: SW5, C3
- Conversion cable: small 8
- Bus extender: 1.2 m Prepro3

Ratio of successful runs with the bus extender (ROC SW5-C3)

LVDS (mA) \ Quality	Perfect	Fine	Bad/Dirty	Half entry	Total
1	17	3	0	45	65
	26%	5%	0%	69%	100%
2	46	3	0	17	66
	70%	5%	0%	26%	100%
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	87%	2%	1%	10%	100%
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	95%	3%	1%	1%	100%
6	13	0	0	1	14
	93%	0%	0%	7%	100%
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	93%	7%	0%	0%	100%
8	60	4	0	0	64
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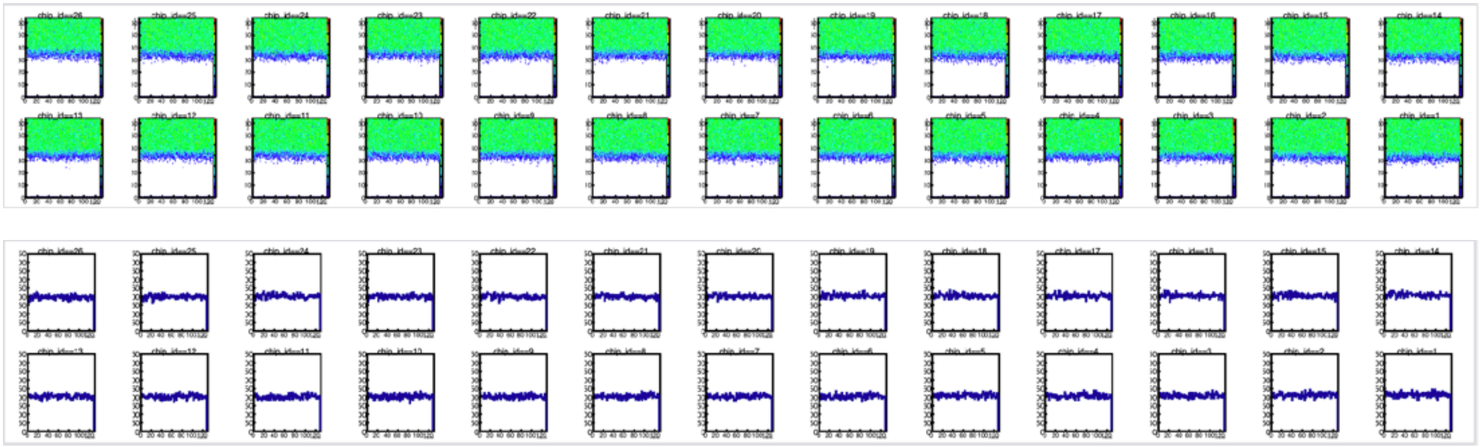
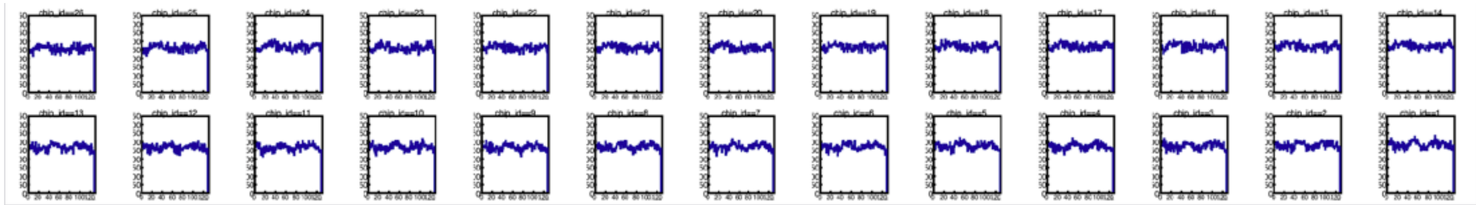
Σ_4^8	348	18	1	5	372
	94%	5%	0%	1%	100%

riken_fphx_raw_20210710-2136_0.dat (LVDS=5mA)



only ~200 entry/ch/chip（normally ~300 entry/ch/chip）was obtained

riken_fphx_raw_20210711-1113_0.dat (LVDS=3mA)



dists. are waving, only 250~300 entry/ch/chip was taken

Calibration tests with ROC SW5 port-C3 and a bus extender

Setup
- Ladder: PPB2-L4S
- ROC, port: SW5, C3
- Conversion cable: small 8
- Bus extender: 1.2 m Prepro3

Ratio of successful runs with the bus extender (ROC SW5-C3)

LVDS (mA) \ Quality	Perfect	Fine	Bad/Dirty	Half entry	Total
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	94%	6%	0%	0%	100%
Σ_4^8	348	18	1	5	372
	94%	5%	0%	1%	100%

Situation at NWU

Setup
- Date: Apri;/5/2021-April/6/2021
- Ladder: PPB2-L5N
- ROC, port: #9, C3 (2.8 & 3.0 V regulators)
- Conversion cable: large #3
- Bus extender: new2 (line for chip24 & chip26 shorten)
- LVDS: 7 or 8 mA (?)

#Runs: 60
Perfect: 49
Half entry: 11
#half entry chip: 15

Runs: 49 / 60 →82%
Chip : (49 ×24 –15) / (49 ×24) chips →99%

It’s not too bad, but the RIKEN testbench encounters less half entry phenomena than NWU’s. As far as I remember, operation with LVDS current less than 7 mA at NWU has so many half entry chips.

Calibration tests with ROC SW5 port-C3 and a bus extender

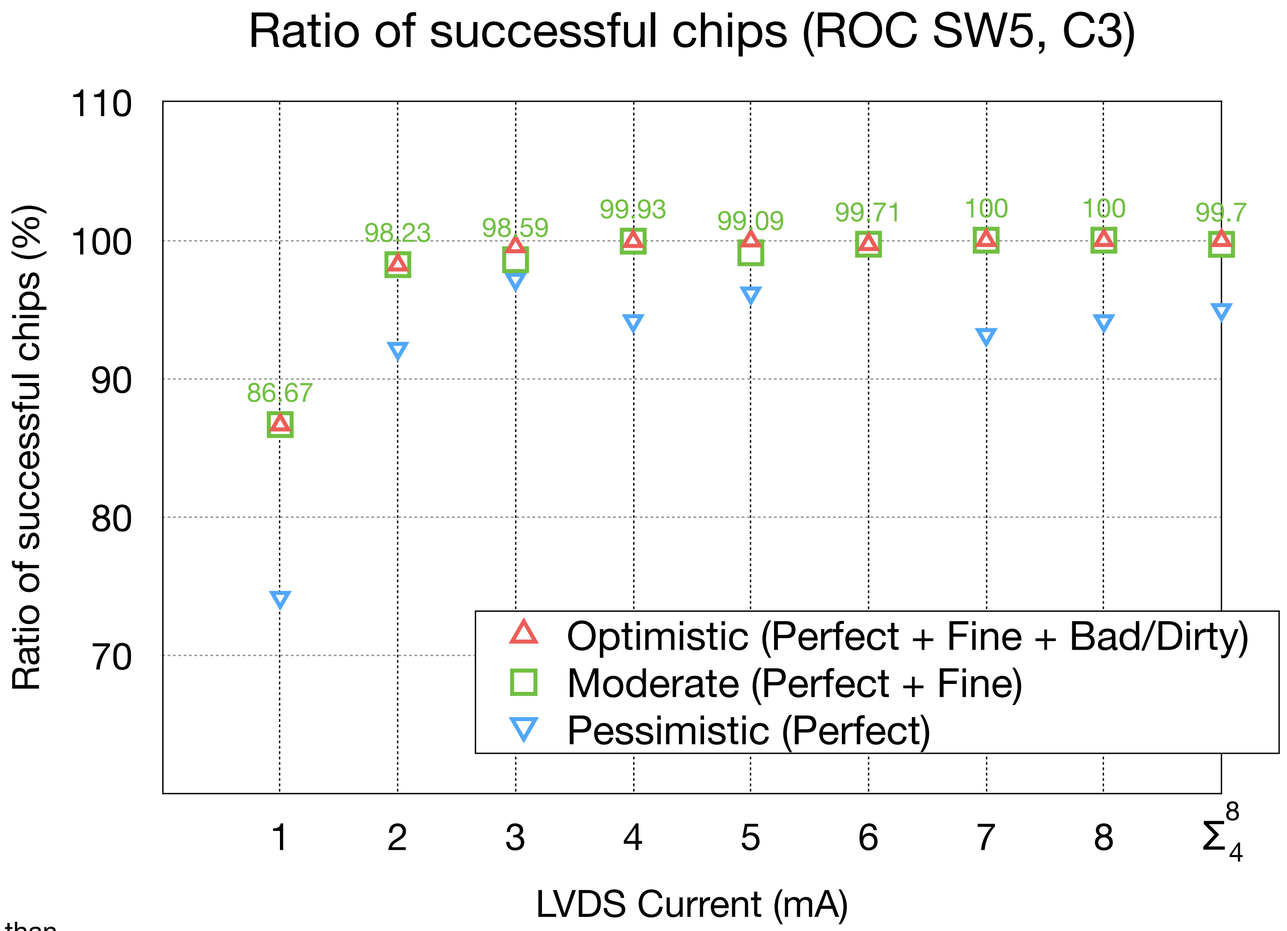
Setup

- Ladder: PPB2-L4S
- ROC, port: SW5, C3
- Conversion cable: small 8
- Bus extender: 1.2 m Prepro3

Ratio of successful chips with the bus extender (ROC SW5-C3)

Quality / LVDS (mA)	Perfect	Fine	Bad/Dirty	Half entry	Total
1	442	78	0	80	600
	74%	13%	0%	13%	100%
2	1196	78	0	23	1297
	92%	6%	0%	2%	100%
3	2600	52	26	12	2690
	97%	2%	1%	0%	100%
4	3952	234	0	3	4189
	94%	6%	0%	0%	100%
5	2834	104	26	1	2965
	96%	4%	1%	0%	100%
6	338	0	0	1	339
	100%	0%	0%	0%	100%
7	364	26	0	0	390
	93%	7%	0%	0%	100%
8	1560	104	0	0	1664
	94%	6%	0%	0%	100%
Σ_4^8	9048	468	26	5	9547
	94.8%	4.9%	0.3%	0.1%	100%

←more chips than 3 INTT barrels

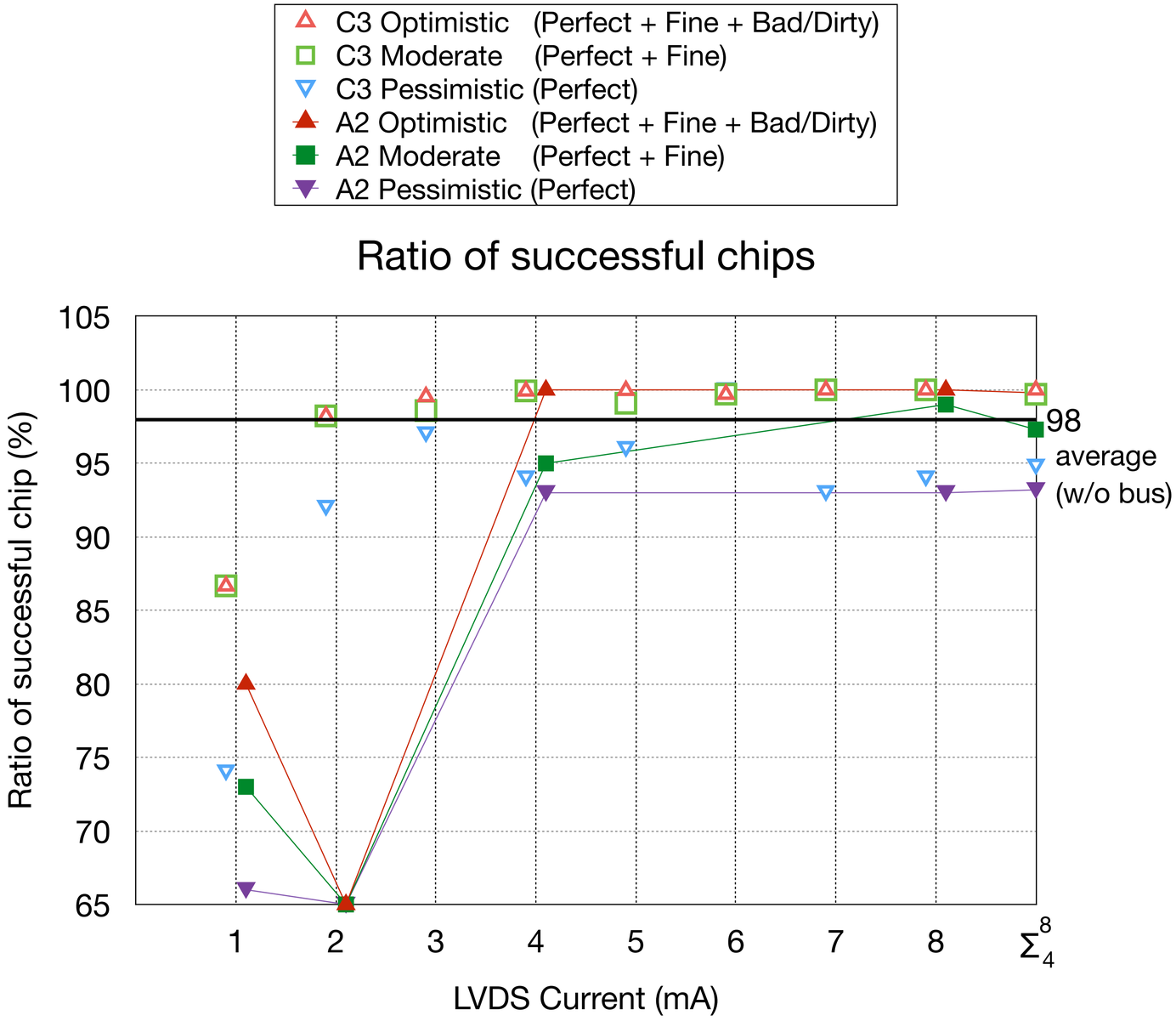


Calibration tests with a bus extender

Setup
- Ladder: PPB2-L4S
- ROC, port: SW5, A2
- Conversion cable: small 8
- Bus extender: 1.2 m Prepro3

Ratio of successful chips (ROC SW5, A2)

Quality / LVDS (mA)	Perfect	Fine	Bad/Dirty	Half entry	Total
1	234	26	26	70	356
	66%	7%	7%	20%	100%
2	156	0	0	83	239
	65%	0%	0%	35%	100%
3					
4	1092	26	52	5	1175
	93%	2%	4%	0%	100%
5					
6					
7					
8	1846	104	26	1	1977
	93%	5%	1%	0%	100%
4mA +8mA	2938	130	78	6	3152
	93.2%	4.1%	2.5%	0.2%	100%



Calibration tests with a bus extender

Setup

- Ladder: PPB2-L4S
- ROC, port: SW5, A2
- Conversion cable: small 8
- Bus extender: 1.2 m Prepro3

Ratio of successful chips (ROC SW5, A2)

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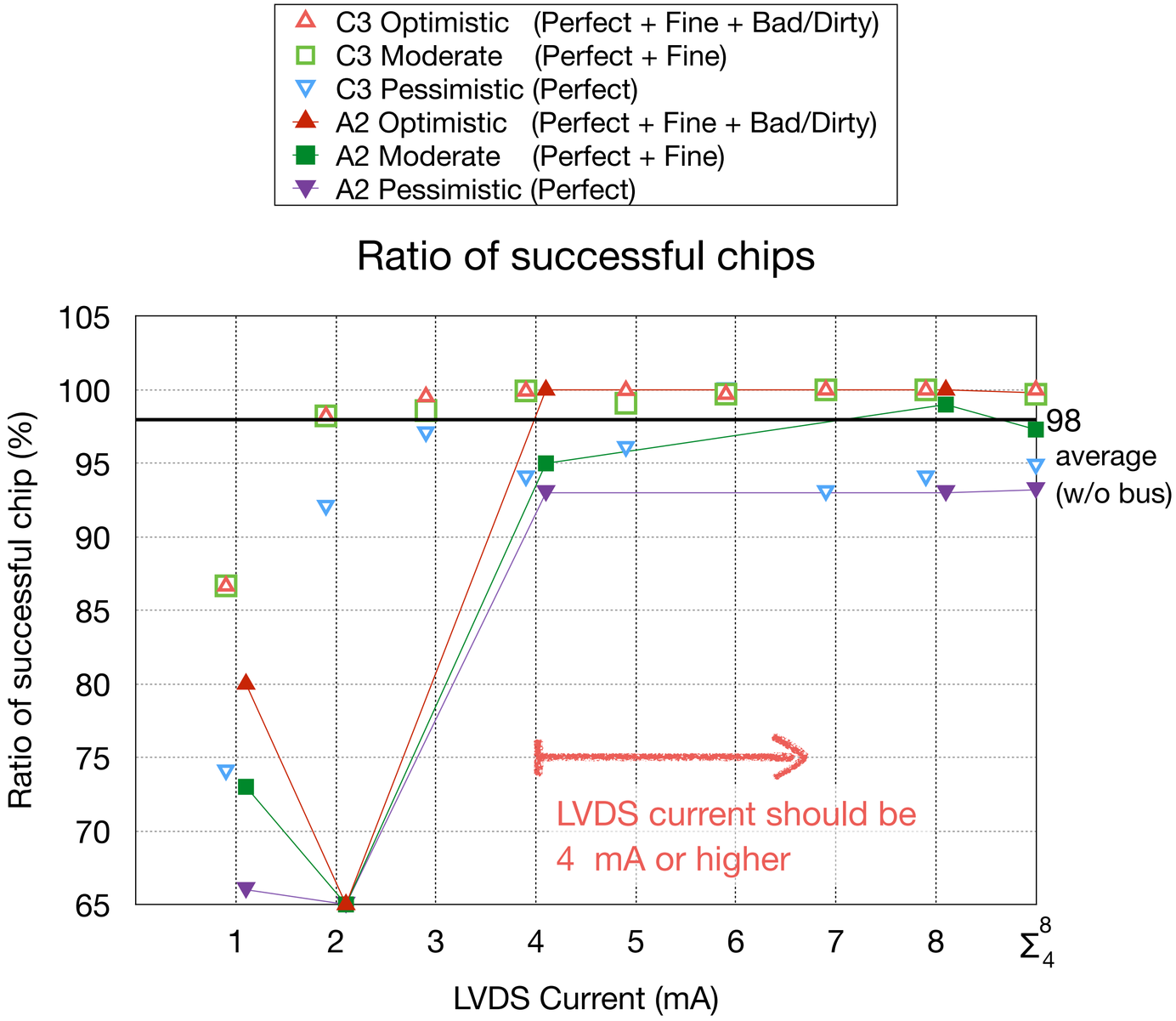
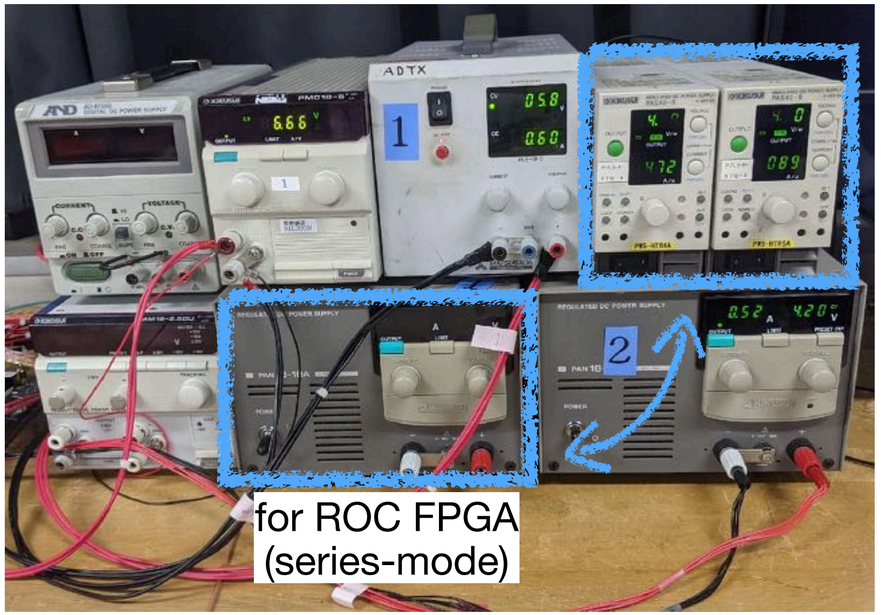


Difference b/w NWU and RIKEN testbenches and plans

Before starting RIKEN testbench, all components (FEM, FEM-IB, one of ROC(7?), conversion cable(s?), bus extender “new2”, cables for power supplies, optical fibers, bias cable) were transported to NWU, and calibration tests (maybe w/o?) a bus extender were performed. People didn’t find special differences at that time, so RIKEN testbench is basically the same as NWU’s. For the moment, we know the difference of power supplies for ROC FPGA at NWU (switching) and RIKEN (linear). Replacement of the linear power supply at RIKEN to switching one didn’t reproduce the half entry issue as NWU faces.

T. Kondo will come to RIKEN next week to measure eye-diagrams. T. Hachiya and I. Nakagawa are working for the FPHX readbacker and ROC FPGA. We may send NWU testbench to RIKEN for tests.



Power supplies
(switching-mode)

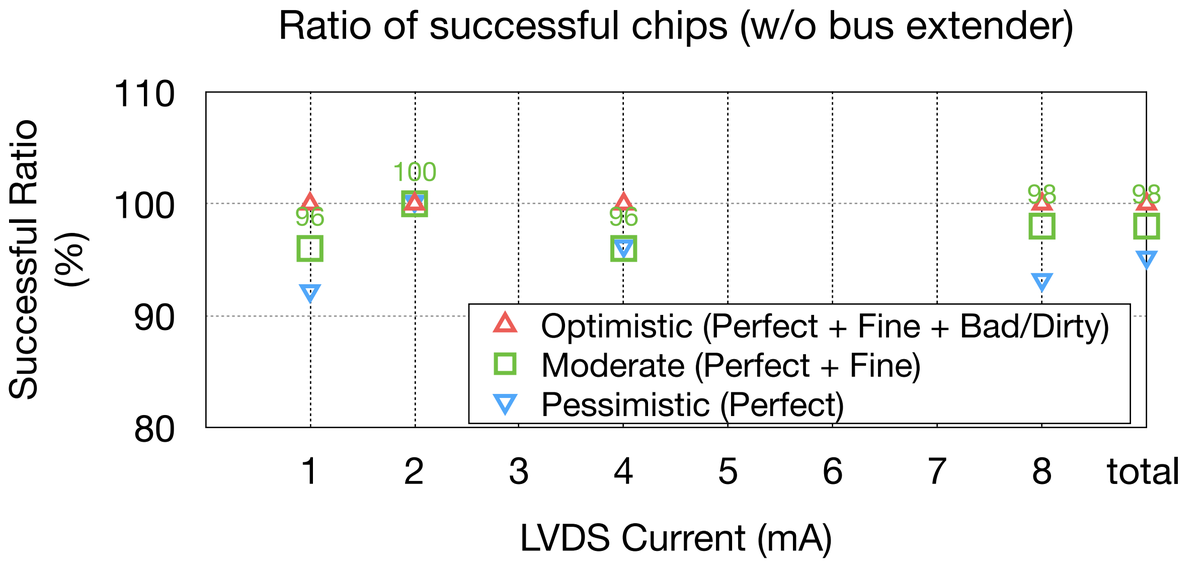
Summary

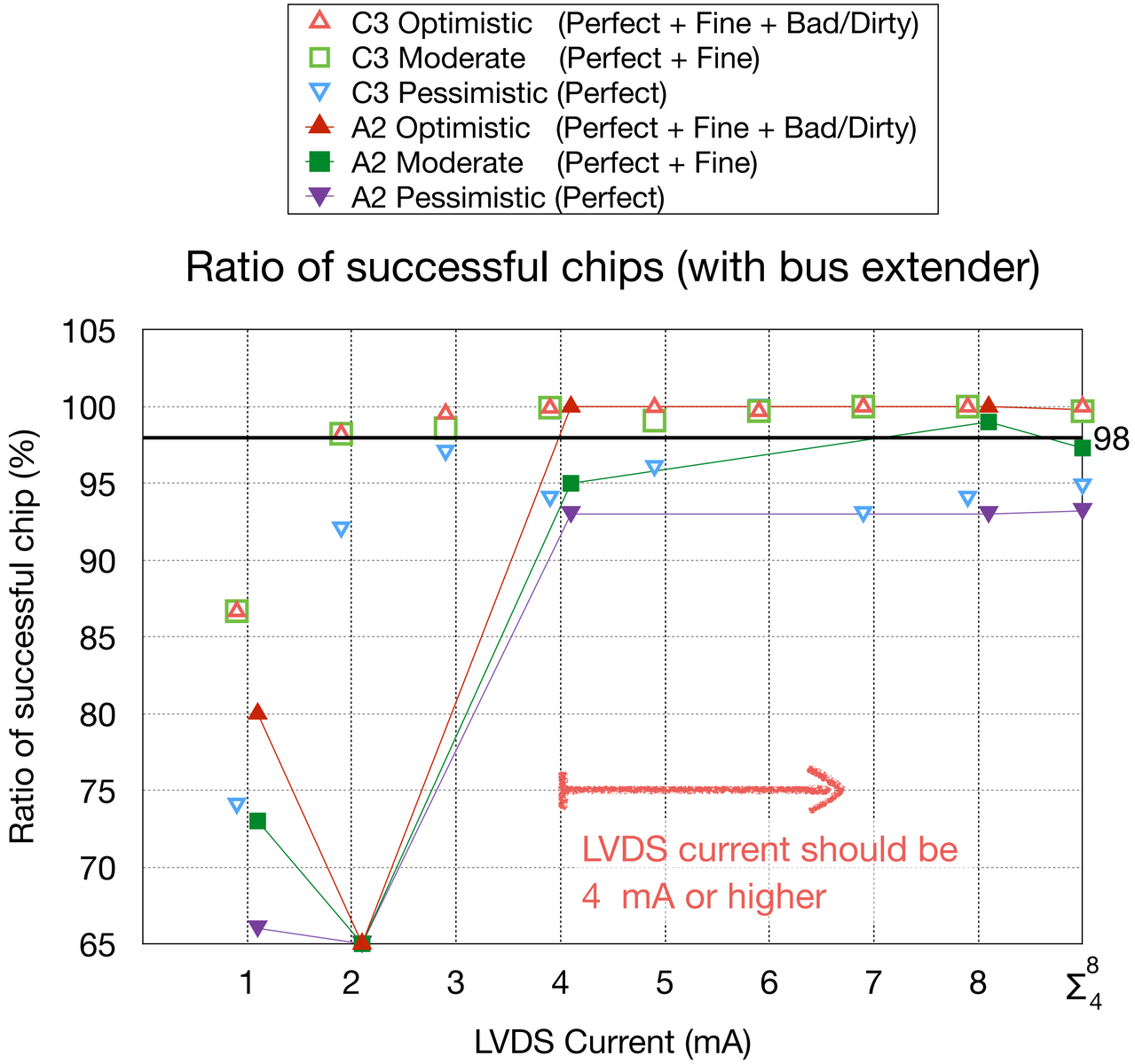
Calibration tests were performed very stably with various configurations.

Chips with only half entry rarely appear at RIKEN testbench about 0.1%. The issue may depends on a setup.

About 5% of chips have less data ~300 entries/ch than usual (350/ch).

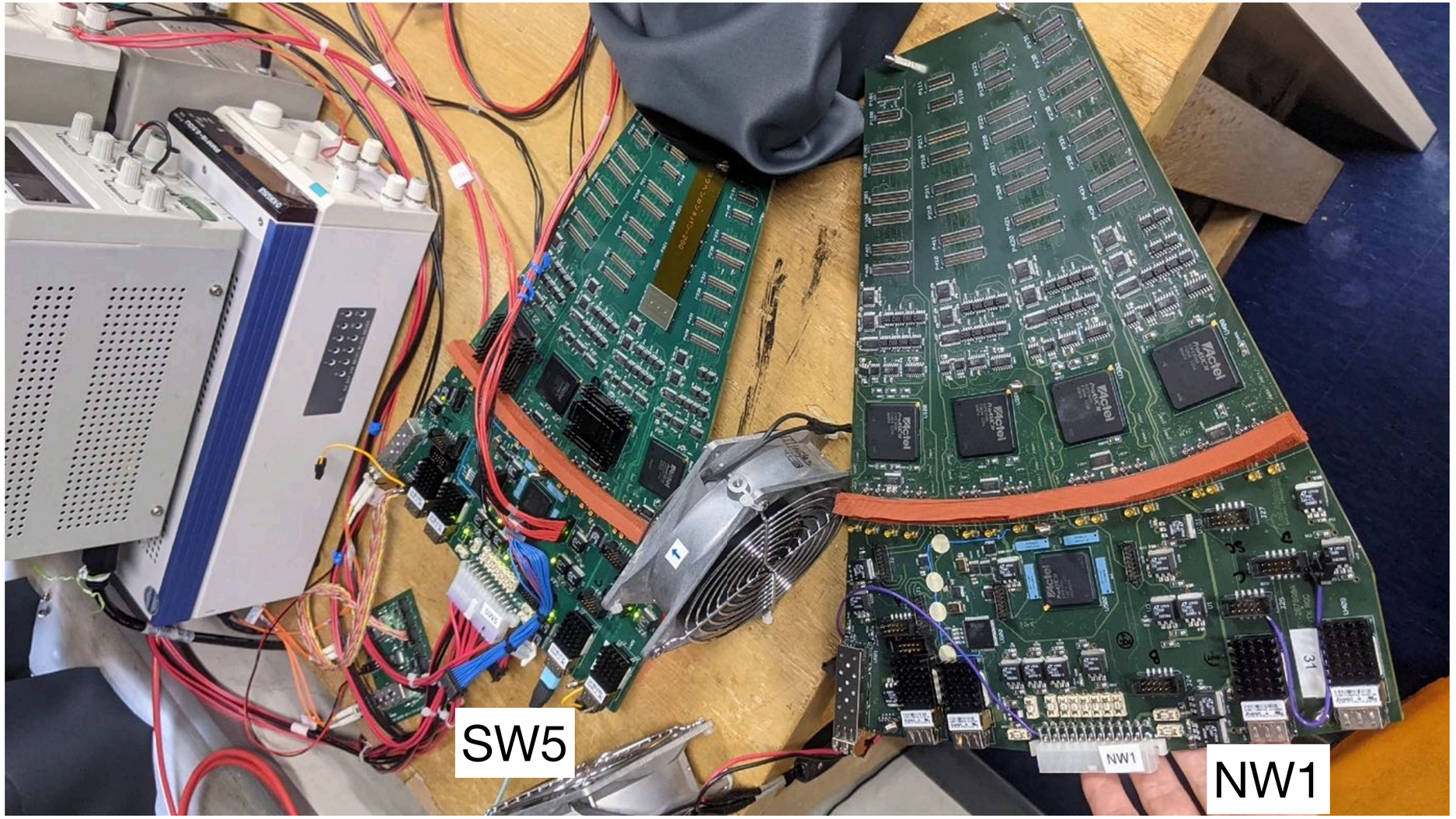
Further investigations are planned.



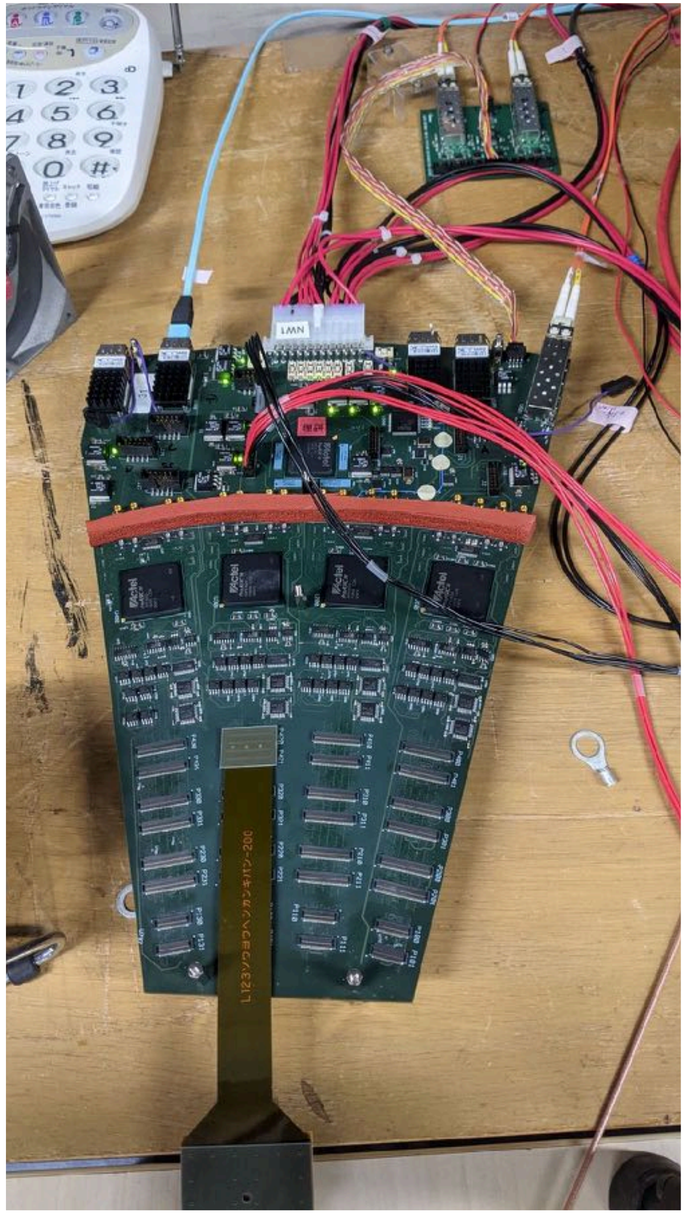


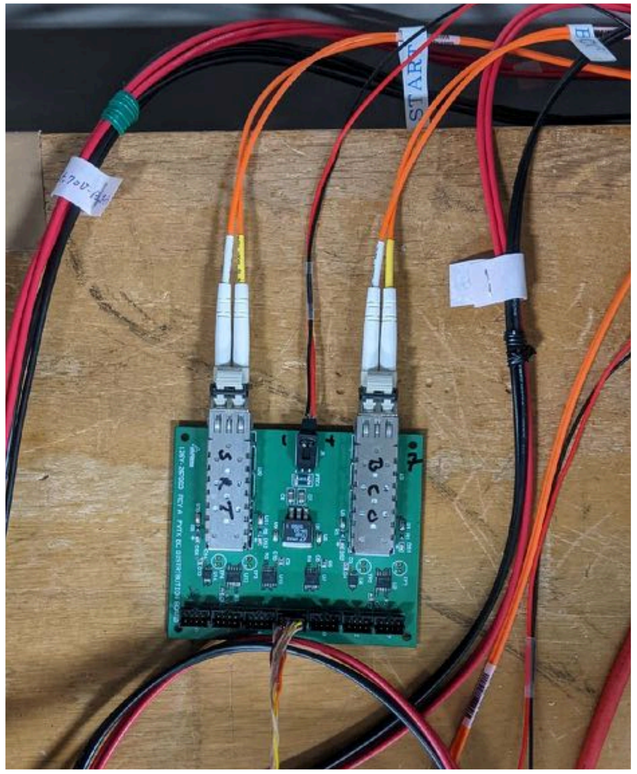
backup

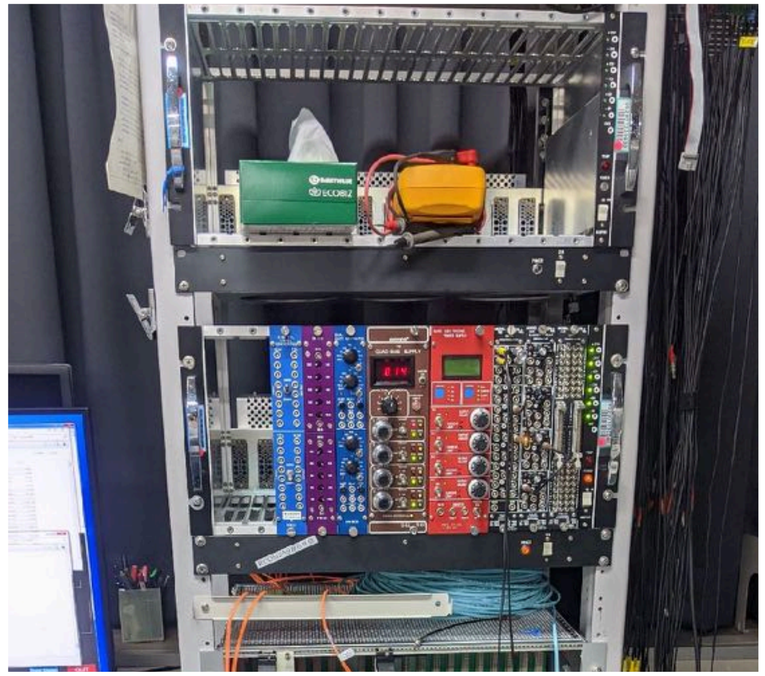
ROC SW5



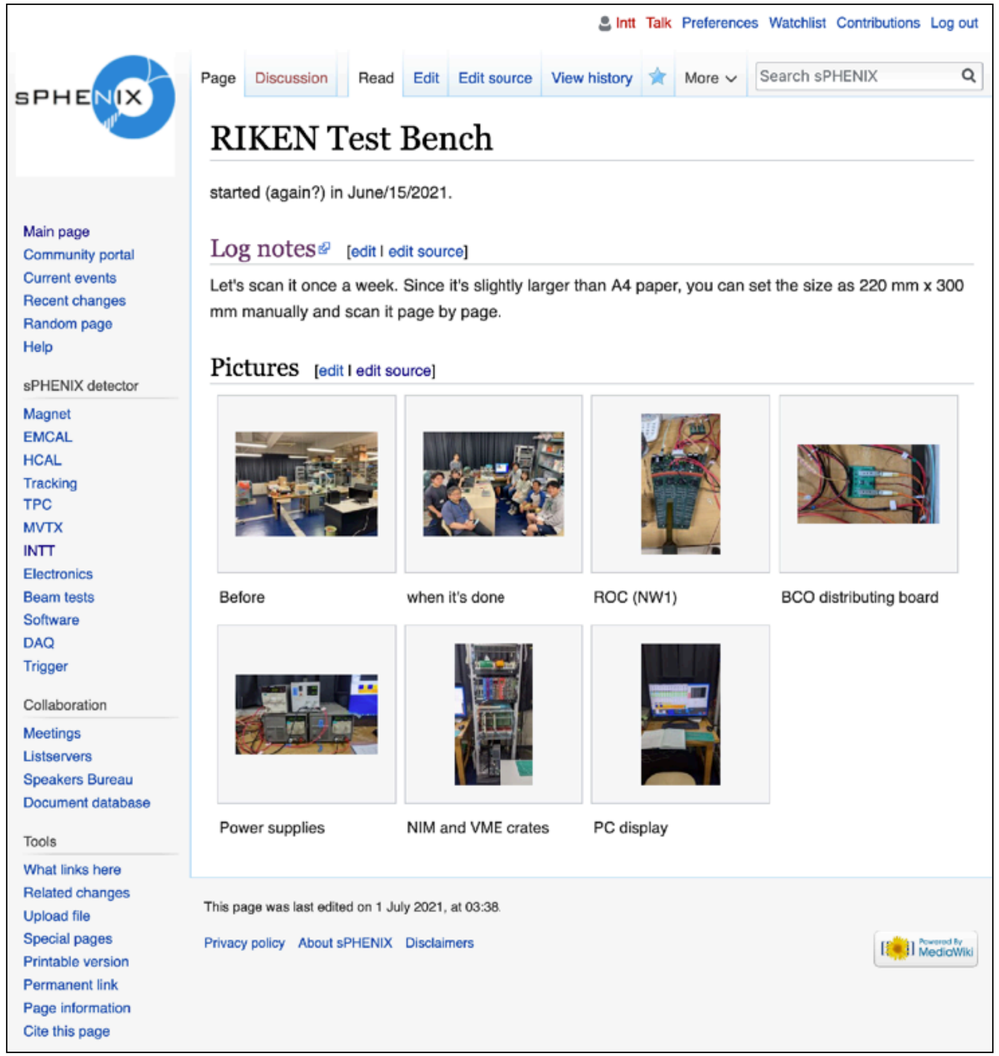
RIKEN testbench







sPHENIX wiki > INTT > RIKEN Test Bench



https://wiki.bnl.gov/sPHENIX/index.php/RIKEN_Test_Bench