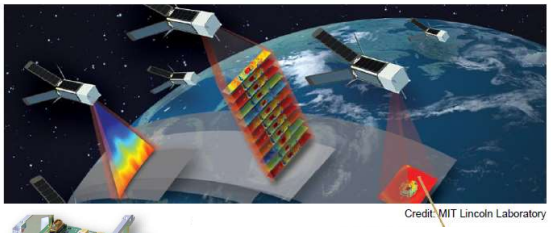
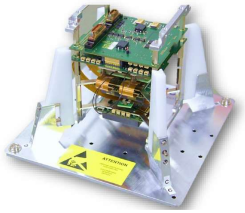
INTEGRATED CIRCUIT DESIGN @ ZEA-2

2021-04-28 | C. GREWING

ZEA 2: System Integration House

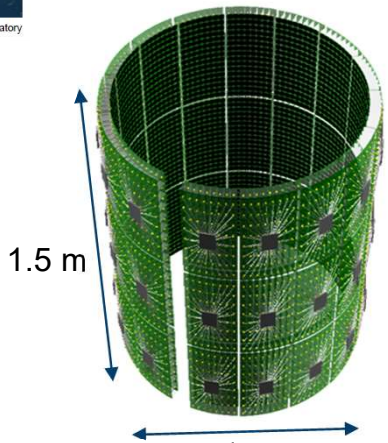
- Detector and Sensor Systems
  - Spectrometry for Atmospheric Measurement
  - Groundpenetration Radar
  - Lysometer Development
  - Medical and Biological Instrumentation
  - Detector Development
    - Analog and Digital SiPM
    - Wavelength Shifting Fiber
    - Strawtubes
    - PMT
- 2010 Start of IC Development



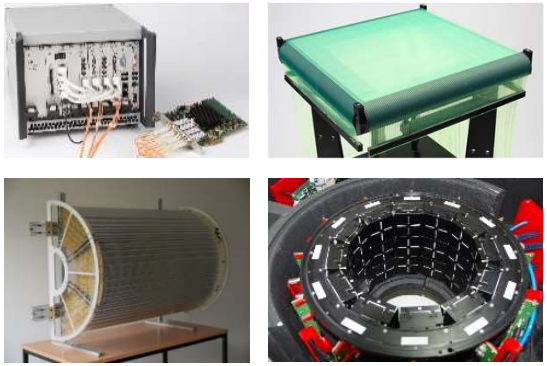


AtmoLite: Spectrometer for CubeSat

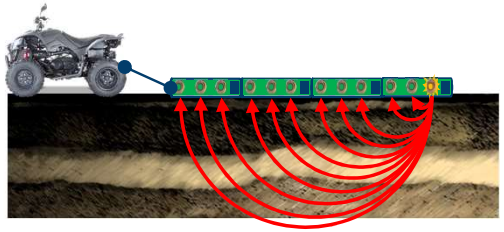
iNode: Medical and Biological research



Lysometer Development



Detector Development TEA2



Ground Penetration Radar

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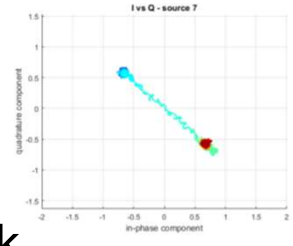
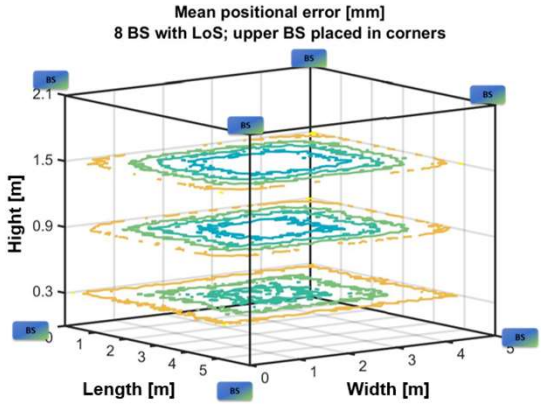
INDOOR POSITIONING SYSTEM

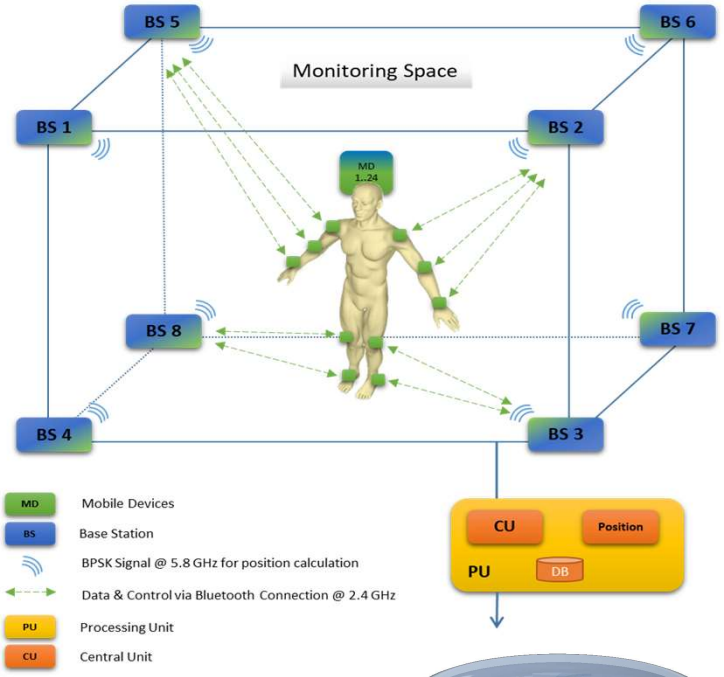
5 Patents

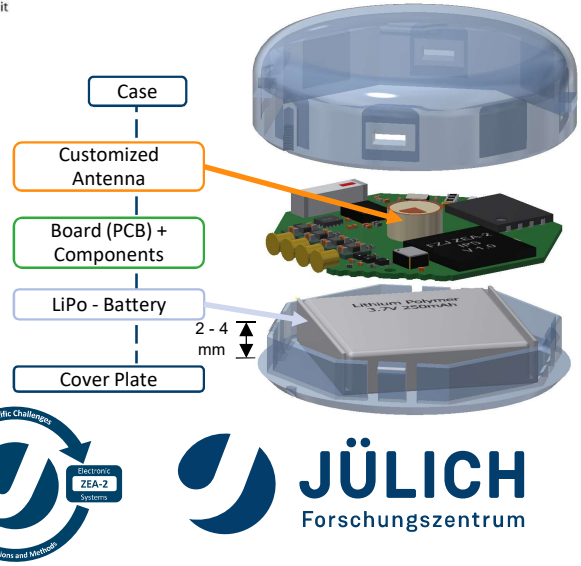
Full System Development of a Proprietary Concept: Resolution<1mm



- Based on a PHD Thesis
  - System Modell in MatLab / Simulink
- TDOA Estimation DSP in Simulink
  - Virtual Oversampling with 1ps Resolution
- 65nm Syperheterodyn Transceiver at 5.7GHz
  - Fully Integrated FE
  - Polyphasefilter with 50MH Bandwidth
  - ADC 12 bit at 350MHz
  - Integrated PLL
- Systemintegration and Verification
  - In House Absorber Chamber Measurements







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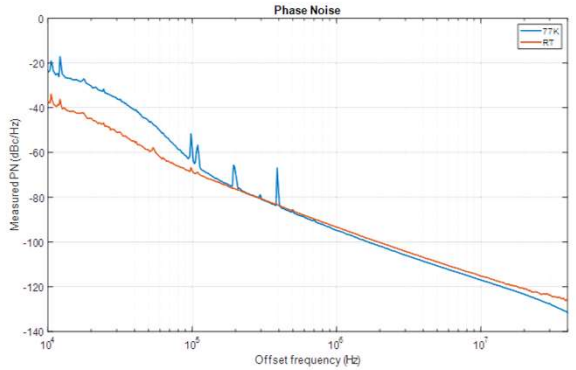
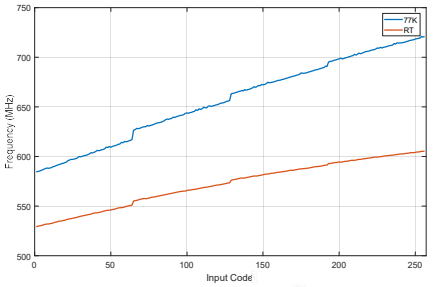
ELECTRONICS FOR QUANTUM COMPUTING

Development of Scalable Control and Readout System for Qubits at Cryogenic Temperatures

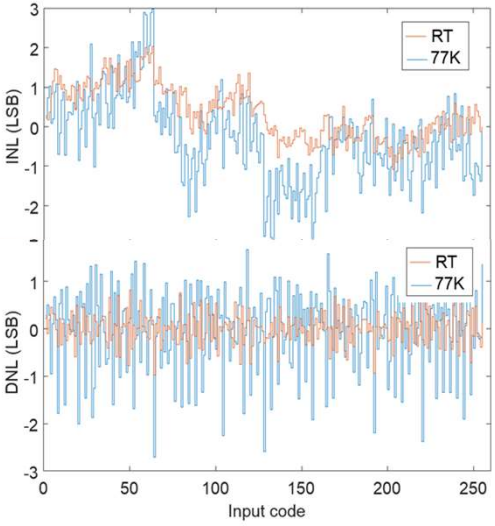
- System View:
  - Development of Qubit models
  - Error Correction Algorithms
- Concept and 22nm SOI Design:
  - Bias DAC
  - Control DAC
  - RF Frequency Control
  - RF Control DAC
  - Bias and Power Control
  - Readout Circuit

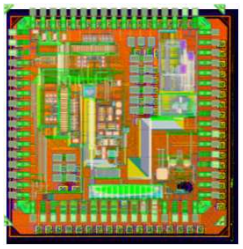




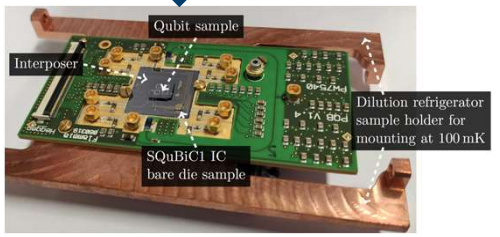
DCO

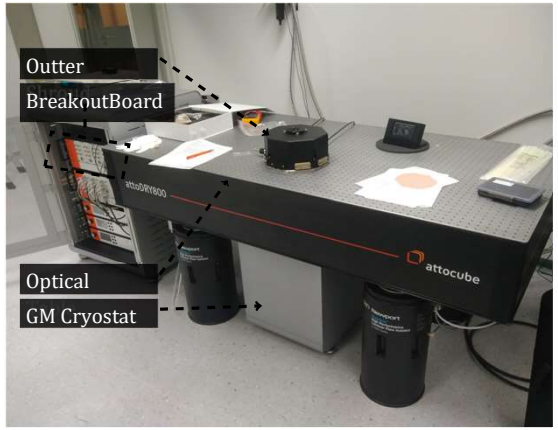
Pulse DAC





SCUBIC1



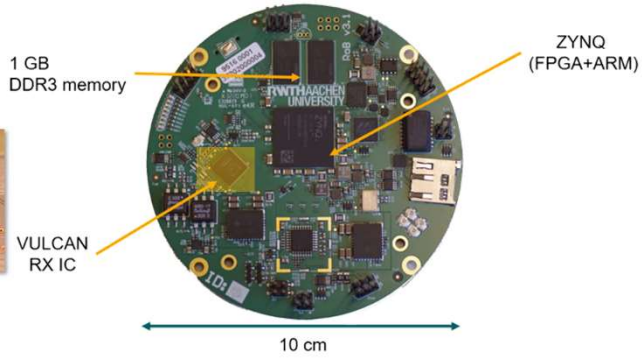


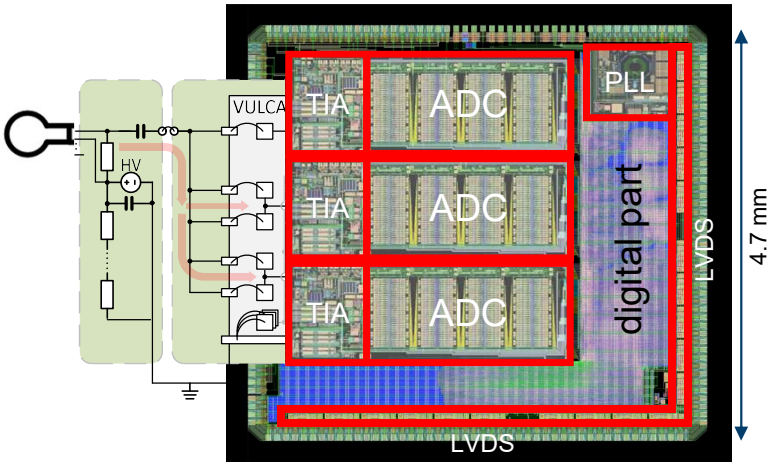
Attocube atto DRY800 cryostat

DETECTOR IC: VULCAN – AN ADC SOC FOR JUNO

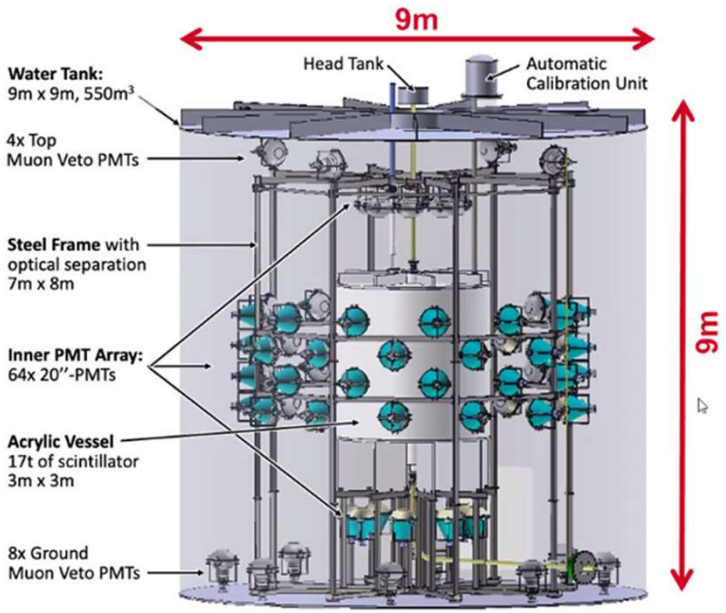
Electronics Submerged with PMT

- Lower Bandwidth on the Cable
- Precise Signal Reconstruction
- No Analog Delay Line
- Control Loop to Suppress DC Variations
- Optional Overshoot Compensation





Vulcan: Son of Juno in ancient Greek mythology



Key Parameter of Vulcan	
Process	65 nm CMOS
Active Area	22 mm²
DSP w/ # Transistors	7 Mio
Power	~ 1.2 W
Input Impedance	< 10 Ohm
Input Bandwidth	500 MHz
Sampling Rate	1 GSample/s
Integrated Sigma Delta PLL	4GHz VCO
Dynamic Range	80 dB
ADC Resolution	3× 8 bit
High Gain	0.06 p.e./bit
Medium Gain	0.4 p.e./bit
Low Gain	8 p.e./bit

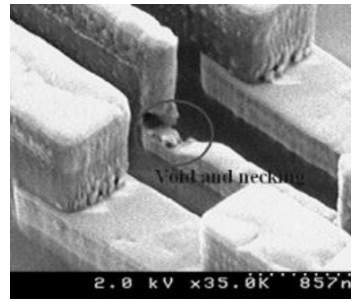
Reliability of Integrated Circuits

Manufacturing defects due to process variations

- **Strong defects**: non-operational transistors or wires
  → immediate impact on functionality
- **Weak defects**: weakened wire wear out with time
  → fails with stress on circuit

Prevent by design methods
- Use wider/multiple conducting wires
- Use multiple vias instead of single vias

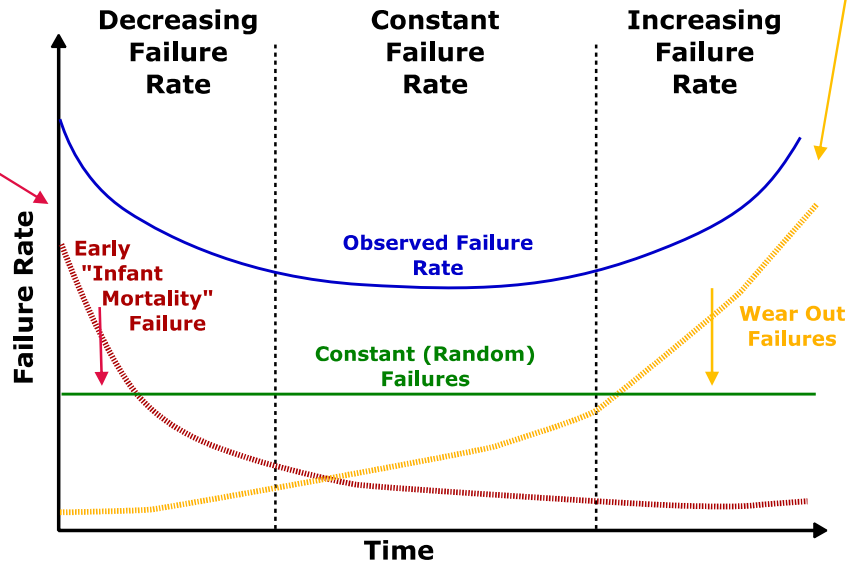
Electromigration studies prior tapeout

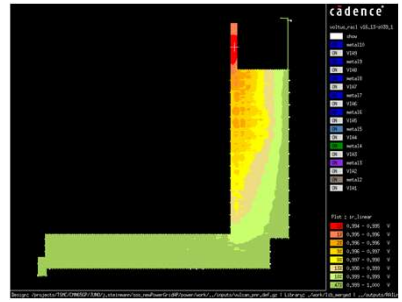


Degredation through electromigration

Suppressing infant failures

- **Test key parameters**
  - PLL frequency, oscillator voltage
  - DAC: INL / DNL
  - ADC: Offset and gain errors…
- **Best samples**, targeted ratio 30%





IR drop simulation digital part of Vulcan

Similar procedure as in automotive industry for reliability assurance

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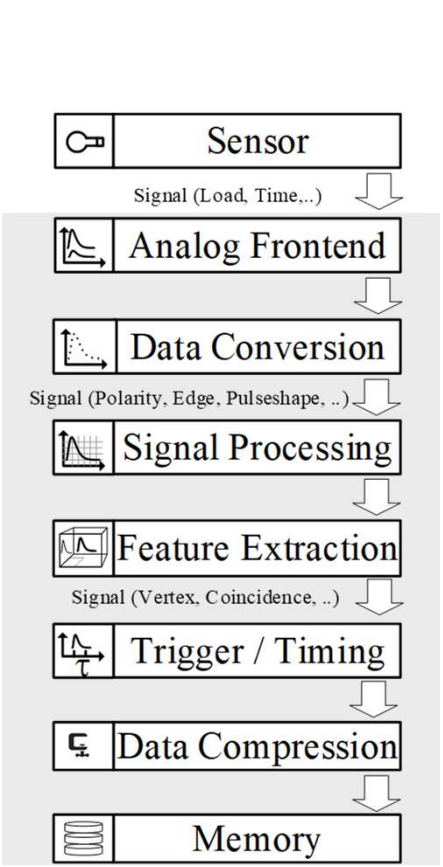
ZEA 2: SYSTEM INTEGRATION HOUSE

- We Can Work On Whole Signalchain: e.g. Sensor to DAQ
- We Have ***Strong Experience*** In:
    - Hardware Development
    - Chip – IC Development
    - Signal Processing
    - Data Management
    - Highspeed Data Transmission System
    - Modeling and Top-Down Development
    - ***Our Main Interests are ASIC and Signal Pre-Processing***
- We Think We Need to be ***Involved in the System Concept***.

SIGNAL FEATURE EXTRACTION HUB SOC

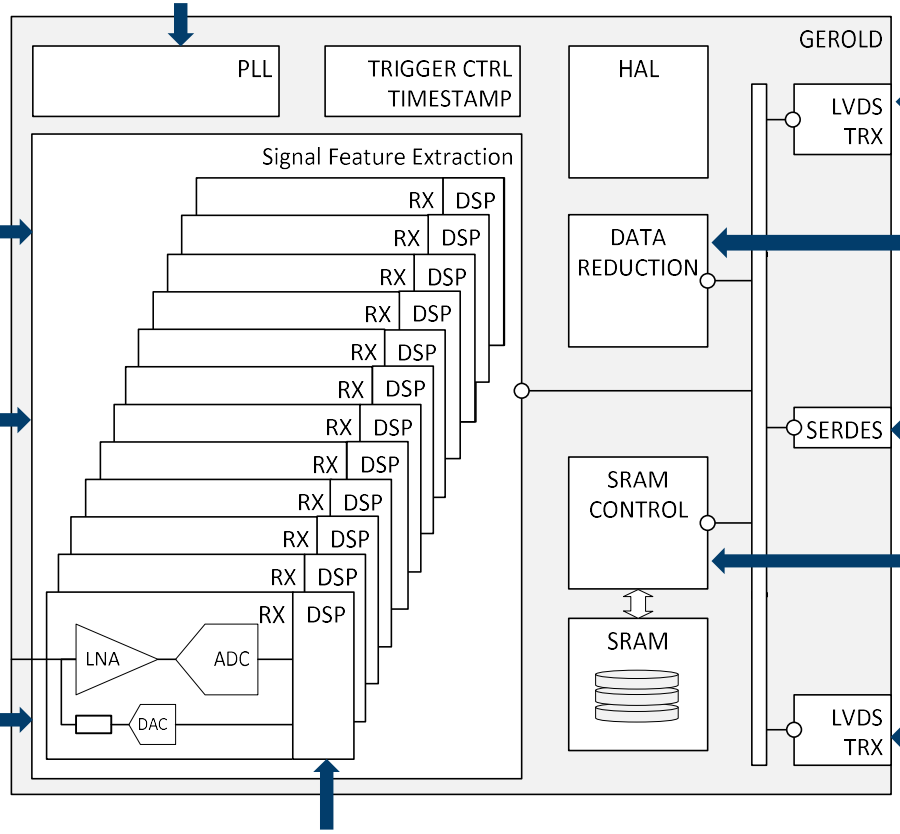


Internal Clock Generation

32 ADC in One ASIC, Variable to Combine for Higher Clock or ENOB

Programmable Input Impedance <10 – 100Ohm

Programable Bias Built-in Self Test



LVDS Interface to Link Up with Other IO

Data Ordered by Timestamp and Zerosuppression

Highspeed Interface to Optical Converter for up to 100m Data Upload

Built in SRAM Memory to Lower Bandwidth Requirement to Average

LVDS Interface to Link Up with Other IC

Calculation of TOA, Feature Extraction: Wavelet, TOT, Number of Hits,…

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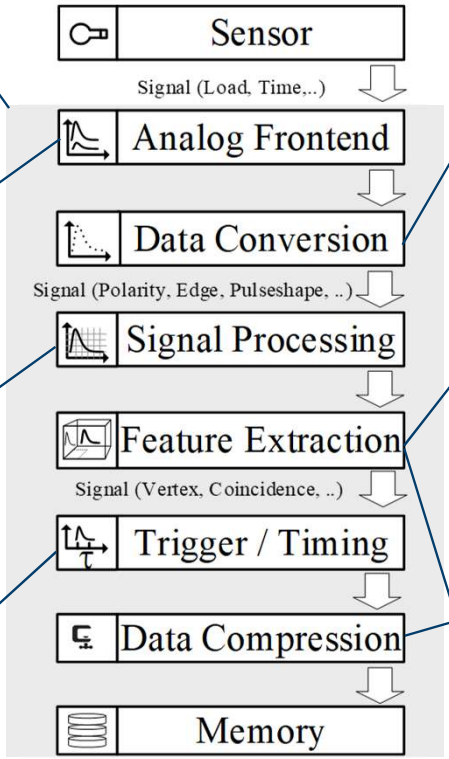
DETECTOR SYSTEMS ROADMAP

WOM based Ship Background Tagger
Prof. Bretz, RWTH Aachen, Physics

Stilbene Crystal Camera
Prof. Pooth, RWTH Aachen, Physics

SHiP Strawtube Tagger
Prof. Dieck, Uni Freiburg

Integrated TDC for Scalable Digital Silicon Photomultipliers
Prof. Heinen, RWTH Aachen, Electronics



Next Generation ADC
Prof. Czylwik, Uni Duisburg-Essen

Prototype RX based on PDPC for LS experiments,
Prof. Wurm, Uni Mainz and Prof. Lachmayer, Uni Tübingen

SHIP: Generic, ASIC based Receiver Electronic (GRX)
Prof. Fischer, Uni Freiburg
Prof. Lacker, TU Berlin

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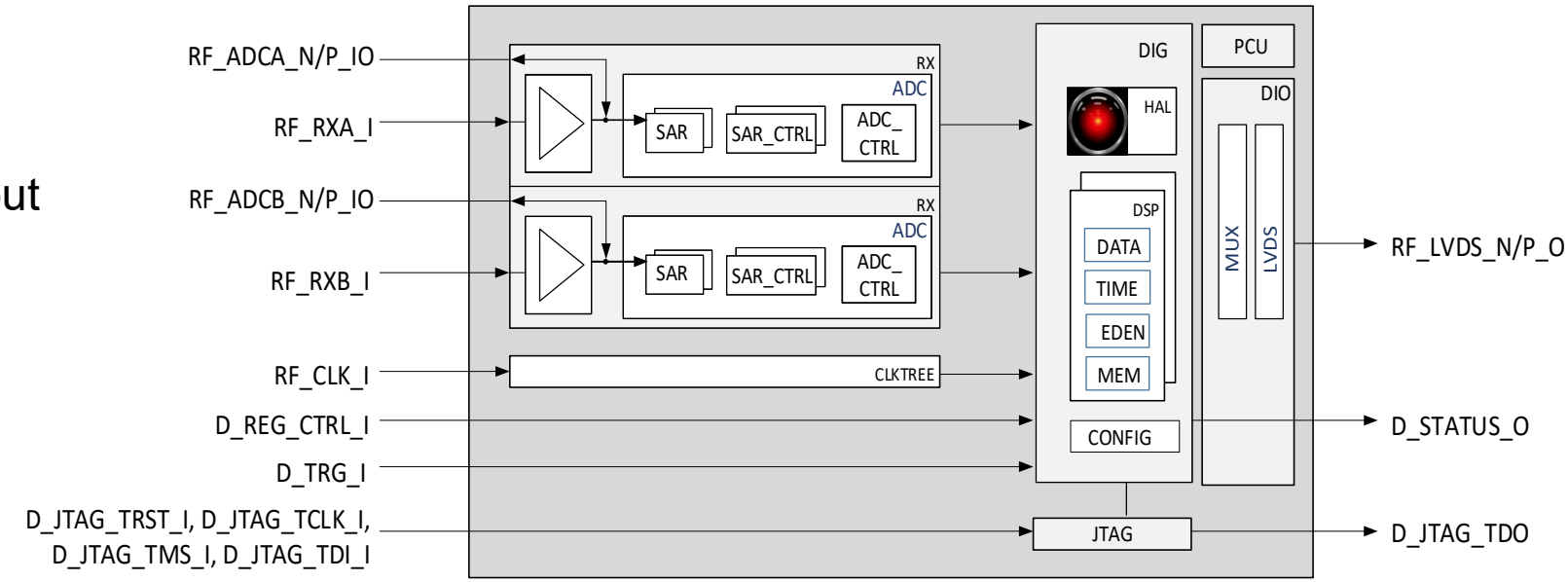
TAPE OUT Q1 2022:

- Configurable ADC:
- 9bit / 12 bit
- 250Mb/s / 1Gb/s
- Input Impedance
- Voltage / Current Input

- Internal Memory
- Trigger Input

- External:
- PLL
- PCU



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Framework to develop top down Data Processing