

Universita' di Trieste and INFN Trieste Contributions to EIC SC

- Past/current activities within ITS3
- Plans

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EIC Silicon Consortium meeting – July 26th 2021

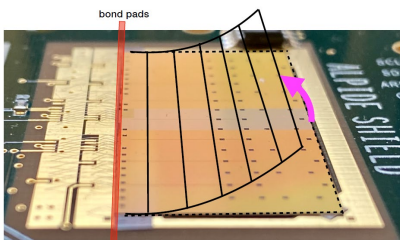
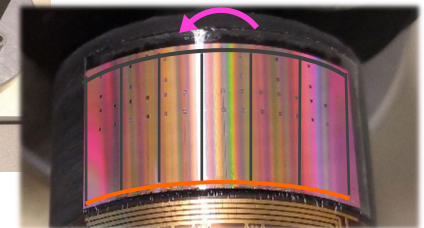
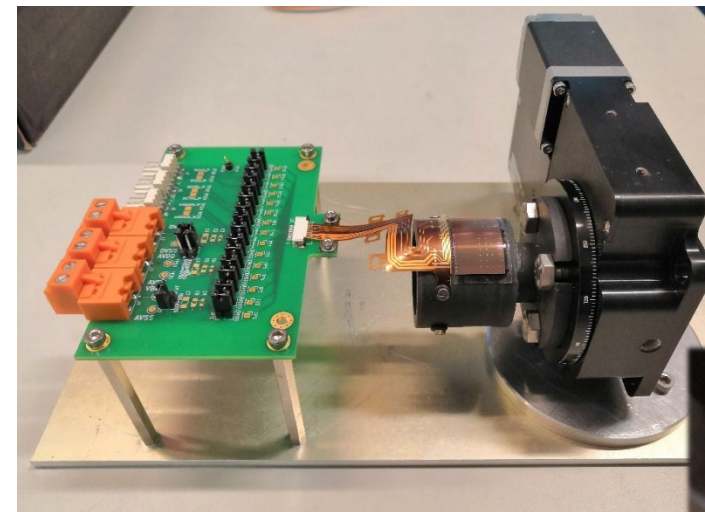
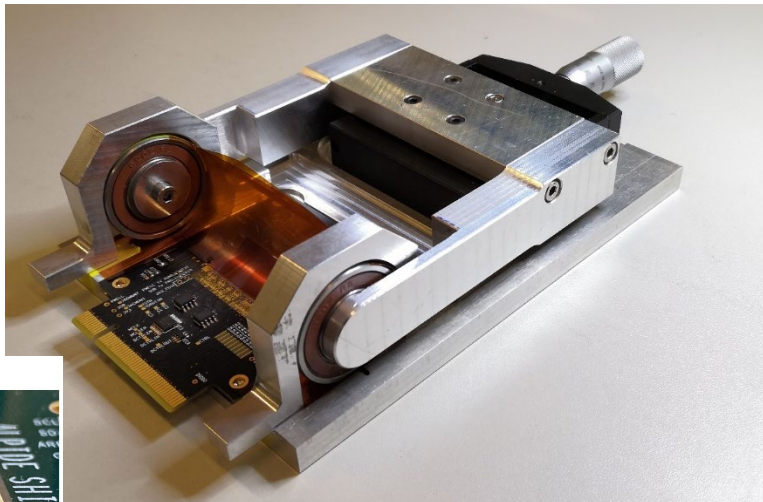
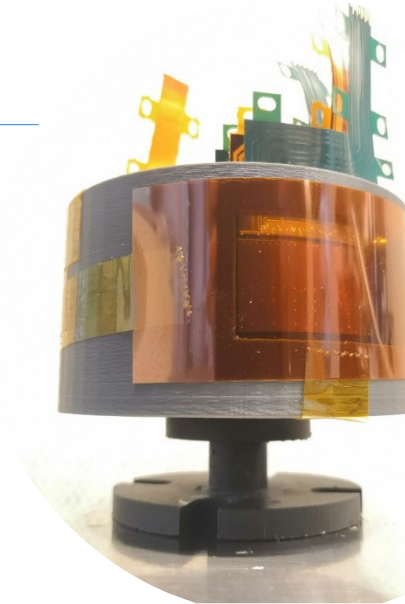
Past/current activities - 1

Pixel sensor bending

First bending development

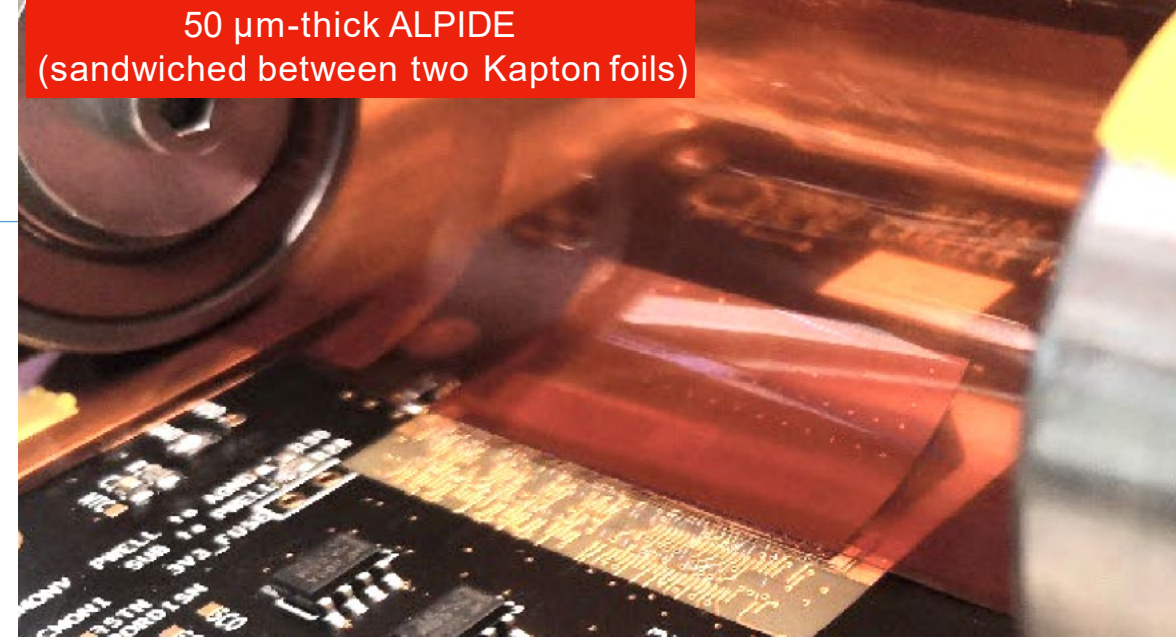
Design and production of sensor bending tools

- Prototyping of bending tools for existing sensors
- Bent sensor surface description

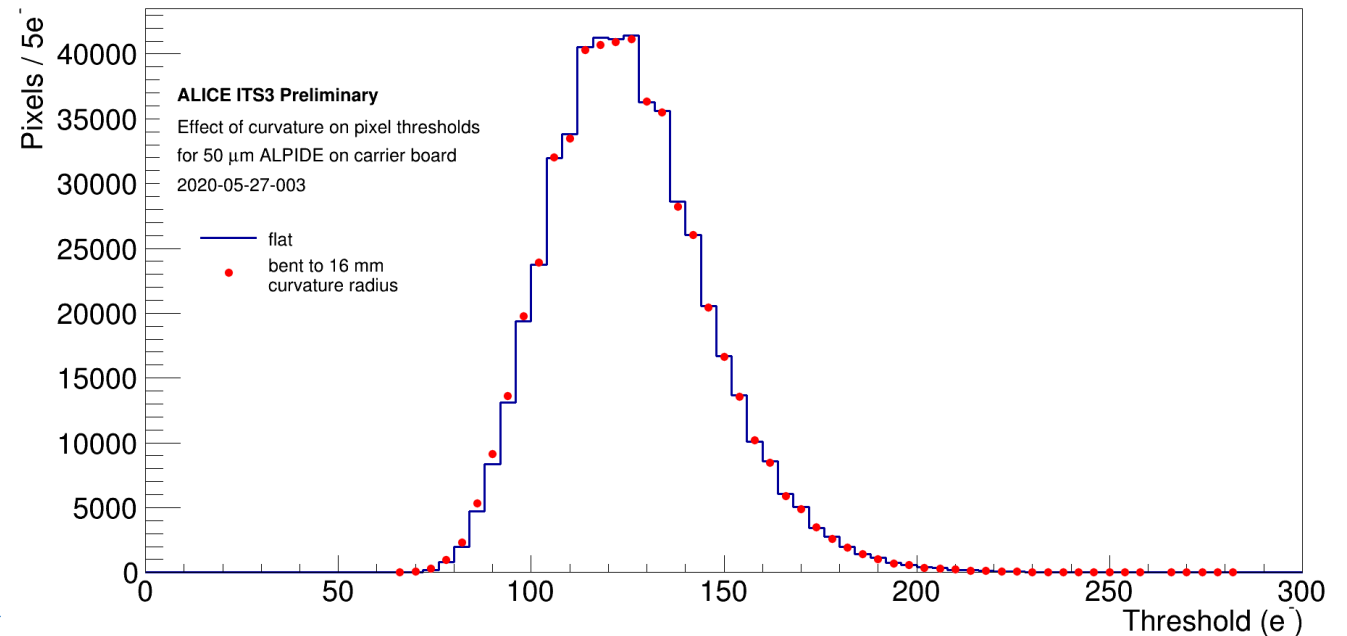


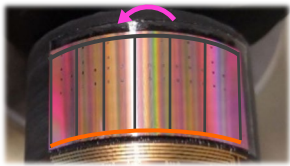
Laboratory tests to characterize bent ALPIDEs

- in terms of thresholds and fake-hit rate
 - different set-ups are tried
 - experience on handling is gained
-
- The curvature effect is not noticeable on:
 - pixel thresholds, FHR, pixel responsiveness
 - tested down to below nominal bending radius
-
- Multiple chips successfully installed and tested in lab, and sent to testbeams

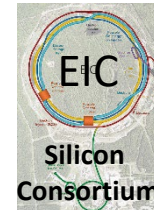


50 μm -thick ALPIDE
(sandwiched between two Kapton foils)





Past/current activities - 3



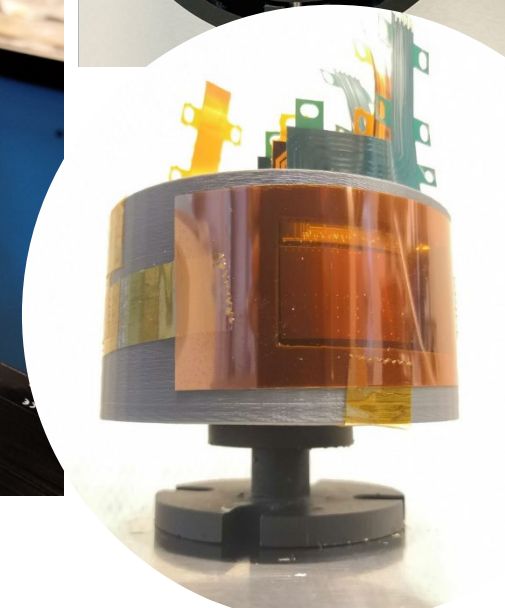
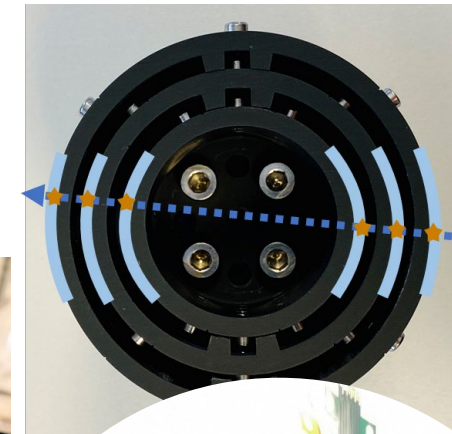
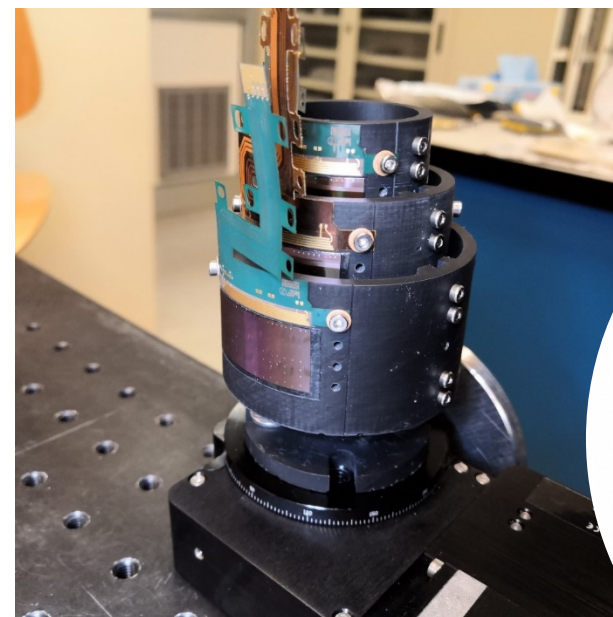
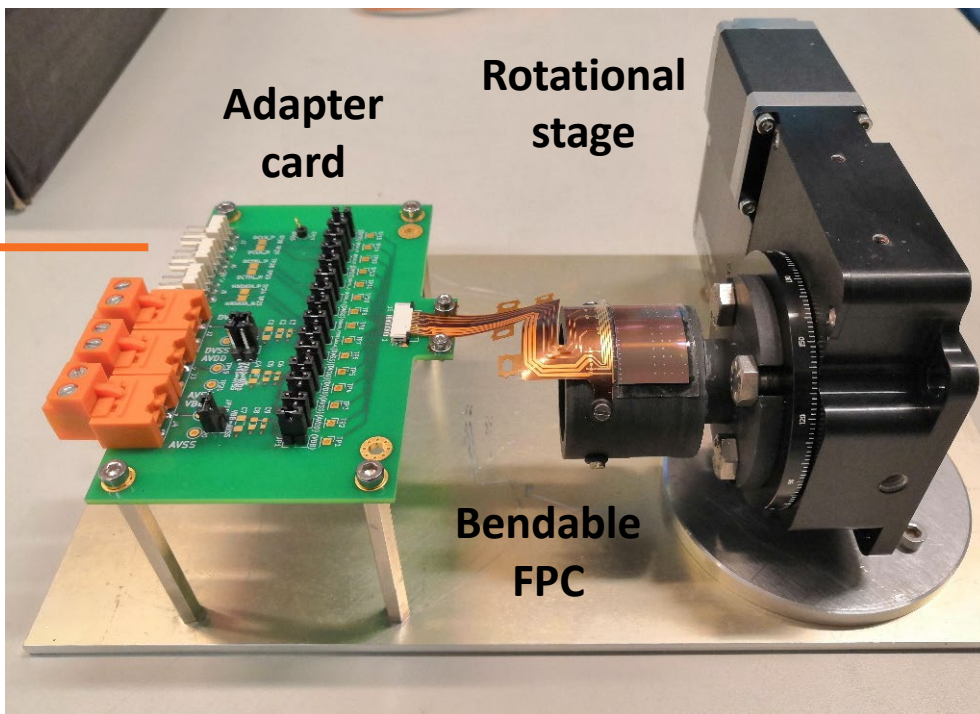
- DUT assembly and lab-characterization

DAQ board /
Power Supply

Adapter
card

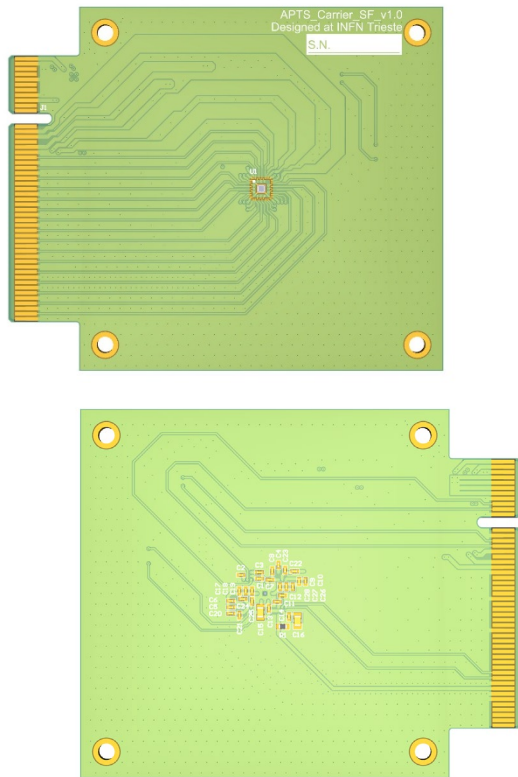
Rotational
stage

Bendable
FPC



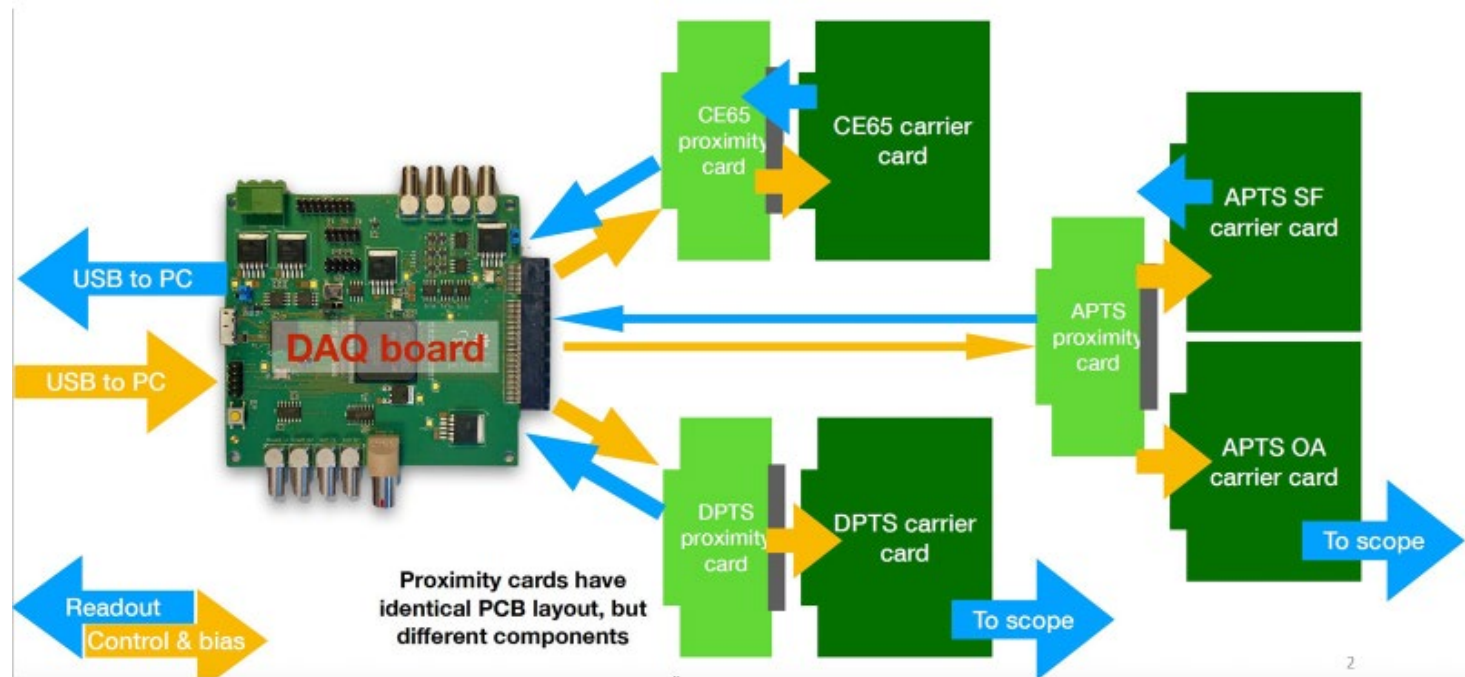
Past/current activities - 4

- Development of APTS Sf carrier board



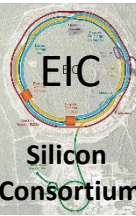
Carrier board layout

Test system concept



2

Plans for future R&D in Trieste



Future activities within ITS3

- Continue with **ALPIDE DUTs** preparation and lab-testing
- **Test and characterization** of MLR1 test structures
- Development characterization setup for **bent MLR1** structures
- Moving to **larger-size** chips for bending and interconnections



Long term tentative plans for EIC-specific development

- **Characterization** of next submissions **after fork-off**
- Development of **test setups** for EIC-specific chips
- Bending and interconnections at **EIC target radius/dimensions**

