High Resolution Timing chips overview

Alexandre Camsonne

ATHENA DAQ Working group

July 22nd 2021

Workshops

- RD51 :

https://indico.cern.ch/event/1040996/

- Streaming workshop 2021

https://indico.mit.edu/event/1/

- Timing workshop upcoming

https://indico.cern.ch/event/861104/

TOF requirements

- New detectors such as thin gap MRPC, MCPPMT, LAPPD, LGAD can reach 40 ps timing resolution and down to 20 ps
- Readout timing resolution and clock jitter needs to be neligible ideally less than 5 ps for 20 ps detectors, could tolerate 25 ps for 40 ps
- Should be compatible with streaming readout

TDC chips

- Omega Group / Weeroc

		sensor	polarity	BW	Zin	Cd	TDC	dyn range	FOM	min thresh	"@Cd="
PETIROC	VPA	SiPM/RPC	both	900 MHz	200	10-100 pF	25 ps			1 mV	
LIROC	VPA	SiPM/RPC	both	300 MHz	1k	10-100 pF	no	10fC-100 pC	2 ns/Q (fC)	40 fC	
ALTIROC	VPA/TZ	LGAD	neg	300-800 MHz	2k/200	1-10 pF	20 ps	0.1-50 fC	100 ps/Q(fC)	2 fC	5 pF
HGCROC	TZ	Si	neg	100 MHz	40	10-100 pF	25 ps	0.1 fC-10 pC	2 ns/Q (fC)	20 fC	50 pF
H2GCROC	CC	SiPM	pos	80 MHz	25	100p-1nF	25 ps	10 fC-200 pC			

- CERN
  - NINO (6ps) +HPTDC TDC (25ps)
  - PicoTDC : 64 channels https://indico.cern.ch/event/1040996/contributions/4402641/attachments/2265267/3846122/PicoTDC_RD51.pdf
- GSI
  - PADI

Sampling chips

- https://indico.cern.ch/event/1040996/contributions/4402546/attachments/2265075/3845732/Digitizers_RD51Workshop.pdf
- Analog memory chips
  - Existing (not ideal because of dead time but could reduce using several chips)
    - DRS4
    - SAMPIC
    - PSEC4
  - Newer less deadtime and self triggering
    - DRS5 (PSI)
    - AARDVARC (NALU)

NALU

Current SoC-ASIC Projects

Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoC	1-3	0.6	2k	64	80-120	May'21
AARDVARC	8-14	2.5	32k	4	4	Rev 3 avail
AODS	1-2	1	8k	1-4	100-200	Rev 1 avail
STRAWZ	5	2	2k	64	10	Dec'22

- **ASoC**: Analog to digital converter System-on-Chip
- **HDSoC**: SiPM specialized readout chip with bias and control
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
- **AODS:** Low density digitizer with High Dynamic Range (HDR) option
- **STRAWZ:** Streaming Autonomous Waveform-digitizer with Zero-suppression

AARDVARC

Parameter	Spec
Sampling Rate	10-14 GSa/s
ABW	> 1GHz
Depth	32k Sa
Trigger Buffer	~3 us*
Deadtime	0**
Channels	4
Supply/Range	1.2V/0.3-0.9V
ADC bits	12
Timing accuracy	<5ps (@13 GSa/s)
Technology	130 nm CMOS
Power	80mW/ch

Sampling chips

- FADC
  - Alphacore
    - A9B1G: Wide Input BW, 9-bit, 1GS/s ADC
    - A10B2G: 10 bit, 2.4GS/s, Ultra Low Power ADC
  - TI
    - ADS54J60 2 ch 16 bit 1 GS/s 10x10 mm2 1.35 W/Ch
    - ADC12DL3200 2 ch 12 bit 3.2 GS/s (or 6.4 GS/s 1 ch) 17x17 mm2 3.15 W
    - ADC12DJ5200RF 2 ch 12 bit 5.2 GS/s (or 10.4 GS/s 1 ch) 10x10 mm2 4 W

NALU chip

Conclusion

- Many chips available
- Preference for FADC but high power consumption
- New analog memory might work with new design but less performant than FADC (better energy efficiency)