Investigation of the half entry issue at the RIKEN testbench
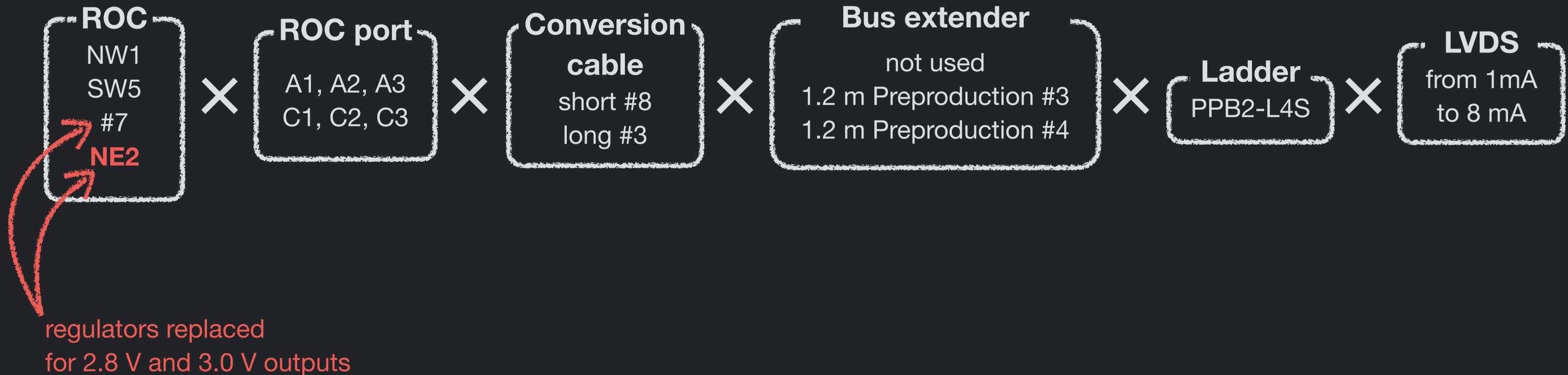
RIKEN, RBRC
    Y. Akiba, I. Nakagawa, **G. Nukazuka**
RIKKYO UNIVERSITY
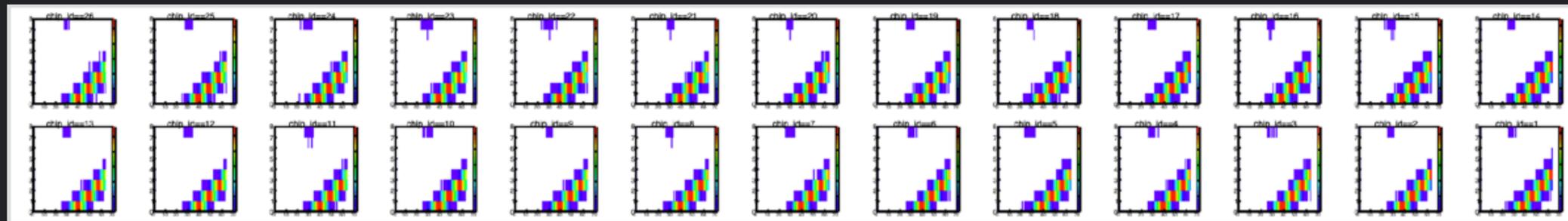   H. Imai, Y. Nakamura, G. Nakano

Calibration tests

To understand the difference between NWU and RIKEN testbenches, mass measurements with various conditions were performed:

ROC
NW1
SW5
#7
NE2

×

ROC port
A1, A2, A3
C1, C2, C3

×

Conversion cable
short #8
long #3

×

Bus extender
not used
1.2 m Preproduction #3
1.2 m Preproduction #4

×

Ladder
PPB2-L4S

×

LVDS
from 1mA
to 8 mA

regulators replaced
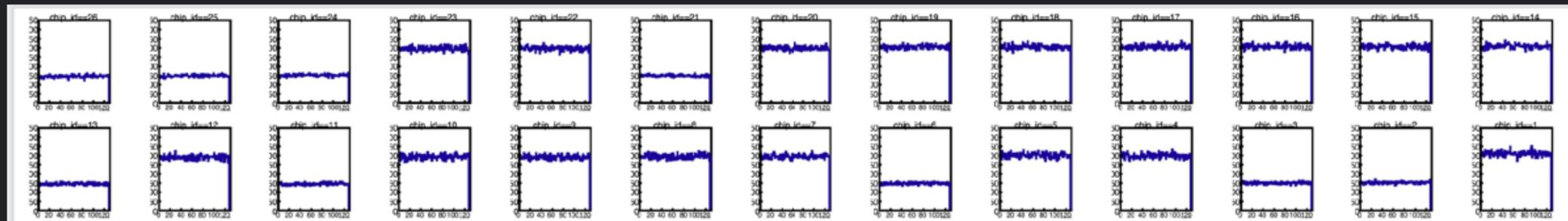for 2.8 V and 3.0 V outputs

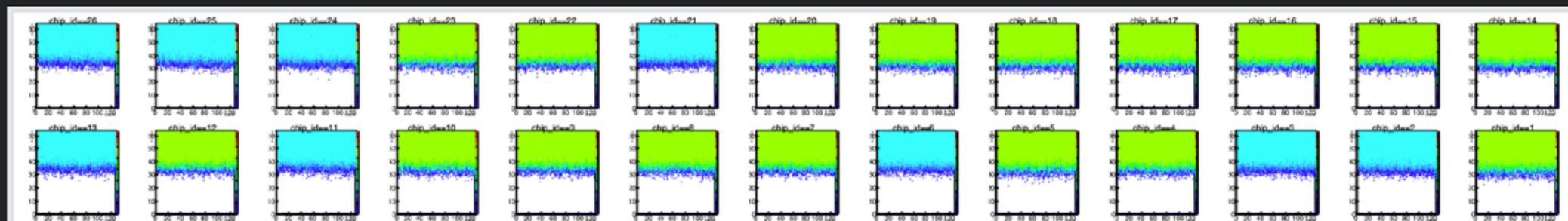# Discovery during the eye-diagram measurements on July/19 - July/20

We firstly used <u>a long conversion cable</u> and a bus extender at the same time in the RIKEN testbench to have exactly the same setup with NWU's.

ADC vs Amplitude

Channel distributions

Setup
   Ladder: PPB2-L4S
   ROC, port: NE2, C1
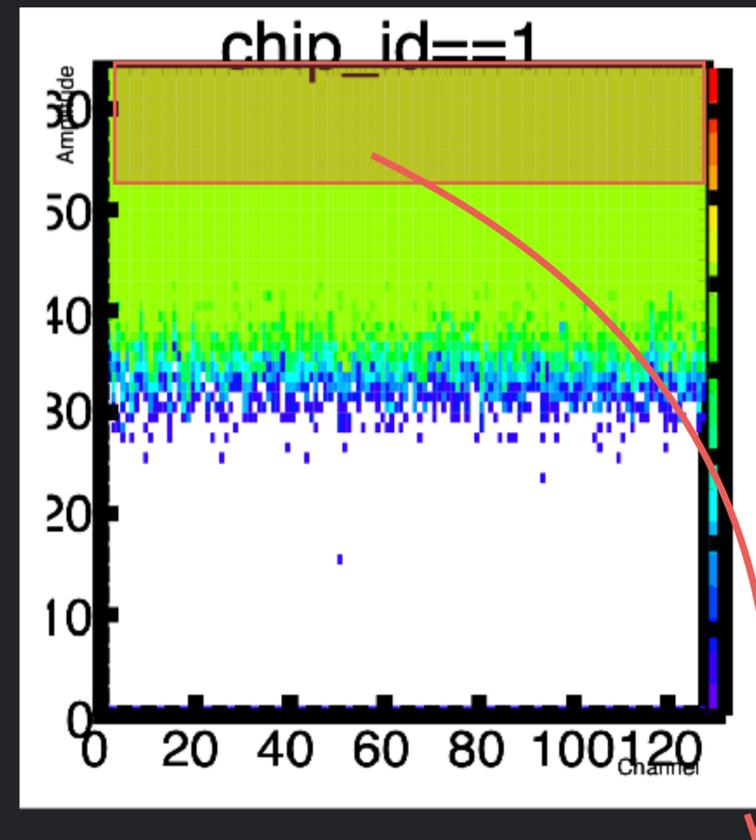   **Conversion cable: long #3**
   Bus extender: 1.2 m Prepro3

Channel vs Amplitude

We performed so many calibration tests with the long conversion cable to confirm the phenomenon.

riken_fphx_raw_20210719-1618_0.dat

Calibration tests, Ratio of successful chips

#run

ROC	port	LVDS = 1 mA	2	3	4	5	6	7	8
NW1	A2		3						
NW1	C3		29		20				
SW5	A1		11						
SW5	A2	56	56		50				102
SW5	A3		3						
SW5	C1		3						
SW5	C2		4						
SW5	C3	115	122	115	215	115	15	15	185
7	A1		7						3
7	A2		5						
7	A3		5						
7	C1		17						
7	C2	3	57		53				53
7	C3		3						
NE2	A1		9						
NE2	A2	37	405	5	104	6	4	4	4
NE2	C1	224	253	223					226

Data points with less than 10 runs not analyzed.

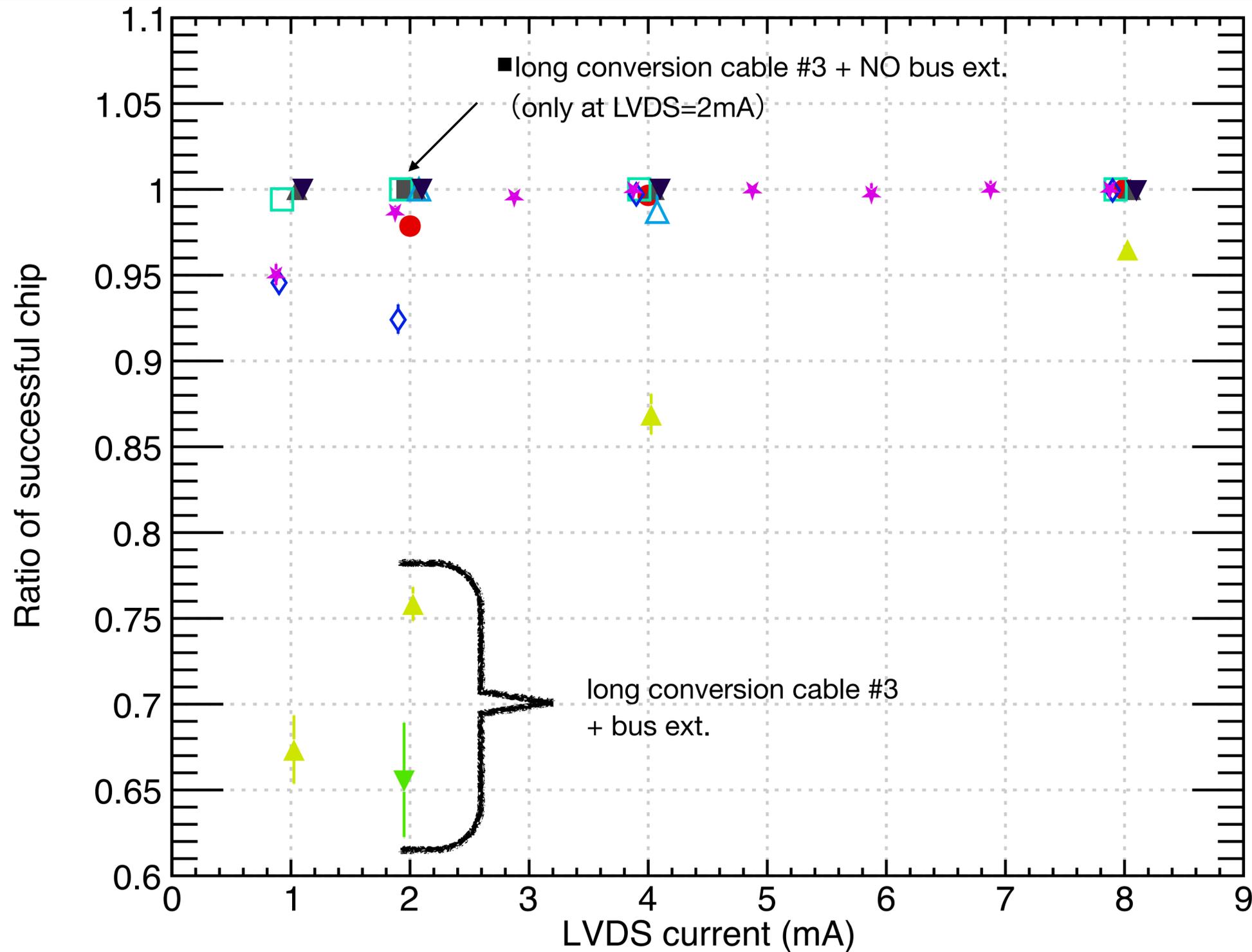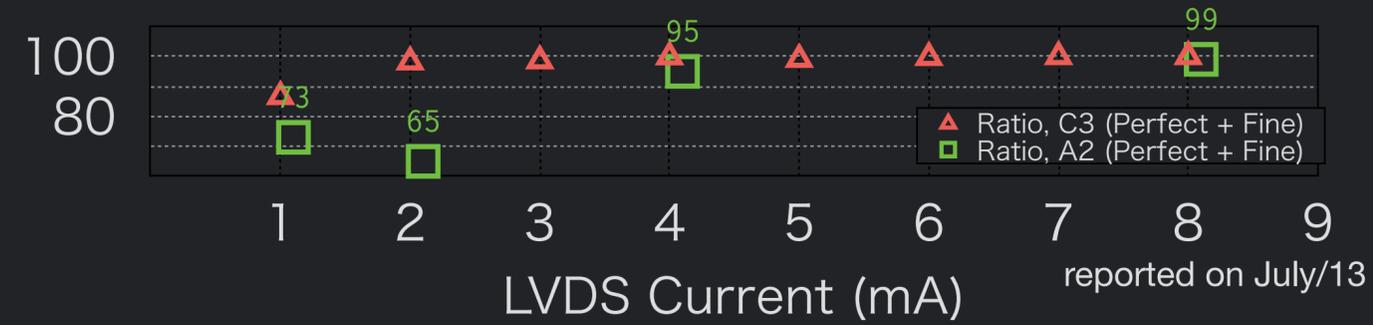| ladder	ROC	ROC port	Conv.	Bus	LVDS
	NW1			not used	1
	SW5	A1	L3	1.2m Prepro3	2
		A2			3
PPB2-L4S		A3		1.2m Prepro4	4
		C1			5
	NE2	C2	S8	1.2m Prepro5	6
		C3			7
	7				8

chip_id==1

Definition of a chip with half entry :
$12700 \times 40\% < \text{entry} < 12700 \times 60\%$

total entries for a chip:
$12700 \times 40\% < \text{entry}$

Ratio of successful ratio:
half entry / total entry

0<ch<128 (ch 0 ignored since noise data tends to be there as well)
53 < ampl < 65 (only stable area)
→ 127 × 10 × 10 = 12700 events/chip in ideal cases

Ratio of successful chip

reported on July/13

Legend (inset top right):
- Ratio, C3 (Perfect + Fine)
- Ratio, A2 (Perfect + Fine)
- LVDS Current (mA)

Main plot annotations:
- ■ long conversion cable #3 + NO bus ext. （only at LVDS=2mA）
- long conversion cable #3 + bus ext.
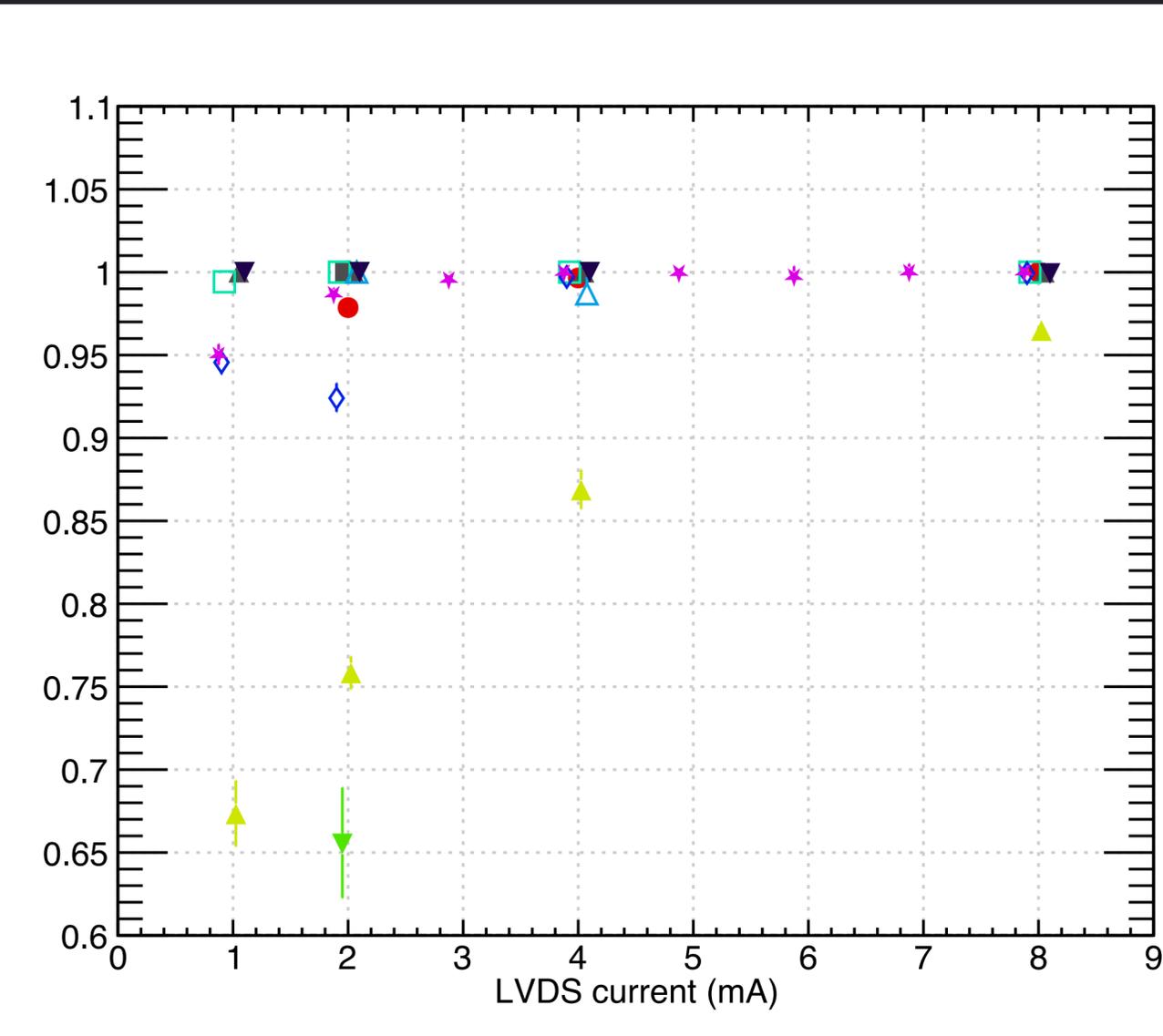
Y-axis: Ratio of successful chip
X-axis: LVDS current (mA)

Legend:
- PPB2-L4S,   7-C2, s8, 1.2mprepro4
- PPB2-L4S, NE2-A2, l3, NotUsed
- PPB2-L4S, NE2-A2, l3, 1.2mprepro3
- PPB2-L4S, NE2-C1, l3, 1.2mprepro3
- PPB2-L4S, NE2-C1, s8, NotUsed
- PPB2-L4S, NE2-C1, s8, 1.2mprepro3
- PPB2-L4S, NW1-C3, s8, 1.2mprepro4
- PPB2-L4S, SW5-A2, s8, 1.2mprepro3
- PPB2-L4S, SW5-C3, s8, NotUsed
- PPB2-L4S, SW5-C3, s8, 1.2mprepro3

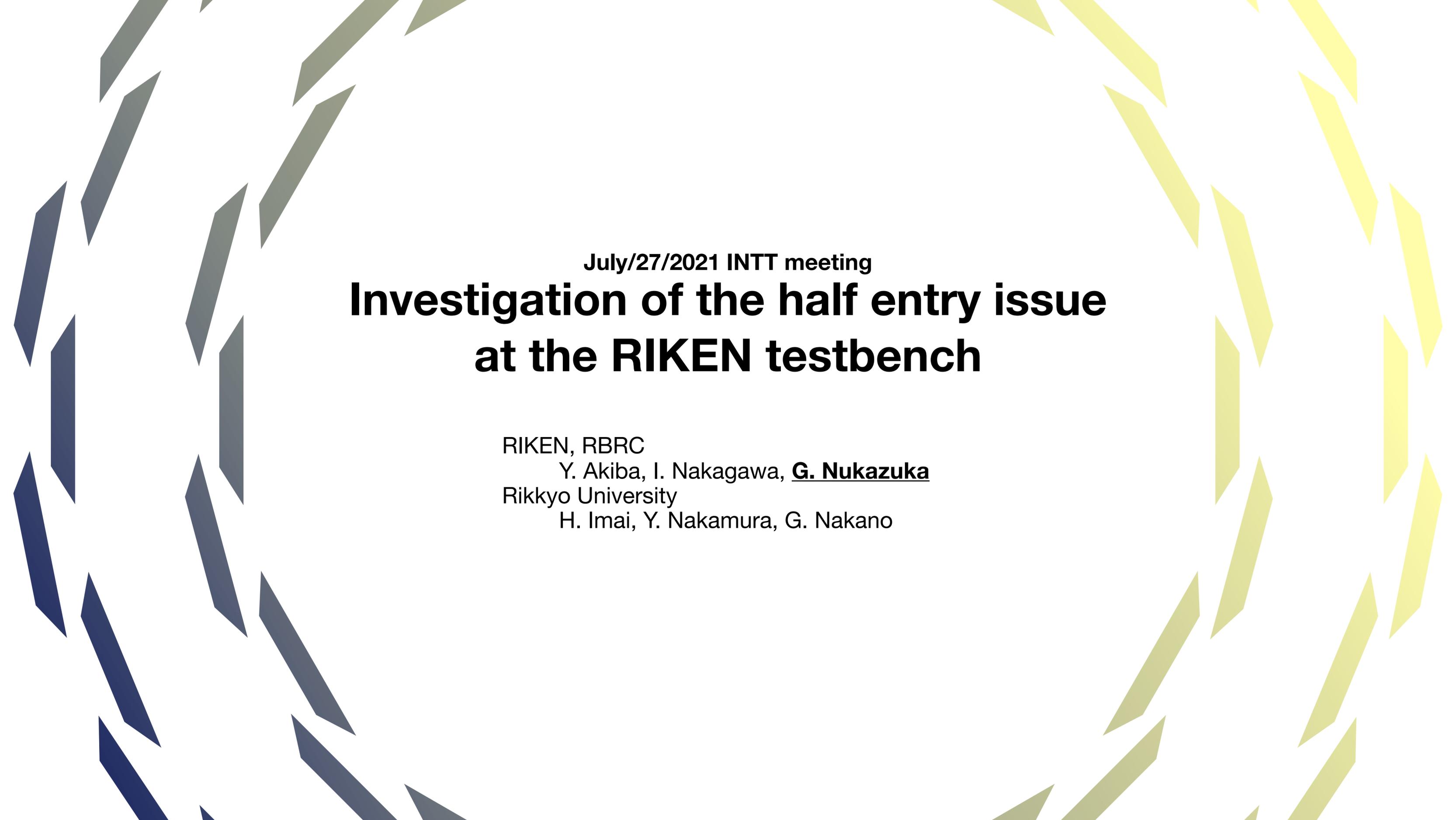Half-entry chips appear frequently when a long conversion cable is used.

Ratio of successful chip, Statistics

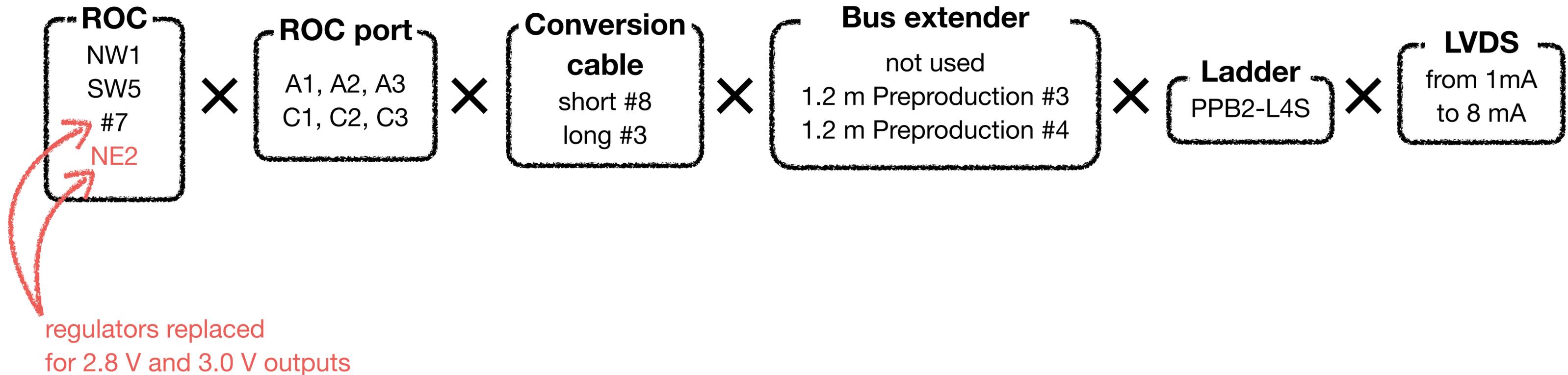|	ROC	Port	Conv	Bus	1 OK	total	Ratio	2 OK	total	Ratio	3 OK	total	Ratio	4 OK	total	Ratio	5 OK	total	Ratio	6 OK	total	Ratio	7 OK	total	Ratio	8 OK	total	Ratio
●PPB2-L4S	7	C2	s8	1.2mprepro4				1145	1170	0.98				570	572	1.00										390	390	1.00
▲PPB2-L4S	NE2	A2	I3	1.2mprepro3	408	606	0.67	1496	1973	0.76				780	898	0.87										1726	1789	0.96
▪PPB2-L4S	NE2	A2	I3					4575	4576	1.00																		
▼PPB2-L4S	NE2	C1	I3	1.2mprepro3				152	232	0.66																		
□PPB2-L4S	NE2	C1	s8	1.2mprepro3	2042	2054	0.99	1716	1716	1.00				1846	1846	1.00										2054	2054	1.00
▲PPB2-L4S	NE2	C1	s8		1586	1586	1.00	1794	1794	1.00				1794	1794	1.00										1846	1846	1.00
△PPB2-L4S	NW1	C3	s8	1.2mprepro4				443	443	1.00				302	306	0.99												
◇PPB2-L4S	SW5	A2	s8	1.2mprepro3	1008	1066	0.95	985	1066	0.92				1037	1040	1.00										1663	1664	1.00
★PPB2-L4S	SW5	C3	s8	1.2mprepro3	1332	1402	0.95	1411	1430	0.99	2666	2678	1.00	3795	3796	1.00	2573	2574	1.00	363	364	1.00	364	364	1.00	1430	1430	1.00
▼PPB2-L4S	SW5	C3	s8		1118	1118	1.00	1326	1326	1.00				1170	1170	1.00										2388	2390	1.00

backup

Investigation of the half entry issue at the RIKEN testbench

RIKEN, RBRC
    Y. Akiba, I. Nakagawa, **G. Nukazuka**
Rikkyo University
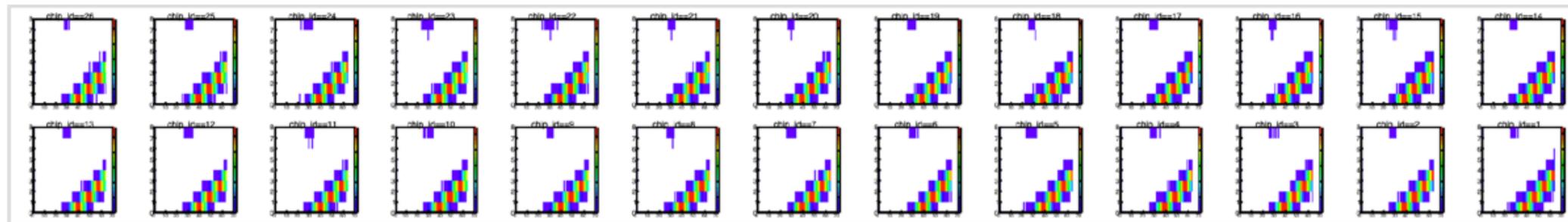   H. Imai, Y. Nakamura, G. Nakano

Calibration tests

To understand the difference between NWU and RIKEN testbenches, mass measurements with various conditions were performed:
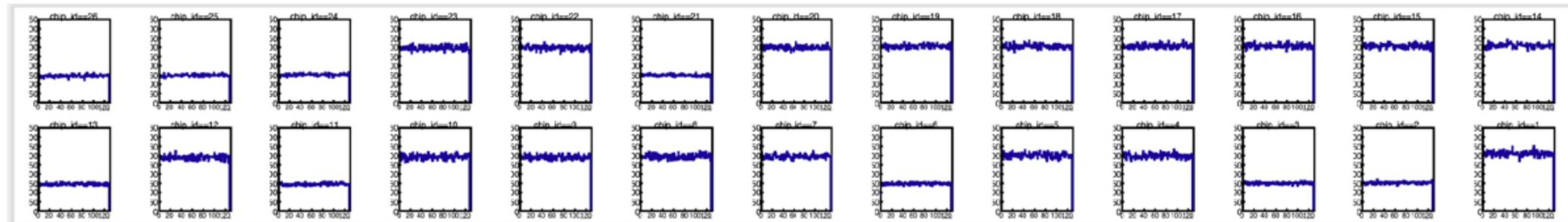
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A1, A2, A3
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ROC, port: NE2, C1
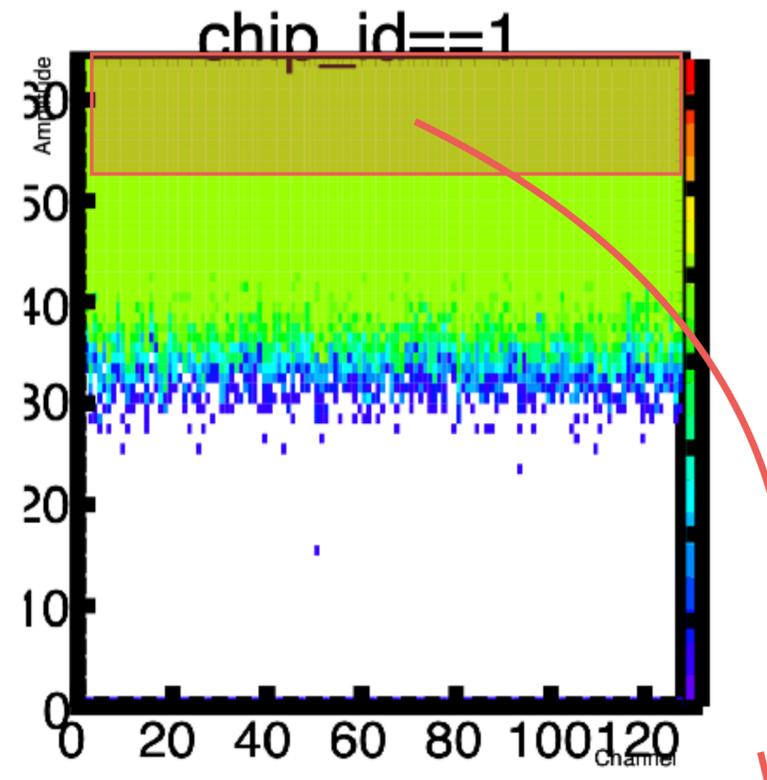**Conversion cable: long #3**
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riken_fphx_raw_20210719-1618_0.dat

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		A2			3
PPB2-L4S		A3		1.2m Prepro4	4
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	NE2	C2	S8	1.2m Prepro5	6
		C3			7
	7				8

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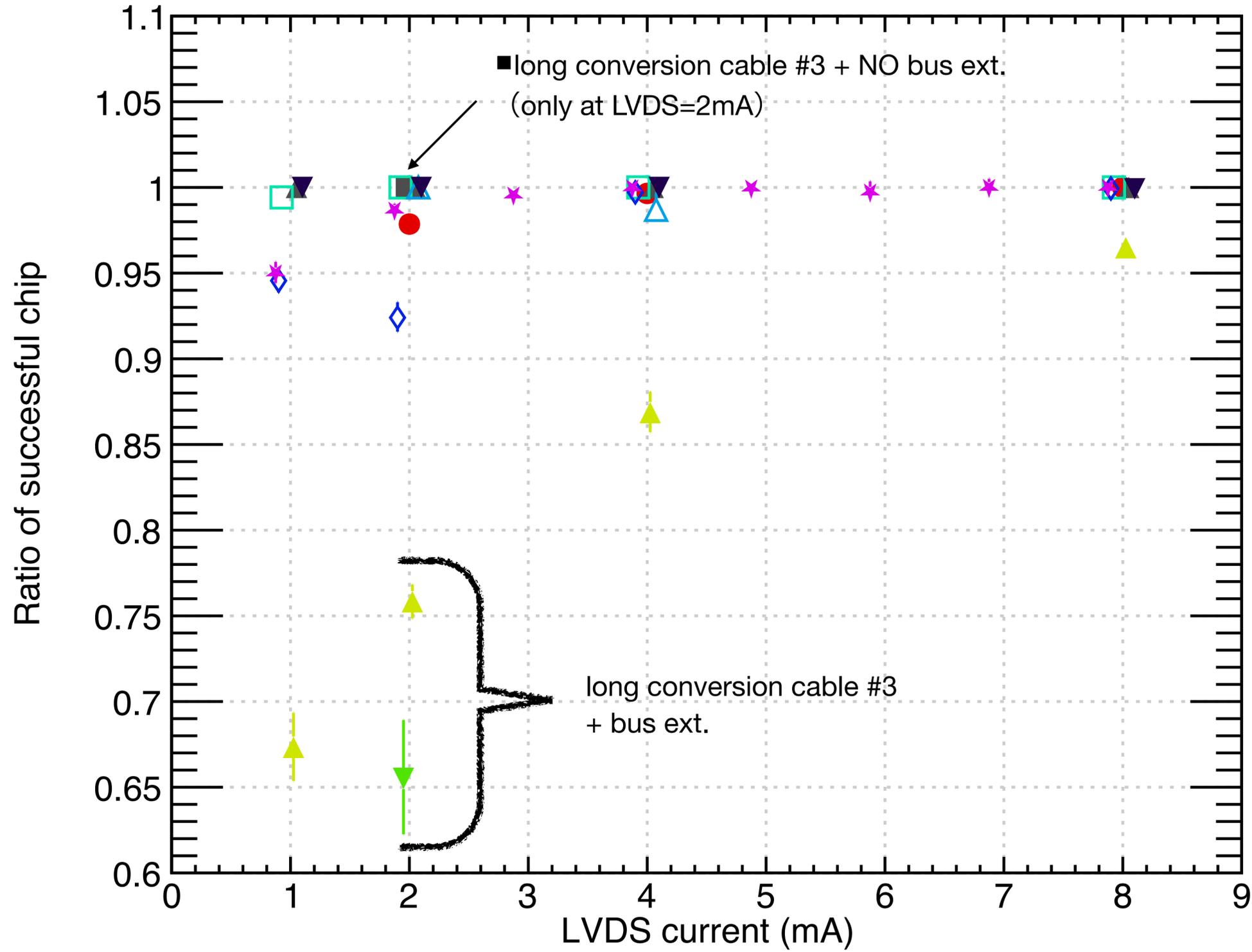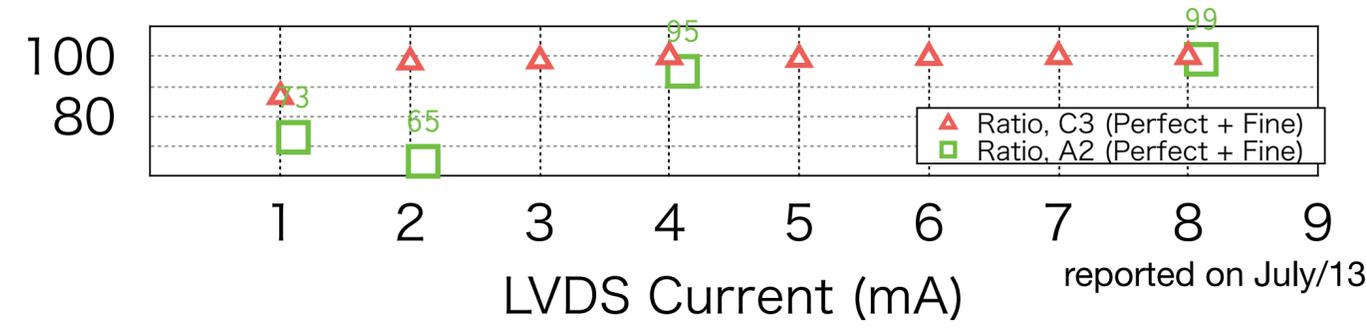
Half-entry chips appear frequently when a long conversion cable is used.

Calibration tests without a bus extender

Measurements were performed without any major problems.

Performance of ROC ports

	A1	A2	A3	C1	C2	C3
7	Good except chip25	no data	Good except chip1-5	Good except chip15	Good	Good
NW1	no data	no data	no data	Good	Good	Good
SW5	Good	Good	Good	Good	Good	Good

H~igh~D~ensity~Interface

ReadOut Card (ROC)
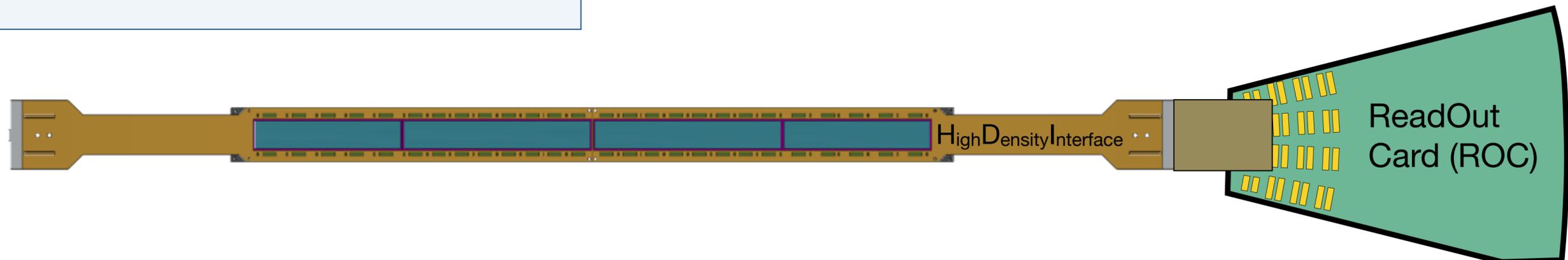
Summary

Calibration tests were performed very stably with various configurations.

Chips with only half entry rarely appear at RIKEN testbench about 0.1%. The issue may depends on a setup.
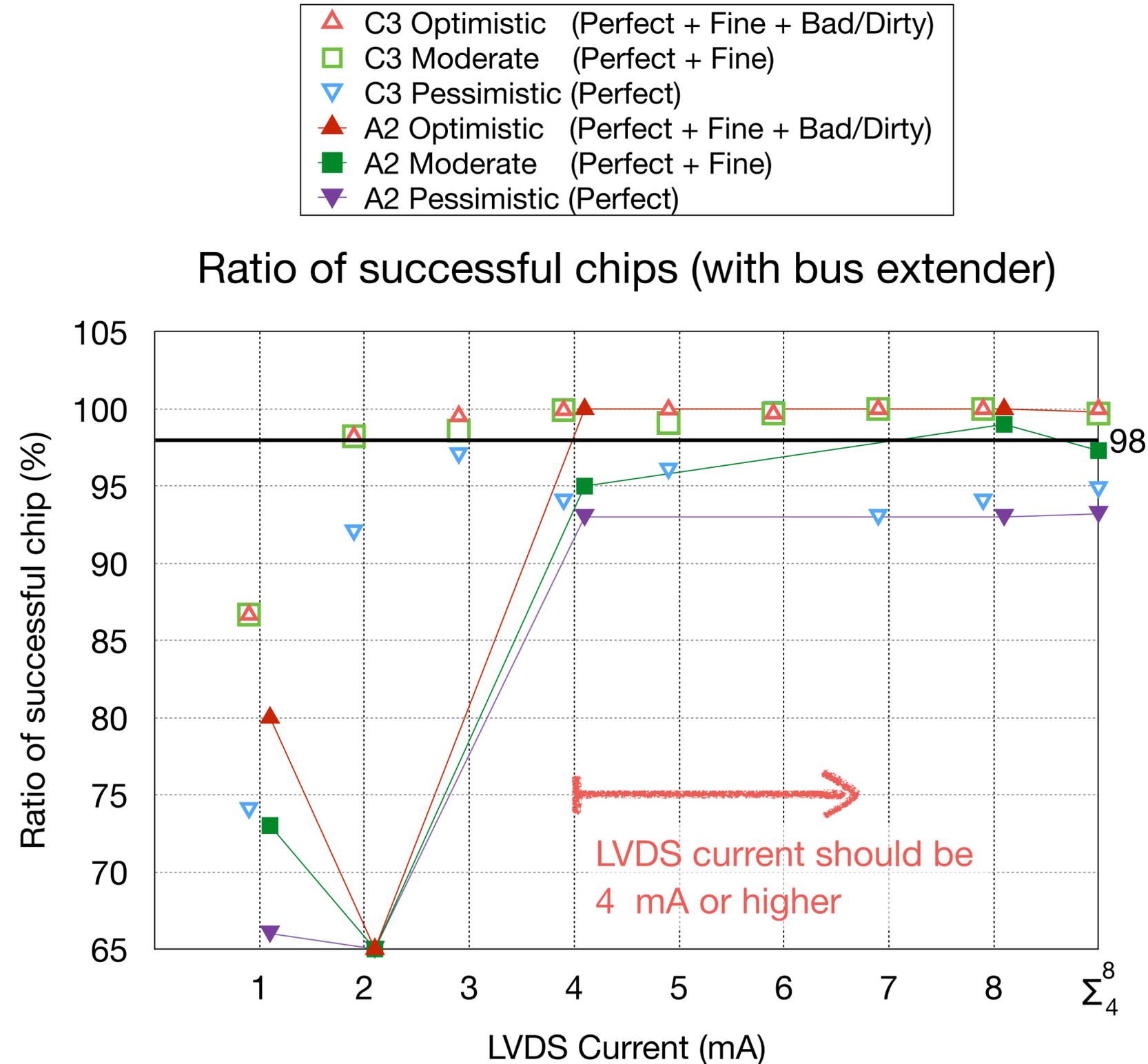
About 5% of chips have less data ~300 entries/ch than usual (350/ch).
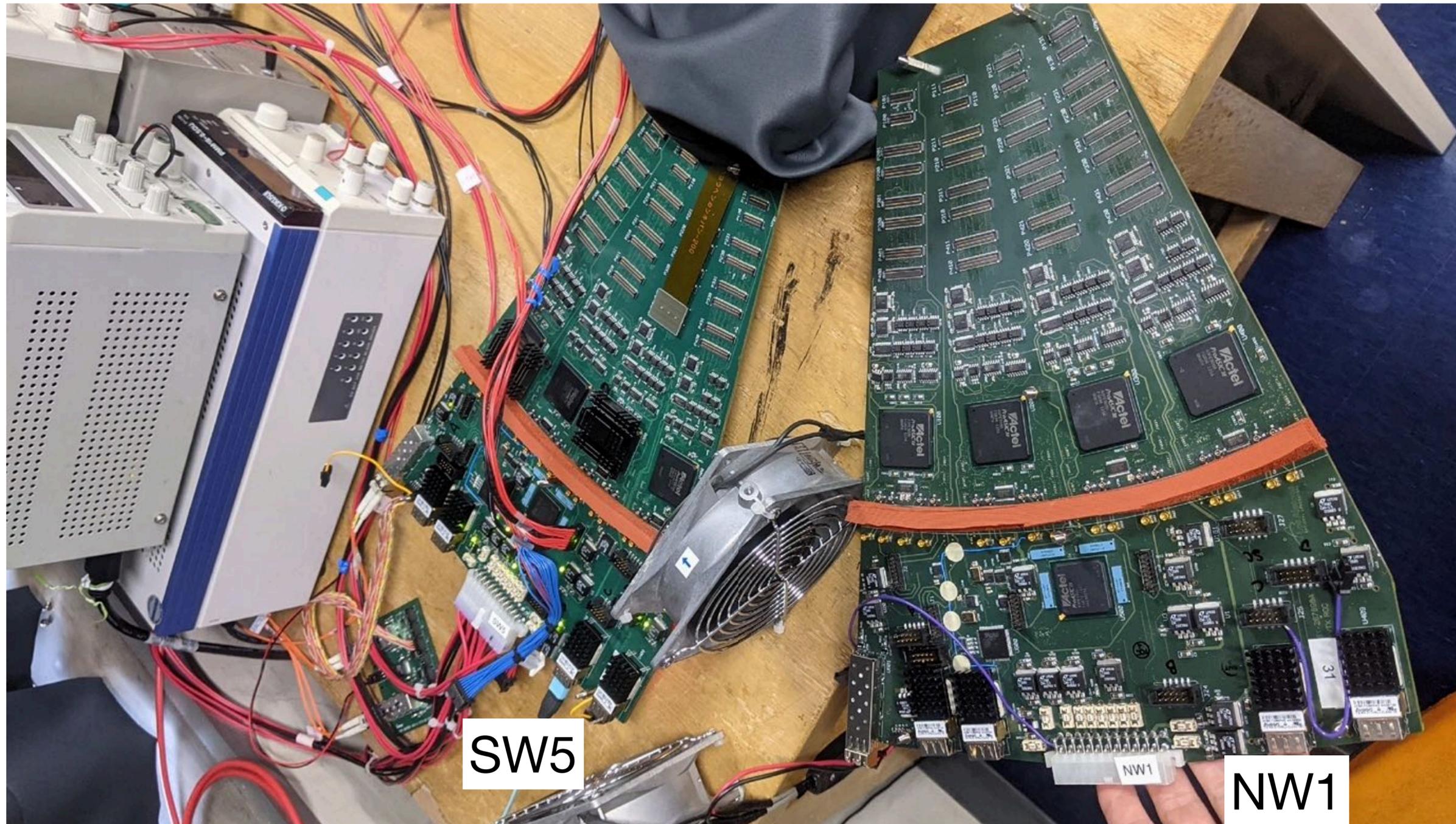
Further investigations are planned.

Ratio of successful chips (w/o bus extender)
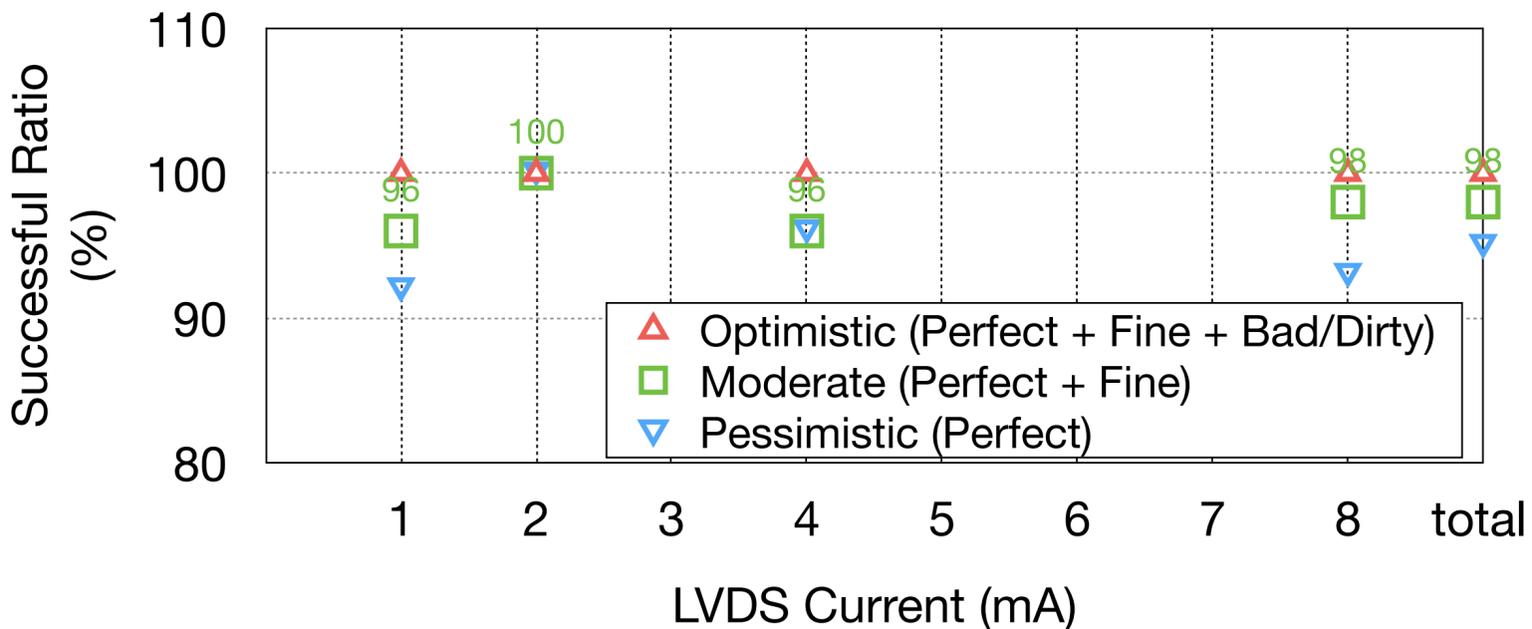
Ratio of successful chips (with bus extender)

RIKEN testbench