Electronics Readout Performance

WBS: 3.01

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July 28^{th} , 2021

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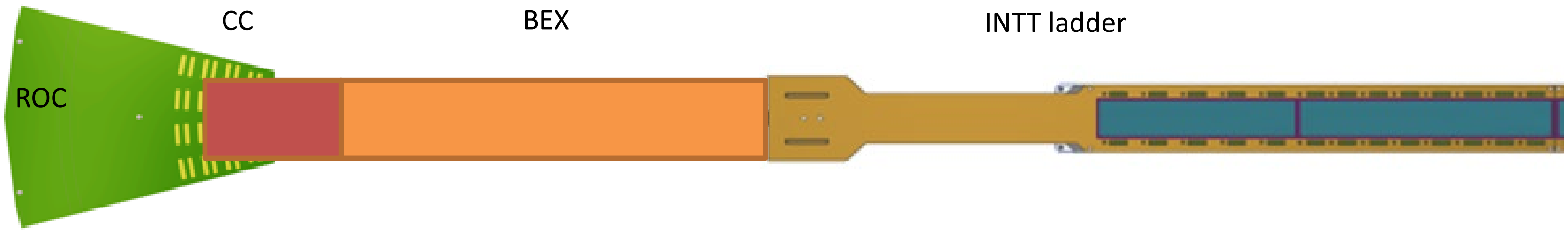
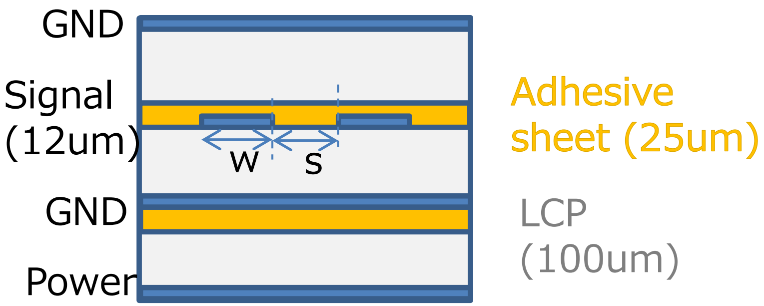


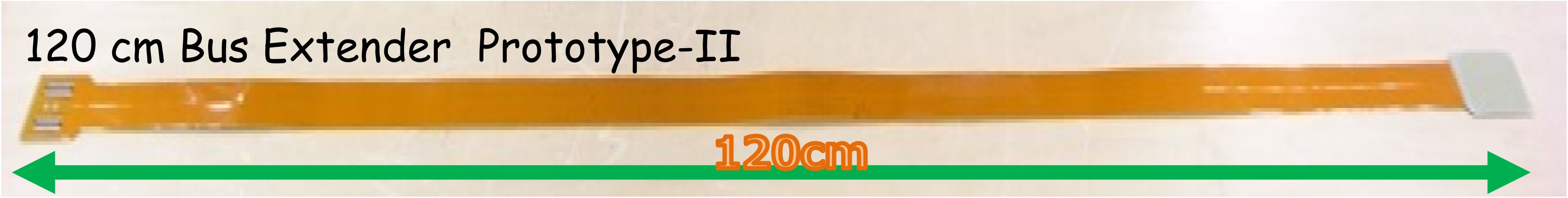
Development of the Bus-Extender

- Cable design (prototype)
  - Dimension (L x W): 120 x 5 cm^2
  - 4 layers (signal , 2xGND, PWR)
  - Lines : 62 lines (Line and space : 130 & 130 um)
  - Z_{diff} : 100Ω by strip line structure
    - Signal layer is sandwiched by GND layers
  - **Liquid Crystal Polymer (LCP) as substrate**
    - Relatively new material for FPC
    - Less signal loss due to low di-electric constant & tan(δ)
    - Thick LCP available for Z_{diff} : 100um
  - **The design is decided based on EM-field simulation**

4 layers laminated by the adhesive sheet



- Prototype

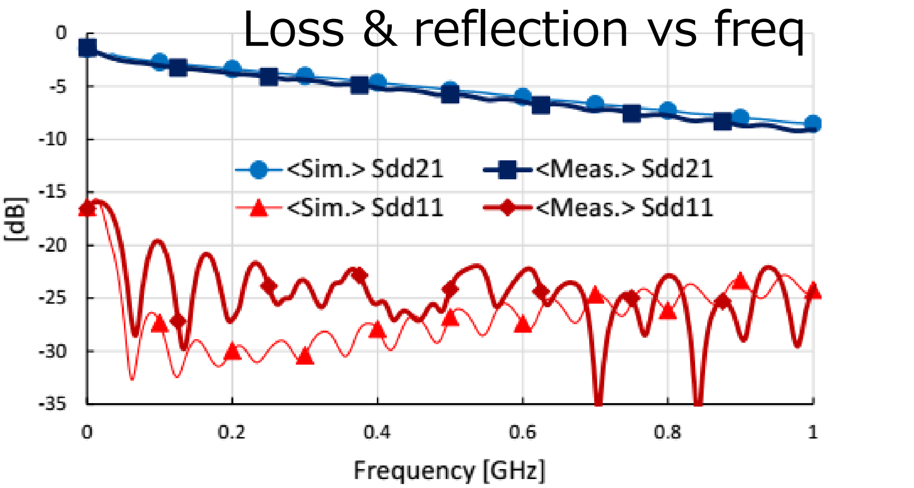


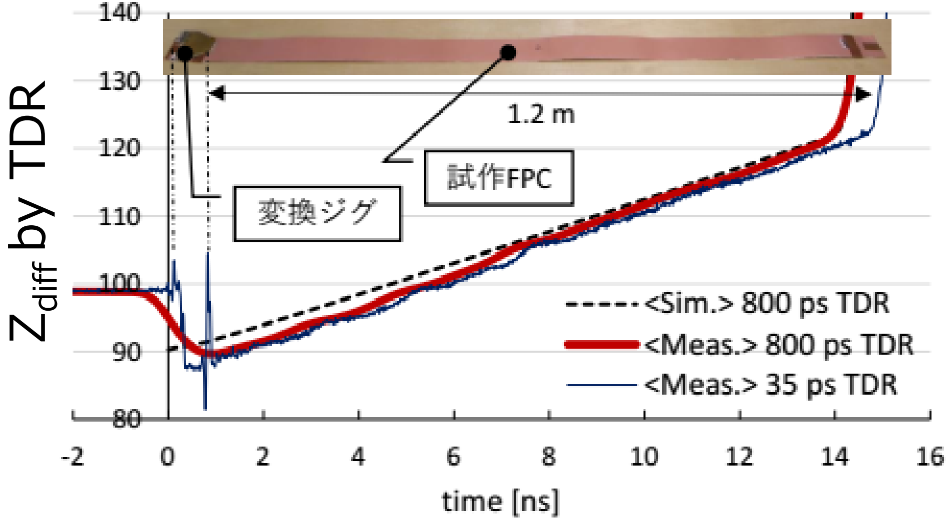
Bus Extender Performance

- Electrical properties
  - **Signal loss vs freq. ,**
  - **Z_{diff} by TDR**
  - **Eye diagram**
- Mechanical property
  - Accuracy of line & space
- Aging test
- Radiation hardness

Test bench to study properties of the single Bus-Extender

Bus Extender Electrical Performance 1.2m



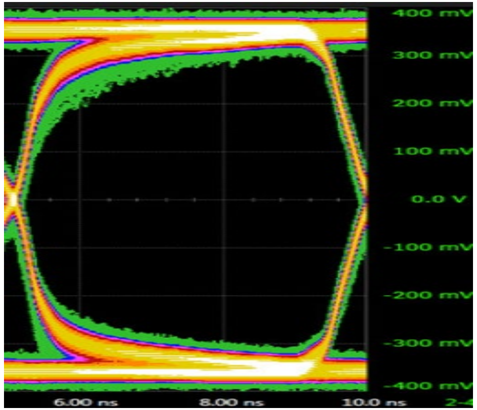


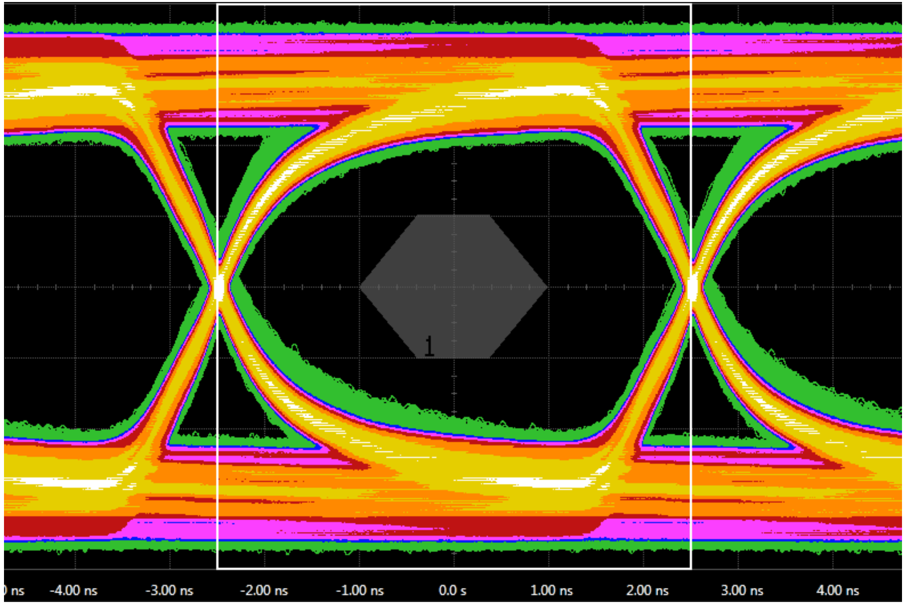
- Freq. dependence(s-parameter)
  - **Signal loss : ~30%、**
  - **Reflection: < 10%**
- Zdiff by TDR
  - **Z ~ 90Ω (slight smaller than 100Ω)**

Data is consistent with the EM field simulation

Eye diagram

Input : 200Mbps pseudo-random pulse with 500 ps rising time,

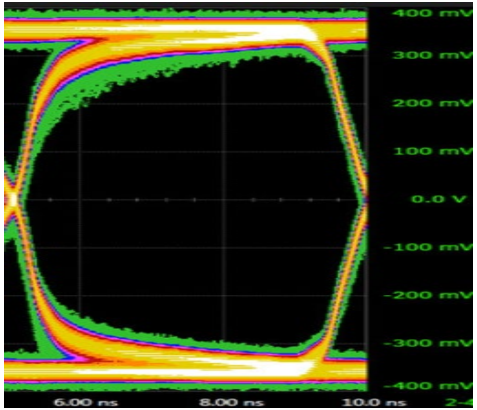


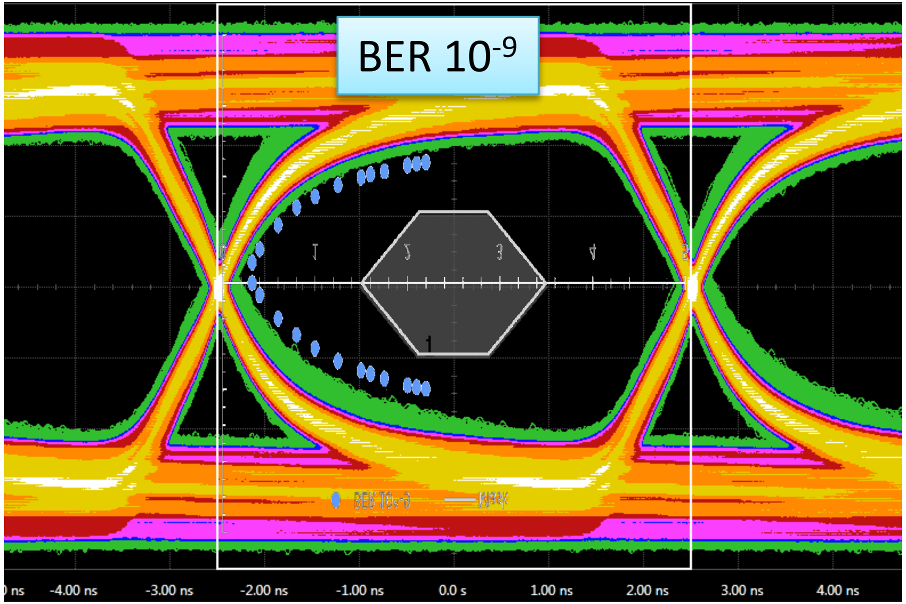


- The signal pulse is clearly separated from the mask
  - Pulse get distorted due to larger signal loss of hi-freq. component

Eye diagram

Input : 200Mbps pseudo-random pulse with 500 ps rising time,



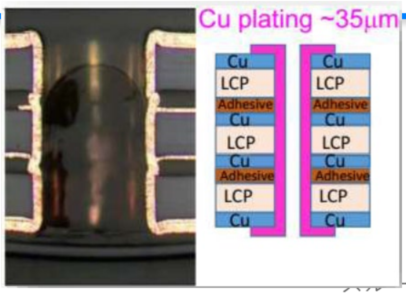


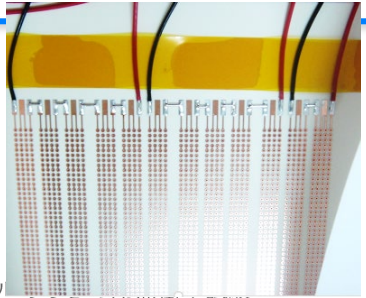
- The signal pulse is clearly separated from the mask
  - Pulse get distorted due to larger signal loss of hi-freq. component
  - Bit error rate < 10^{-9}

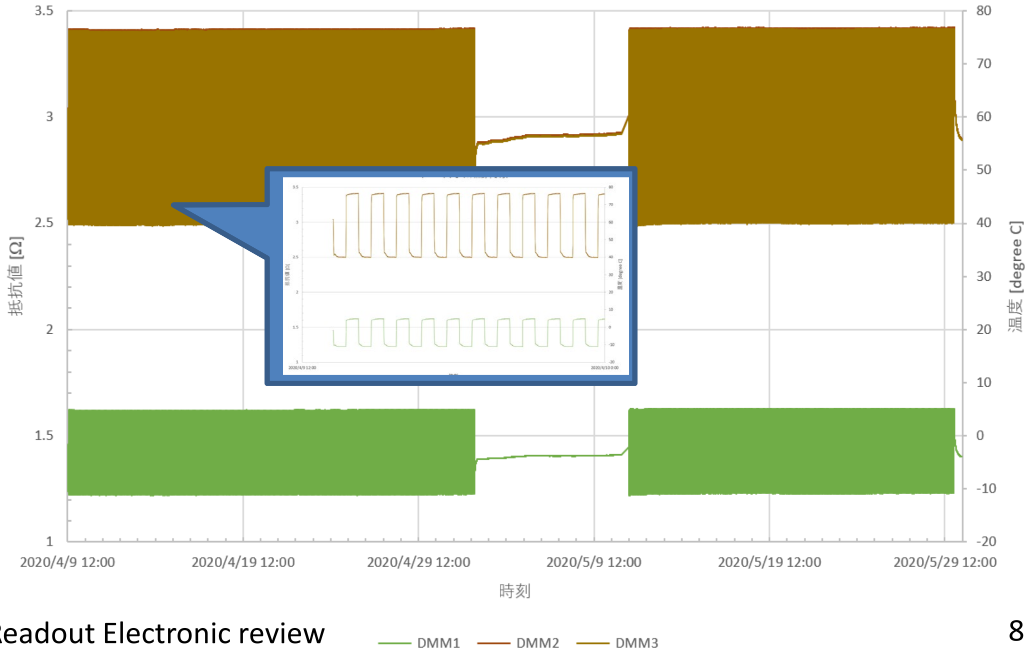
The performance of bus-extender is good enough for INTT

Aging Test

- Keep healthy at least 3 year operation
- Mechanical stress by temperate
  - **LCP is expanded and shrunk**
  - **Throu-hole could be damaged.**
- Temperature cycle
  - **-15 (30min.) ~ 75℃ (30min.) with 1~2min. transition.**
  - **1000 cycles (40 days)**
- Test FPC sample
  - **4 layers, same as bus extender**
  - **400, 1000, 1000 throu-holes are daisy chained and its resistance monitored .**
- Results
  - **Resistances changed with temperature**
  - **All FPC samples are healthy after 1000 cycles.**

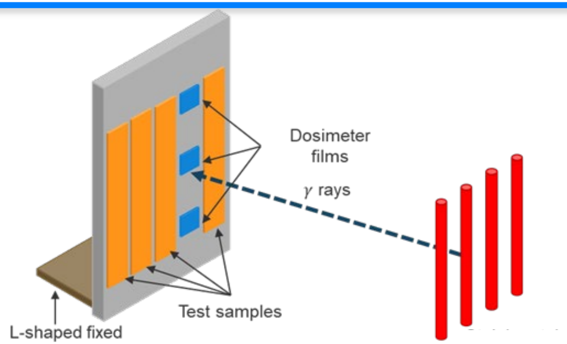






Radiation hardness

- Radiation hardness tested
  - **Keep healthy for at least three years of operation.**
  - **Investigate the radiation hardness since the Bus-extender is produced with advanced materials, LCP and adhesive sheet.**



^{60}Co pellets are enclosed by stainless tube

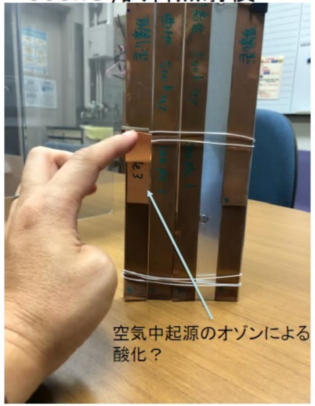
- FPC samples are exposed by strong Gamma source (^{60}Co) @ QST Japan
  - Radiation dose：5kGy, 500kGy, 1000k Gy

- Evaluate radiation hardness using two mechanical properties
  - **Stiffness (Young's modulus)**
  - **Peeling Strength**

準備室内

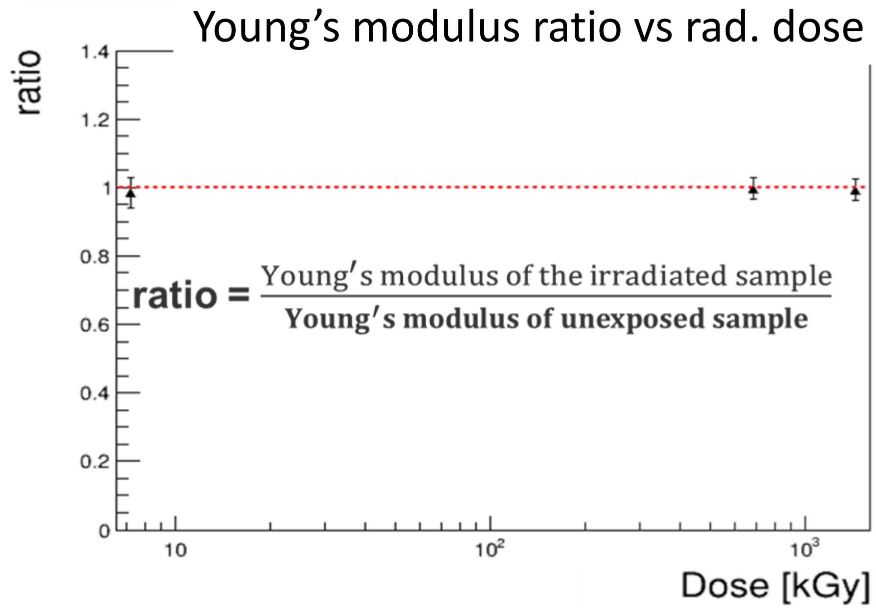
線量評価シート
レンジ：1-150kGy
精度：<7% 5-150kGy

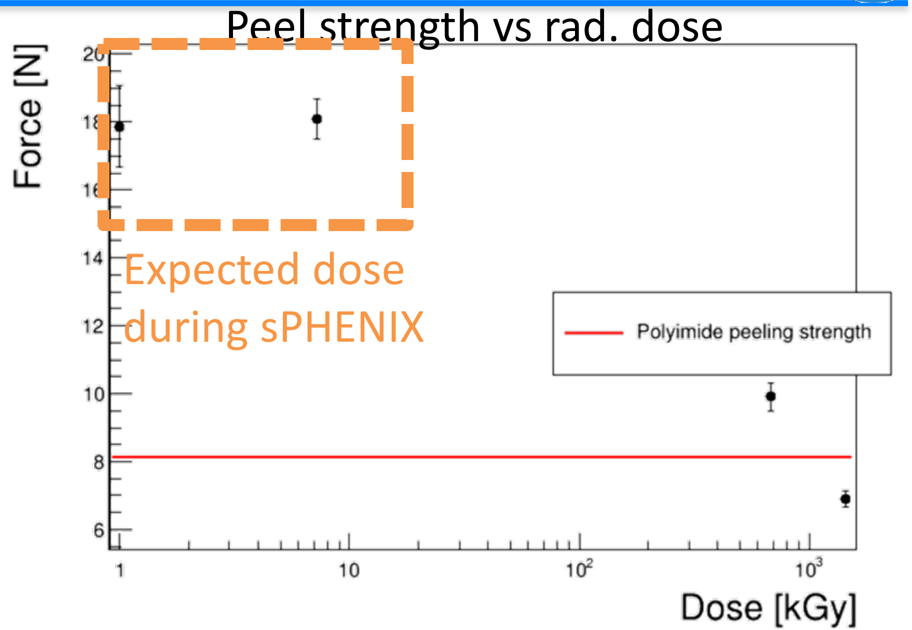
• 500kGy試料照射後



After exposure,
the samples look oxidized by ozone (O_3)

Results: Rad. hardness



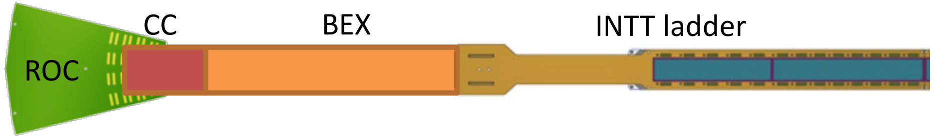


- Young's modulus: No change within 7% uncertainties by radiation exposure
- Peel strength : No change for sPHENIX data taking and get smaller clearly for the higher exposure.

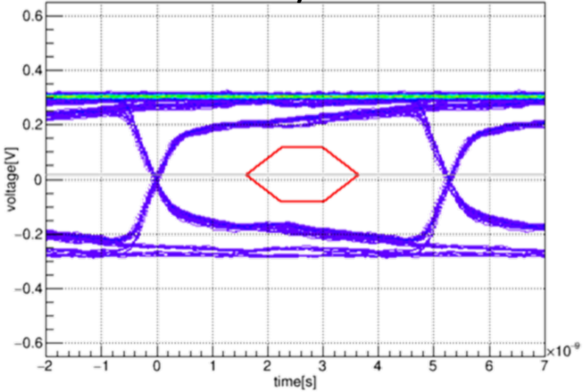
Radiation hardness of Bus extender is good enough for sPHENIX

HDI + Bus Extender in Full Readout Chain

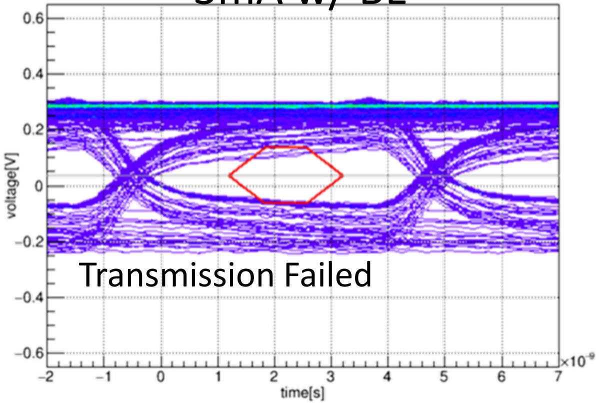
- Eye diagram w/ BE in the readout chain
- Data transmission sometimes failed w/ BE
  - **Distortion and attenuation is consistent w/ the self BE performance**
  - **HDI make additional distortion.**
- Larger (8mA) LVDS current recovers the transmission successfully
  - **FPHX chip has a capability to change LVDS current from 1 – 8 mA**



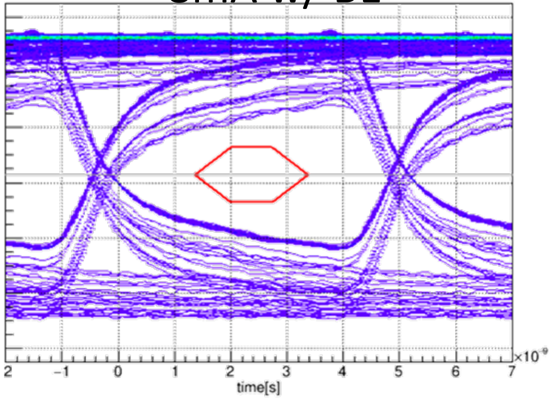
3mA w/o BE



3mA w/ BE



8mA w/ BE

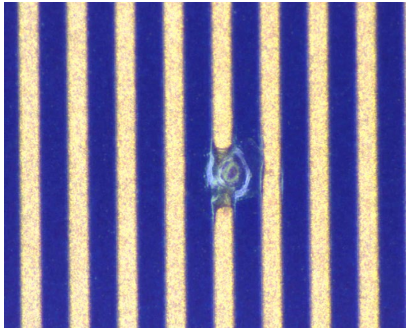


Recovered by large LVDS current

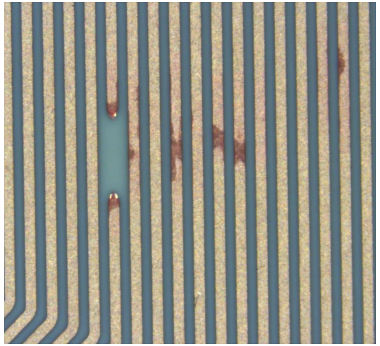
Toward Mass production

- Improving the yield rate is necessary
  - Current good yield rate was ~20~30%
  - Production parameters are best tuned
    - Pressure to make multi-layer & make throu-hole
- Inspected/discussed the production procedure with manufacturers
  - Contamination of small dusts is major cause when producing the FPC
- New procedures to remove the dust as much as possible
  - UV lights to look for remaining dust
  - Silicon roller to remove dust
- Check the continuity before laminating multiple layers
- Expect to be improved to good yield rate ~80%

Short line by mis-exposure



Open line by mis-etching



Continuity checks for the production

Single layer

- **Exposure**
- **Etching**

→ Continuity check

Multi-layer

- **Laminate Multi-layer**
- **Through hole** Drilling & Cu-plating
- **Surface layer** Finishing processes

→ Continuity check

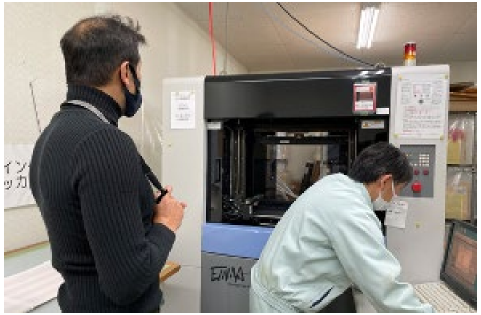
- **Mount parts (conn)**

→ Continuity check

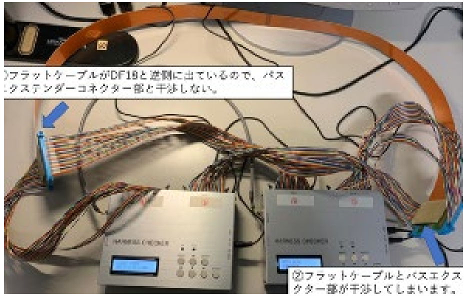
Three times of the continuity checks during the production

- Twice at manufacture.
- One as receiving inspection

Yield rate improved dramatically



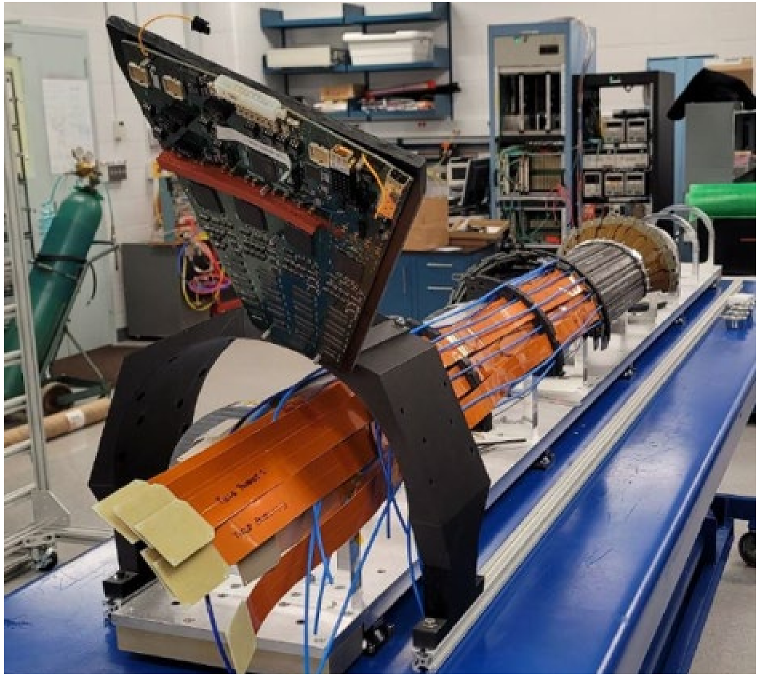
Flying probe tester

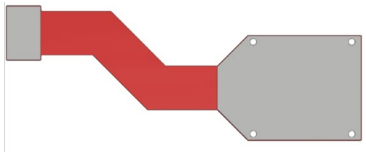


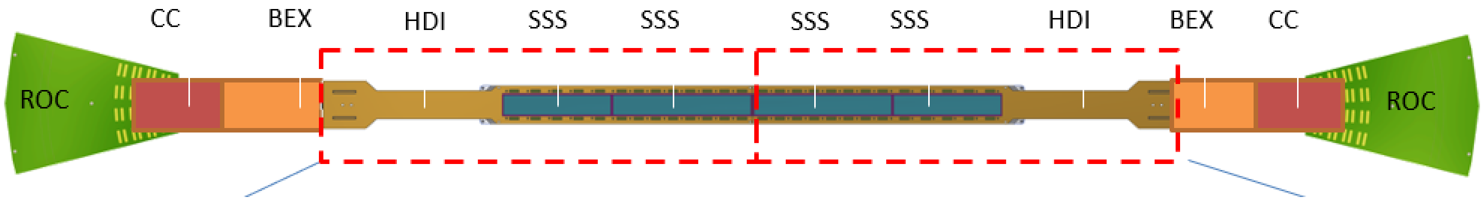
The special cable checker

Bus-Extender in Barrel

- Barrel assembly is in progress
  - **Checking the interfere of the ladders**
  - **Adjust the length of the bus extender.**
  - **Optimized the shape of the conversion cables**







Plan & Schedule

- Bus-Extender
  - **Final design : End of July**
  - **Test production: End of September**
  - **Full mass production**
    - **50 % production in Oct-Nov/2021**
    - **50 % production in Dec/2021-Jan/2022**
- Conversion cable
  - **Design : several different shapes**
  - **Test production**
  - **Mass production**

Bus-Extender Summary

- Bus-Extender, Long and High Density Flexible Cable, is technically most challenging part on the INTT development.

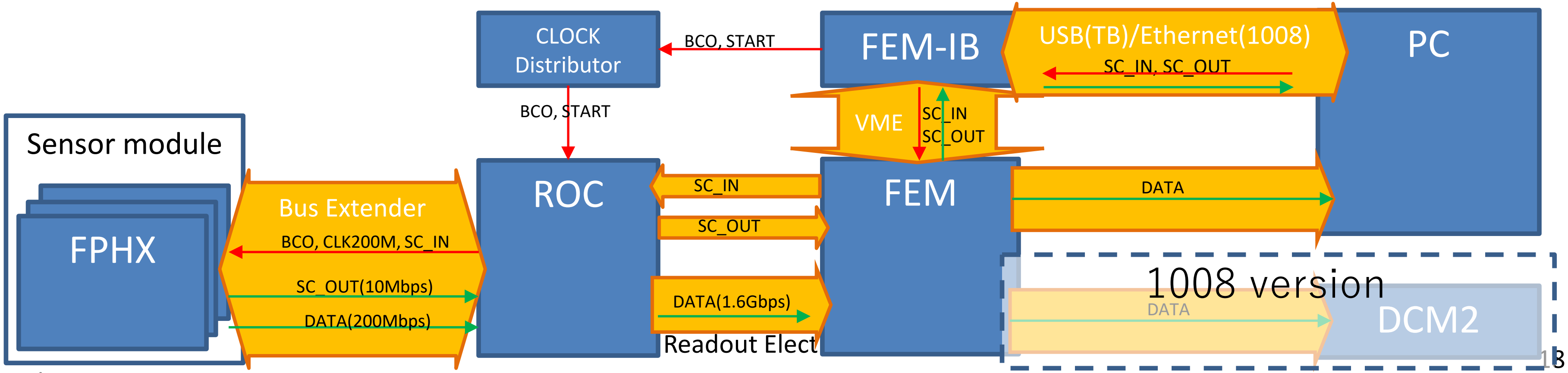
- Performance of single bus-extender is confirmed to be good for INTT
  - **Signal loss and reflection is ~30% and ~10%, respectively**
  - **Enough opening of EYE**
  - **Good mechanical strength for long term stability**
- Yield rate improved
  - **Small dust to be removed**
  - **Another production is running to evaluate the yield rate with new procedure**

- Ready for the mass-production
  - **Final length of the bus-extender under consideration**
    - **Expect to be slightly shorter**
  - **Improve the yield rate ~80% expected.**

Full Readout Chain

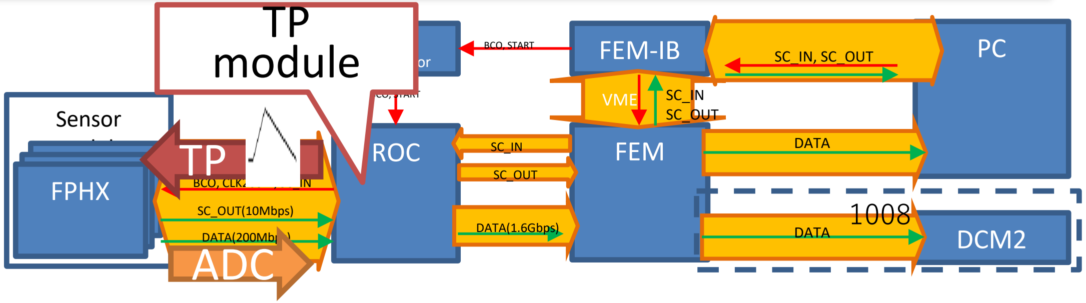
Readout, SlowControl & Readbacker

- Full Readout Chain
  - **20 bit /hit is generated at FPHX and sent to ROC w/ 200 Mbps**
- SlowControl
  - **Send the control command to FPHX and the readout electronics (FEM, FEMIB, ROC) w/ 10 Mbps**
  - **The SC commands set thresholds in FPHX, Channel masks, flash memory**
    - **Flash memory expected to be used for the initial values**
- Readbacker
  - **Useful to see the ladder condition remotely**

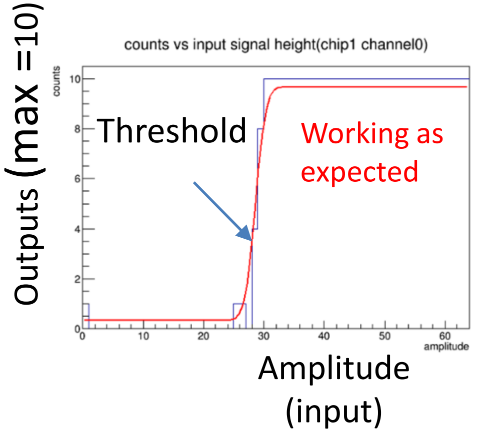


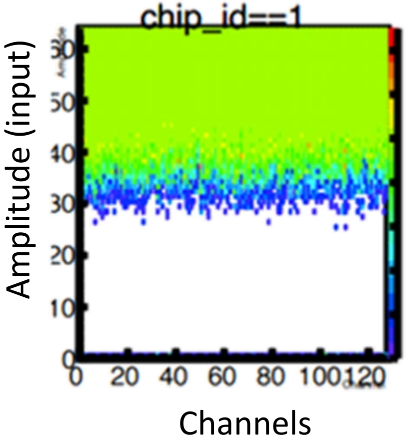
Full Readout chain with Test pulse

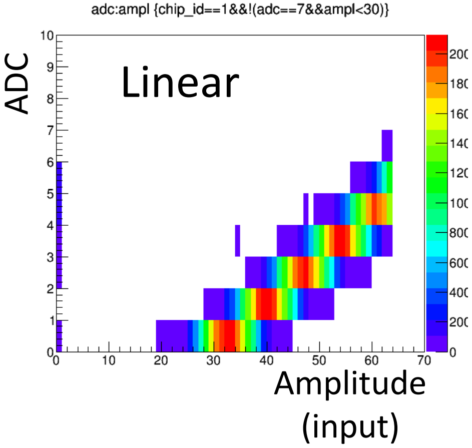
- TP module built-in at ROC
  - **10 TP / ch with amplitude of 0-63**
- Useful to see ch-by-ch response
  - **ADC threshold clearly seen**
  - **Linearity between ADC (output) vs amplitude (input)**
  - **Nhits/ch by TP should be 350**

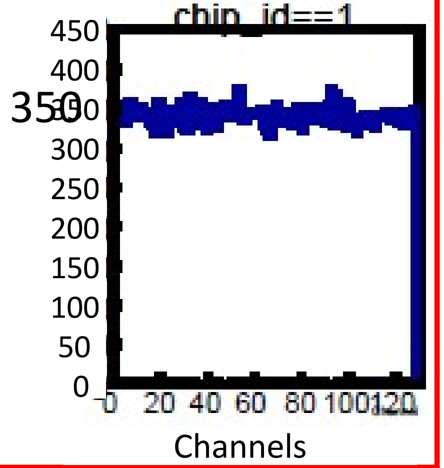


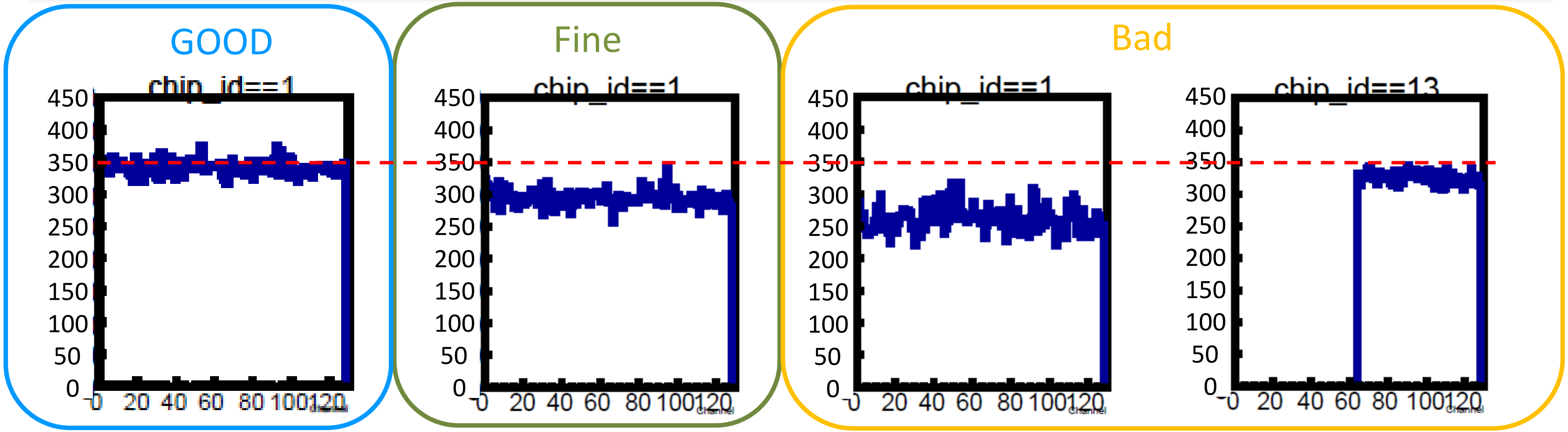
This could be used for QA of the data transmission











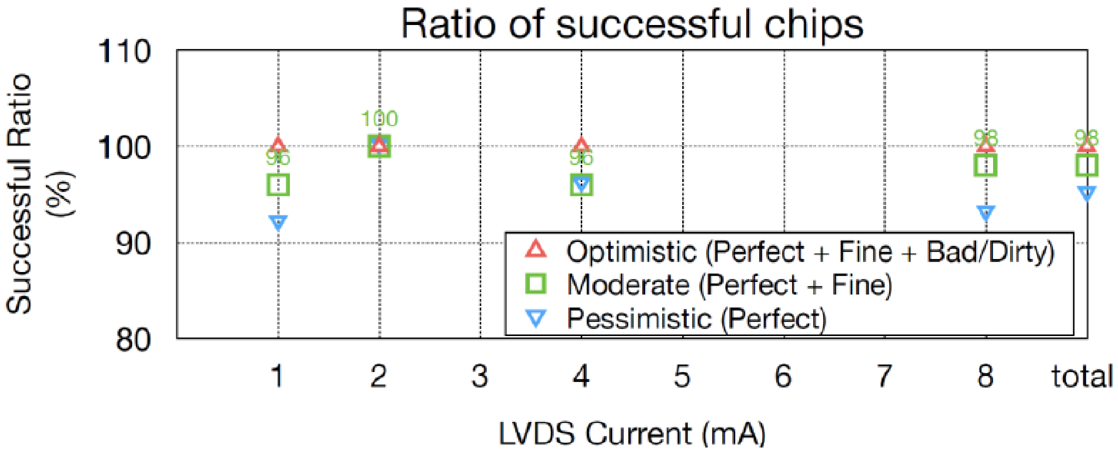
- GOOD: <N> ~ 350
- Fine :   <N> ~ 300
- Low Entry : <N> ~< 250
- Lost Channels :

Data transmission test W/O BEX

- Tested the data transmission by running TP repeatedly
  - **Drawing current of LVDS changed from 1,2,4 and 8mA**
  - **Testing 1 half ladder = 26 FPHX chips simultaneously**
- Results
  - **Transmission successful without BE for all LVDS currents**

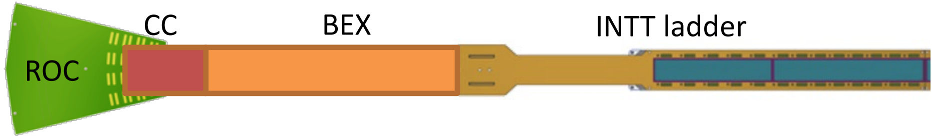
Performance of ROC SW5 port C3 (chip-wise)

LVDS (mA) \ Quality	Perfect	Fine	Bad/Dirty	Half entry, lost channels	Total
1	1196 92%	52 4%	52 4%	0 0%	1300 100%
2	1404 100%	0 0%	0 0%	0 0%	1404 100%
4	1248 96%	0 0%	52 4%	0 0%	1300 100%
8	2496 94%	130 5%	26 1%	4 0%	2656 100%
Total	6344 95%	182 3%	130 2%	4 0%	6660 100%



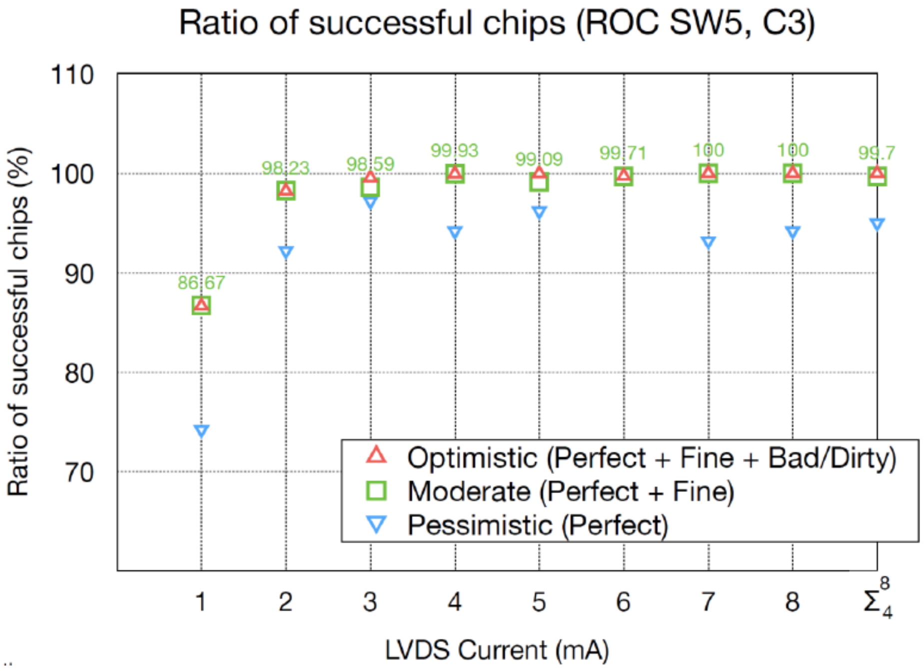
Data transmission test W/ BEX

- Add bus-extender to the data path
- Results
  - **Ratio increase w/ LVDS currents**



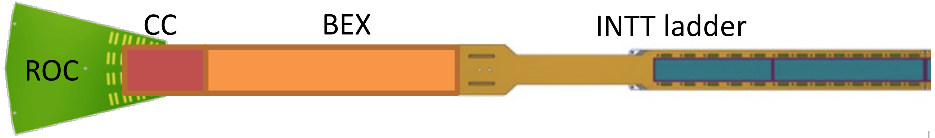
Ratio of successful chips with the bus extender (ROC SW5-C3)

LVDS (mA) \ Quality	Perfect	Fine	Bad/Dirty	Half entry	Total
1	442	78	0	80	600
	74%	13%	0%	13%	100%
2	1196	78	0	23	1297
	92%	6%	0%	2%	100%
3	2600	52	26	12	2690
	97%	2%	1%	0%	100%
4	3952	234	0	3	4189
	94%	6%	0%	0%	100%
5	2834	104	26	1	2965
	96%	4%	1%	0%	100%
6	338	0	0	1	339
	100%	0%	0%	0%	100%
7	364	26	0	0	390
	93%	7%	0%	0%	100%
8	1560	104	0	0	1664
	94%	6%	0%	0%	100%
Σ_4^8	9048	468	26	5	9547
	94.8%	4.9%	0.3%	0.1%	100%



Data transmission test W/ BEX

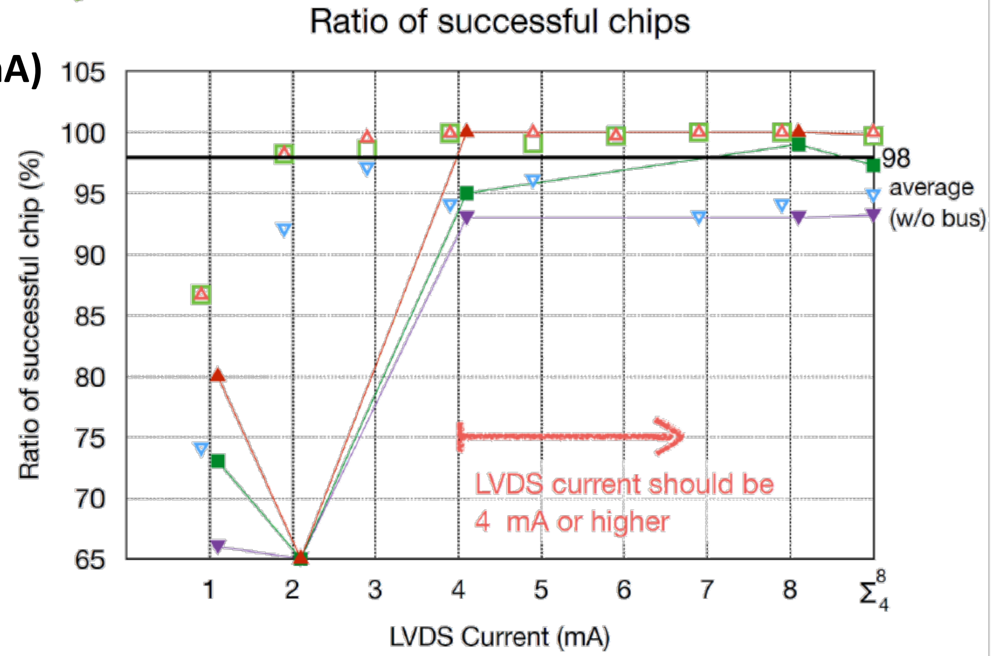
- Add bus-extender to the data path
- Results
  - Ratio increase w/ LVDS currents
  - Ratio ~ 100% at LVDS >= 4mA (FVTX = 2mA)



Ratio of successful chips (ROC SW5, C3)

Quality / LVDS (mA)	Perfect	Fine	Bad/Dirty	Half entry	Total
1	234 66%	26 7%	26 7%	70 20%	356 100%
2	156 65%	0 0%	0 0%	83 35%	239 100%
3					
4	1092 93%	26 2%	52 4%	5 0%	1175 100%
5					
6					
7					
8	1846 93%	104 5%	26 1%	1 0%	1977 100%
4mA +8mA	2938 93.2%	130 4.1%	78 2.5%	6 0.2%	3152 100%

2 different ports at ROC

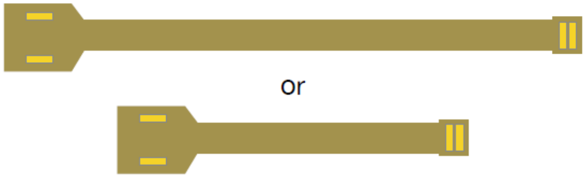


Data transmission w/ Bus-Extender successful

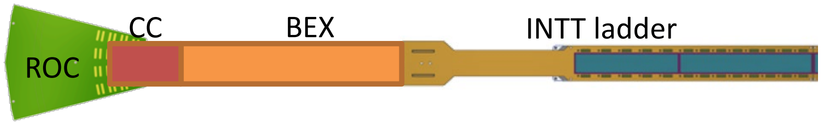
Continue further investigation w/ different setups

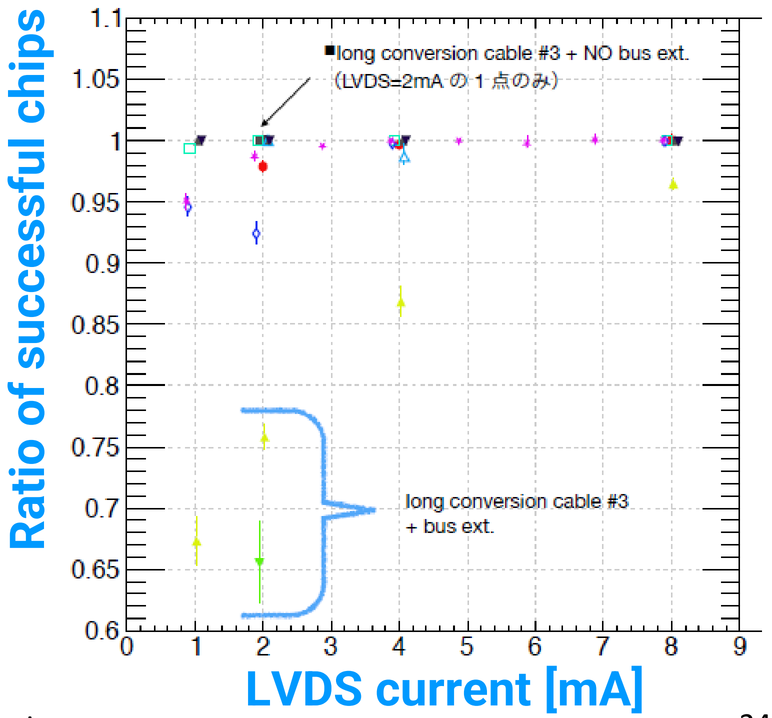
Conversion cable

- 20cm and 40cm CC w/ BEX is tested
  - **20cm successful**
  - **40cm sometime failed**
    - **Larger LVDS current improve the signal transmission**
  - **Further investigation in progress**
    - **The designs are same except for the length**



- INTT uses smaller Bus-Extender and CC (<40cm) at 1008
  - **Smaller Signal loss and distortion expected**

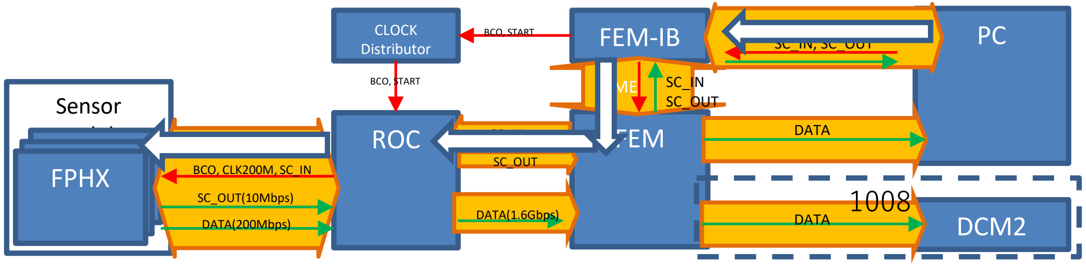


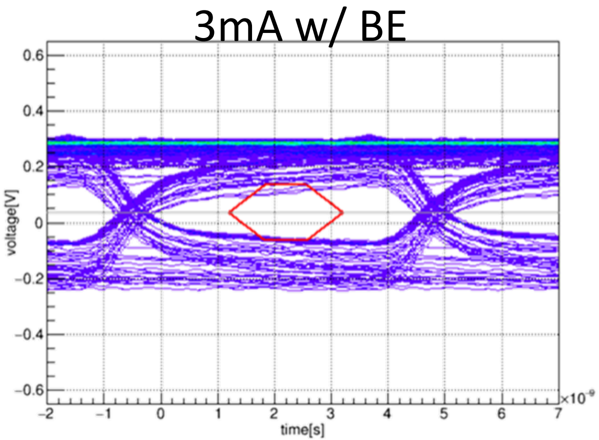


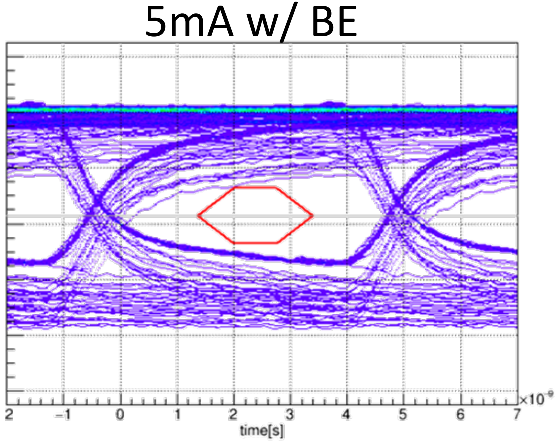
Slow Control

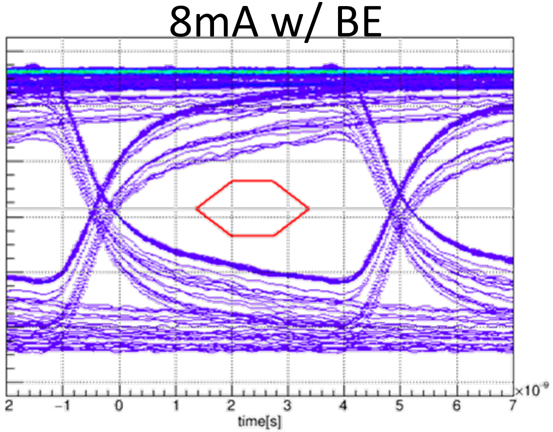
Initialize FPHX with Slow Control

- Tested that SC initialize the registers for each FPHX
- Example: LVDS current changed to 3, 5, 8mA





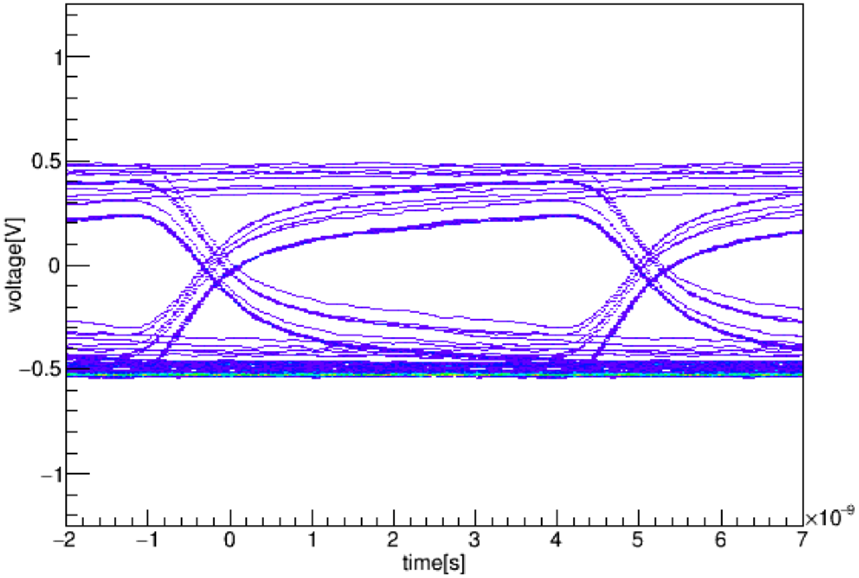




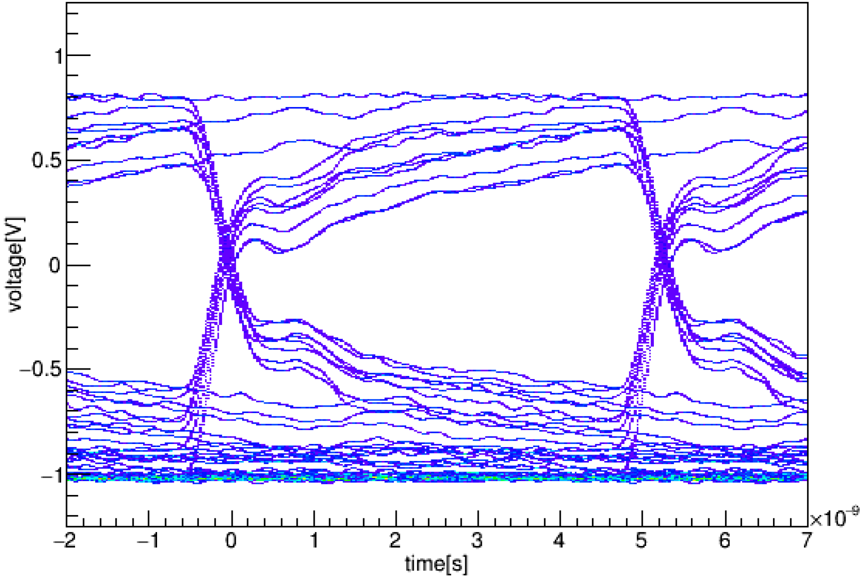
Signals after ROC regulator upgrade

All ROC regulators were replaced from 2.5V to 3.0V to compensate the voltage drop

Before



After

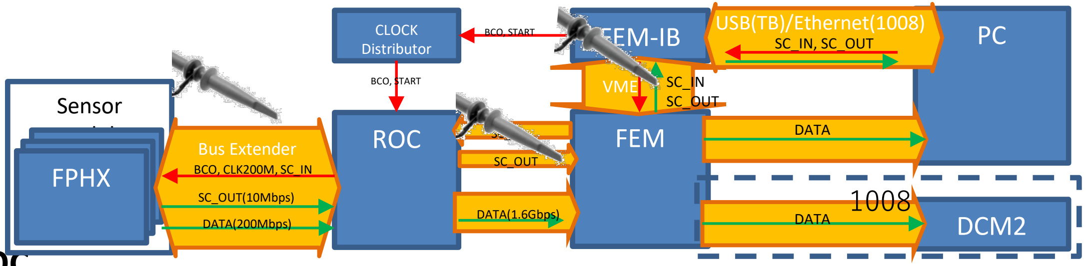


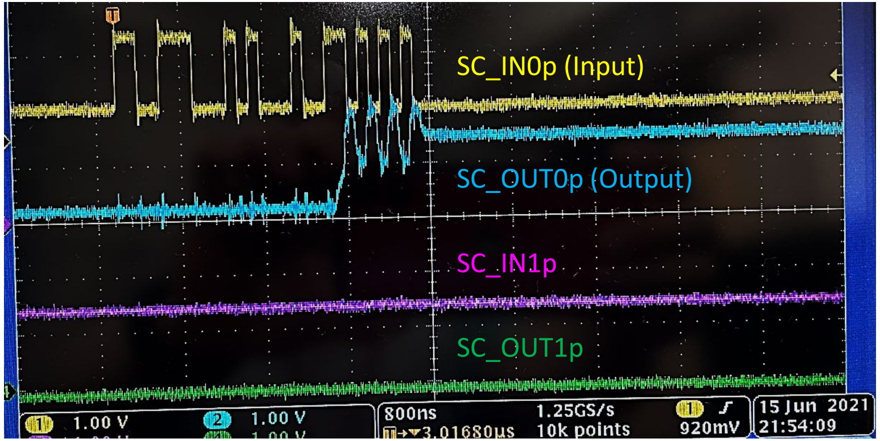
- LVDS signal heights matches 8mA setting after the regulator upgrade
  - **8mA setting → 0.5V : Power was not enough to drive 8mA before the upgrade**

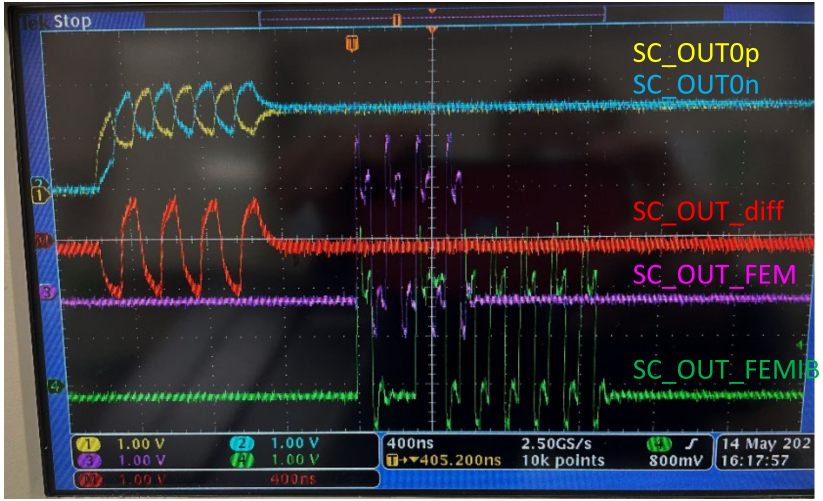
Readbacker at GUI

Readback pulse

- Send the SC command to the chip.
  - **SC commands and Readback values are monitored on the interception board**
- Readback signal reach to FEM-IB
  - **Transmitted from FPHX to FEM-IB via ROC and FEM.**
  - **Header (b_10001101) added at FEM**







Readbacker at GUI

- Readbacker is tested at the NWU test bench.
- Readbacker works at the test bench in Nara and RIKEN.
  1. **Readback value is the same with what we set to the register**
  2. **Readback value is the same with the default in hardware after reset**
- The readbacker needs to be implemented with FELIX readout system

1:Readback = setting

Reg	Desc	To Chip	From Chip		Ch
*	Wild	0		Read	Write
1	Mask	0		Read	Write
2	Dig Ctrl	5	7	Read	Write
3	Vref	1	1	Read	Write
4	DAC0	20	20	Read	Write
5	DAC1	25	25	Read	Write
6	DAC2	30	30	Read	Write
7	DAC3	35	35	Read	Write
8	DAC4	40	40	Read	Write
9	DAC5	45	45	Read	Write
10	DAC6	50	50	Read	Write
11	DAC7	55	55	Read	Write
12	N1Sel <3:0>	6	6	Read	Write
	N2Sel <7:4>	4	4		
13	FB1Sel <3:0>	4	4	Read	Write
	.eakSel <7:4>	0	0		
14	P3Sel <1:0>	0	0	Read	Write
	P2Sel <7:4>	4	4		
15	GSel <2:0>	2	2	Read	Write
	BWSel <7:3>	8	8		
16	P1Sel <2:0>	5	5	Read	Write
	InjSel <5:3>	0	0		
17	LVDS Current	3	3	Read	Write
18	Resets	n/a		Read	Write

2: Readback = HW default

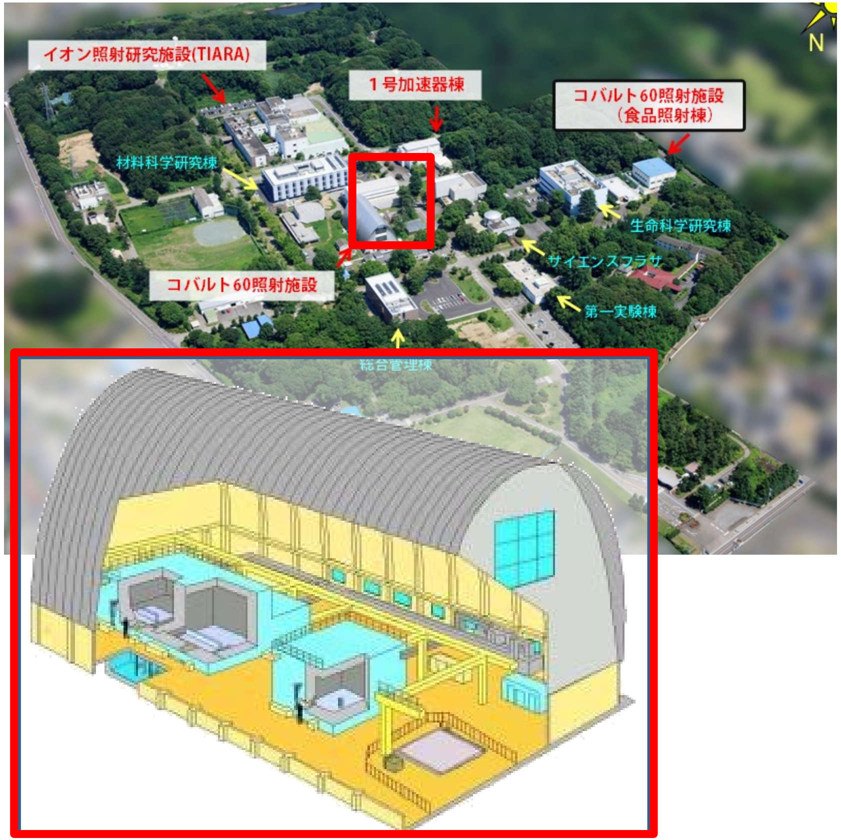
Reg	Desc	To Chip	From Chip	
*	Wild	0		Read
1	Mask	0		Read
2	Dig Ctrl	5	1	Read
3	Vref	1	1	Read
4	DAC0	20	8	Read
5	DAC1	25	16	Read
6	DAC2	30	32	Read
7	DAC3	35	48	Read
8	DAC4	40	80	Read
9	DAC5	45	112	Read
10	DAC6	50	144	Read
11	DAC7	55	176	Read
12	N1Sel <3:0>	6	6	Read
	N2Sel <7:4>	4	4	
13	FB1Sel <3:0>	4	4	Read
	.eakSel <7:4>	0	0	
14	P3Sel <1:0>	0	0	Read
	P2Sel <7:4>	4	4	
15	GSel <2:0>	2	1	Read
	BWSel <7:3>	8	4	
16	P1Sel <2:0>	5	5	Read
	InjSel <5:3>	0	0	
17	LVDS Current	170	170	Read
18	Resets	n/a		Read

Summary

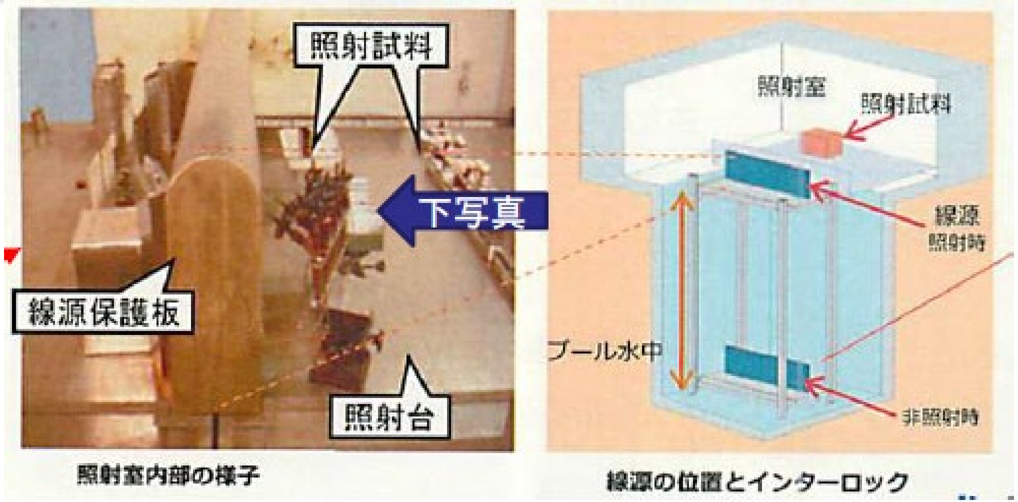
- Bus-Extender, Long and High Density Flexible Cable, is technically most challenging part on the INTT development.
- Bus-Extender is ready for the mass production
  - **Final length of the bus-extender under consideration**
    - **Expect to be slightly shorter: 1.1m instead of 1.2m (prototyping it works)**
  - **Improve the yield rate.**
- Data’s transmission w/ BEX is successful with the test pulse, the source test is in progress
- All ROC regulator (2.5V -> 3.0V) were replaced, leading to obtain very good test results.
- Slow Control and Register readback work successfully at the test bench

backup

QST lab



N
イオン照射研究施設(TIARA)
1号加速器棟
コバルト60照射施設
(食品照射棟)
材料科学研究棟
生命科学研究棟
サイエンスプラザ
コバルト60照射施設
第一実験棟



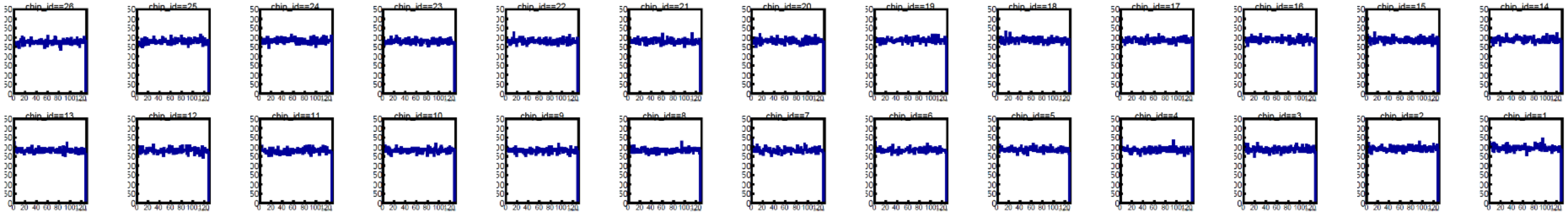
照射試料
下写真
線源保護板
照射台
照射室内部の様子
照射室
照射試料
線源
照射時
プール水中
非照射時
線源の位置とインターロック

Co
ステンレス
2重のステンレスチューブに封入された線源(模型)
1本の線源は最大約9g
の⁶⁰Co(約9×10²²原子)
を含有(1万Ci (0.37PBq))

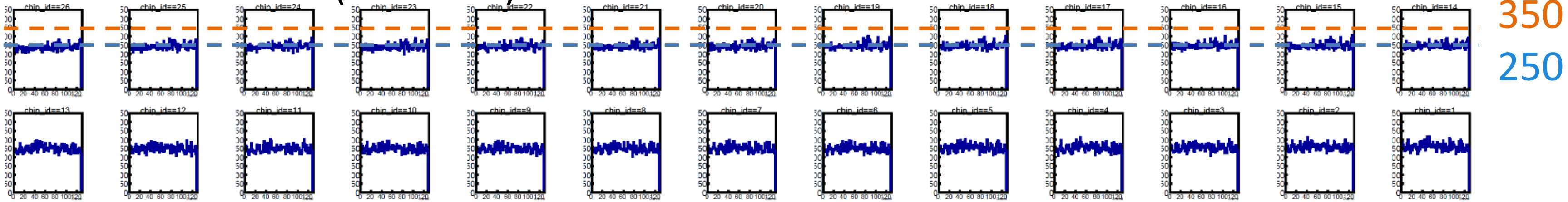
上からみた線源

TP results : Fine and BAD

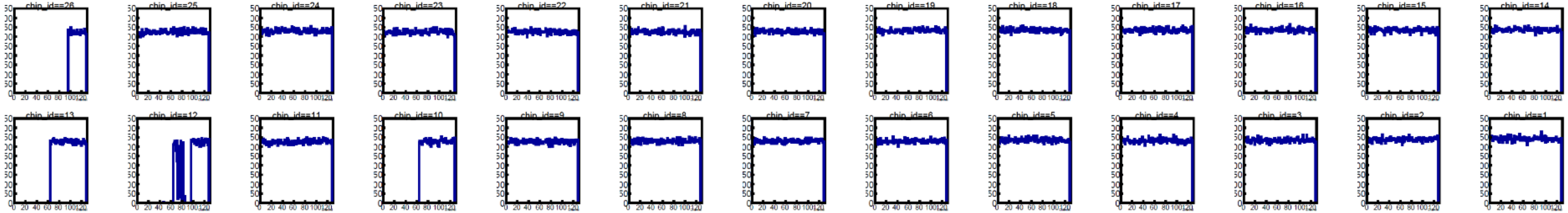
Fine (N < 300)



BAD1: less entries (N ~< 250)

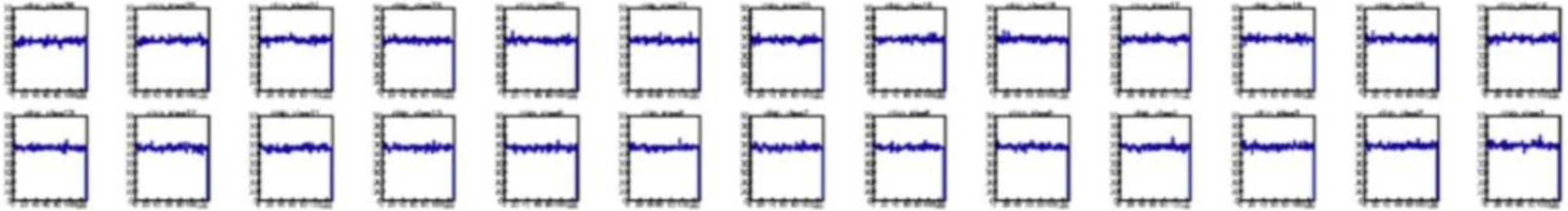


BAD2: Lost channels

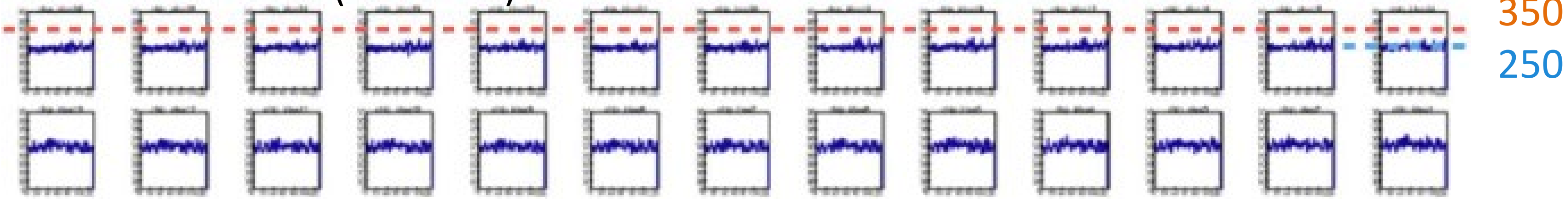


TP results : GOOD and BAD

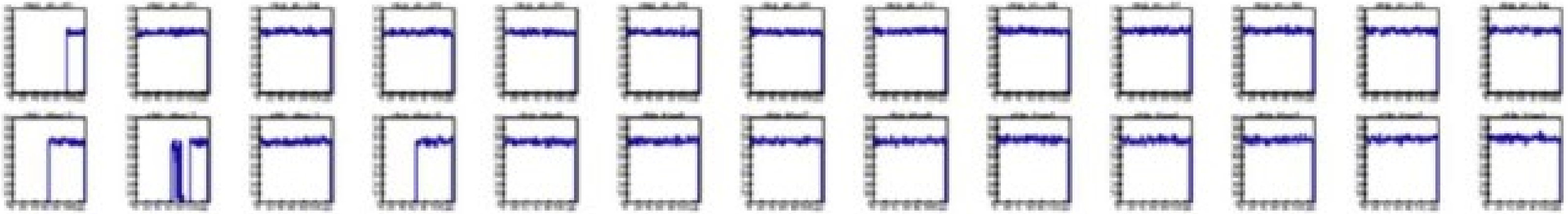
Fine (N < 300)



BAD1: less entries (N ~< 250)

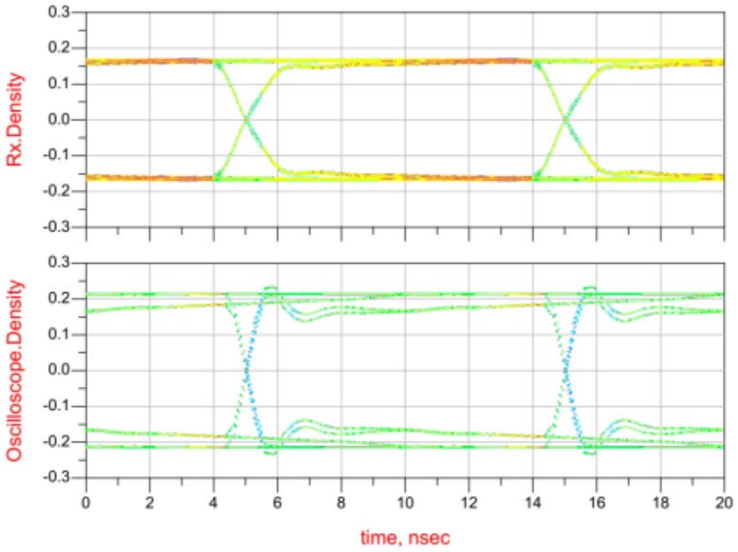


BAD2: Lost channels



Interception board

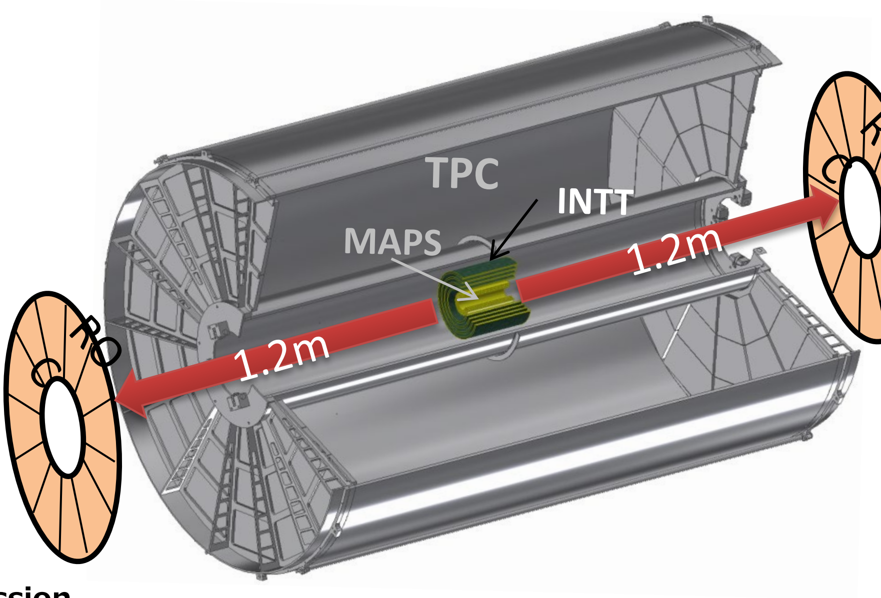
- The interception board is designed to measure the signal pulse of data transmitting between the ladder and ROC.
  - **Useful for debugging and QA**
- The side effect by the interception board is a distortion of the pulse



Long and High Density Flexible Cable

Requirements of the data cable for INTT

- **Long ~ 120cm**
- **Dense = 62 pairs of the signal line (and power/GND)**
- **High speed =200 Mbps LVDS (Z_{diff}=100Ω)**
- **Tight space ~5cm and curving path**
- **(re)use the FVTX ROC**



No commercial cable available in the market

- Develop the cable based on the FPC technology
  - **Flexible and can be micro-fabricated**

- Very long FPC is challenging
  - **No fabrication machine for 120cm FPC**
  - **Large signal loss by 120cm during the signal transmission**
  - **Keep line & space precisely for whole length**
    - **Make the circuit open/short easily if the line width is fluctuated**

Electrical and mechanical performance studied and production procedure developed

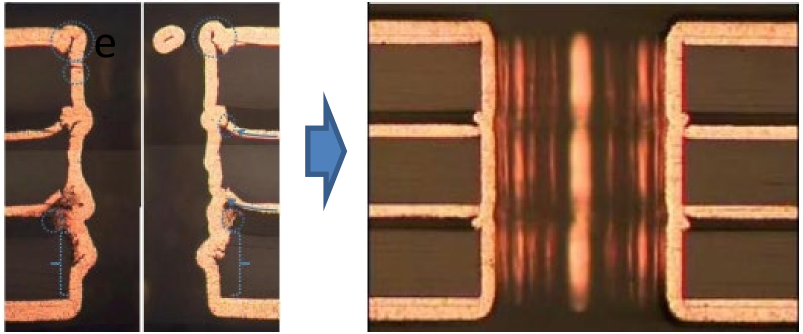
Self-test completed

- Issues solved
  - Nodule structure on Cu-plating of the throu-hole
  - Week peel strength

The new adhesive sheet fixs the issues.

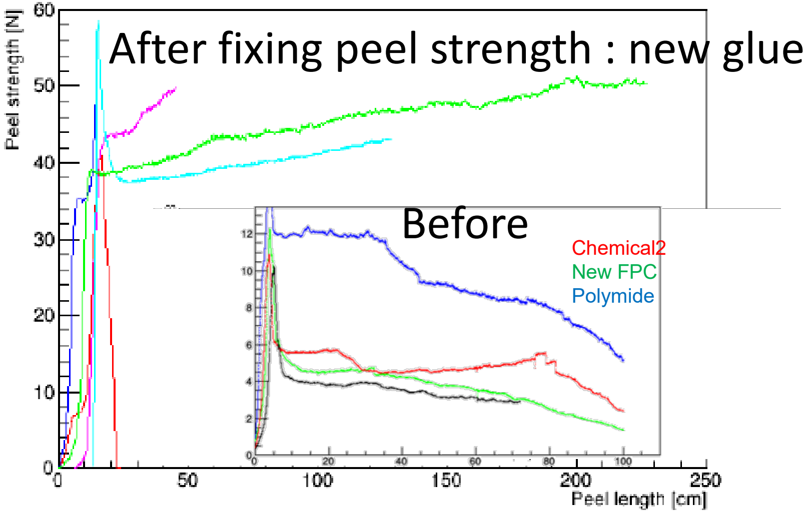
Nodul
e

Smooth



- Additional tests reported by M. Morita
  - Signal measurement with full readout chain
  - Radiation hardness test

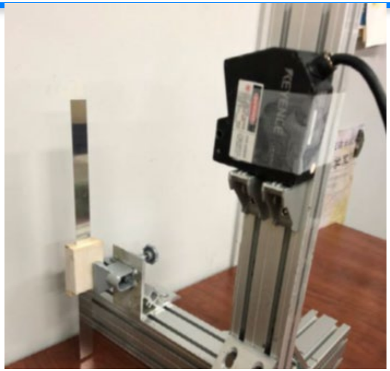
Ready for the mass production

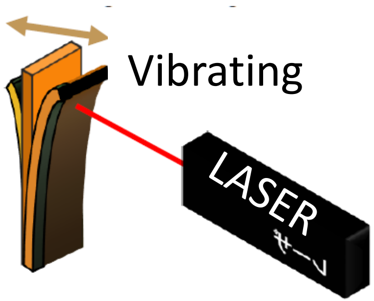


Evaluation methods

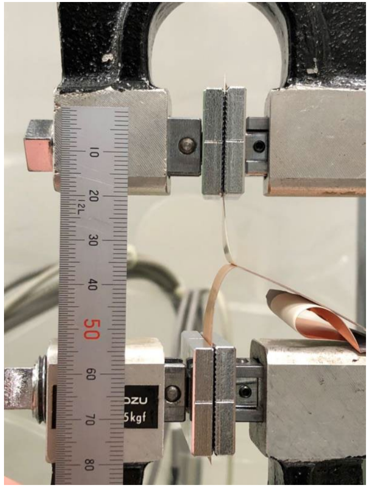
- Young's modulus
  - **Vibrate the sample and measure the natural freq. by the LASER system**

> Natural frequency to Young's modulus
>
> $$f_n = a\,E$$
>
> fn : Natural frequency
> E : Young's modulus,
> a,b : coefficients



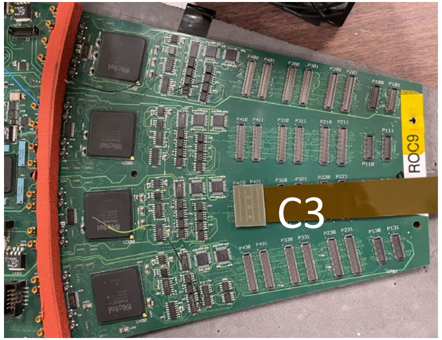


- Peel strength
  - **Sample peeled off with 180 degree and measure its strength by a tensile tester**

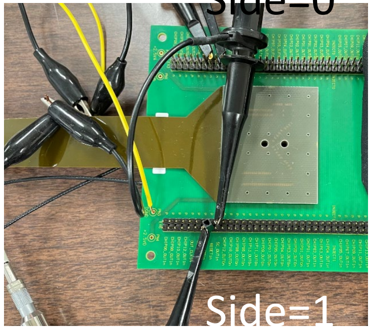


Additional test to send the SC to the chip

- Send the SC command to the chip of interest.
  - **SC commands and Readback values are monitored on the IC board**
- The test is successful

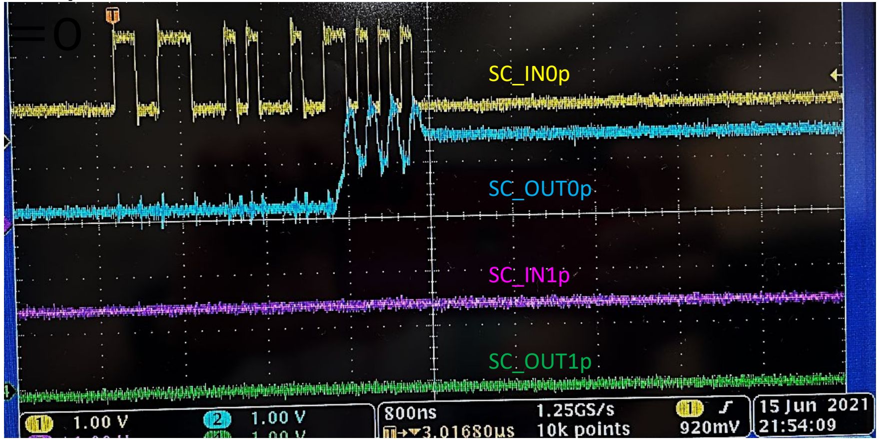


Side=0

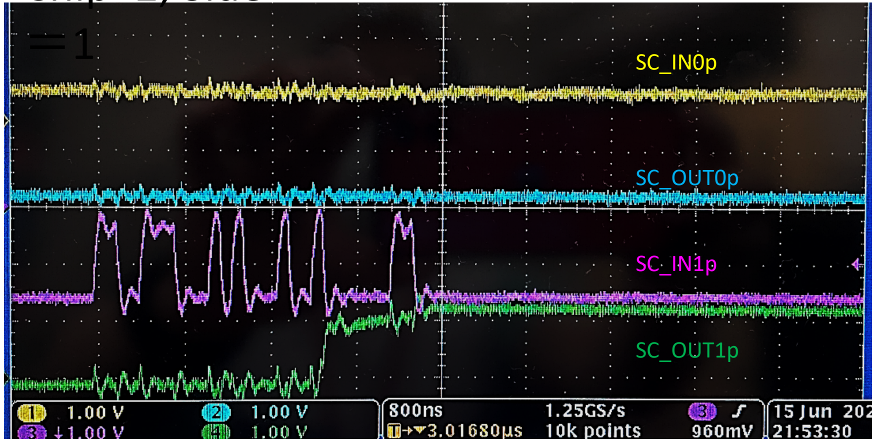


Side=1

Chip=2, Side=0

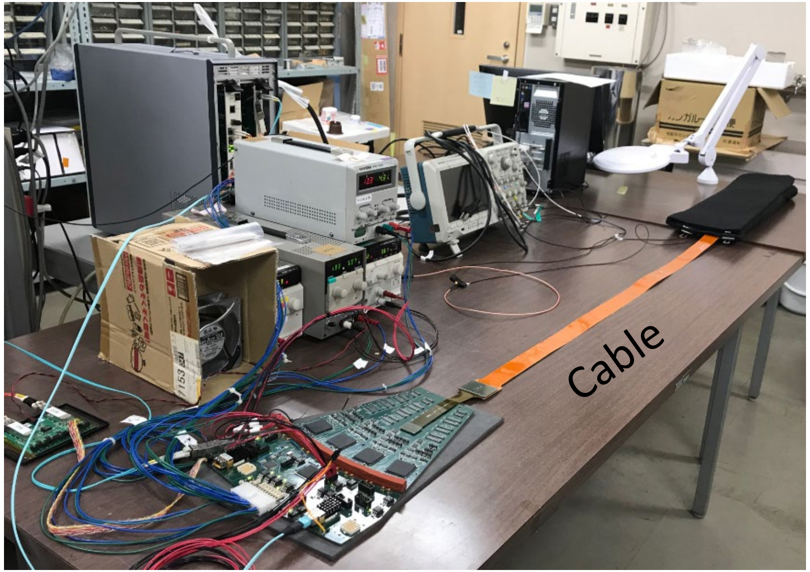


Chip=2, Side=1



BEX for INTT and FVTX

- BEX for INTT is much longer than that for FVTX
  - **LCP used for small signal loss**
- Technically challenging
  - **Small signal loss**
  - **Stable Zdiff for the length**



	FVTX	INTT
Length	10~30 cm	**120cm**
Layer	7	4
Signal	62 pairs (LVDS)	62 pairs
Power	V-a, V-d, GND	V-a, V-d, GND
Substrate	Polyimide	LCP
Impedance	50	50