



Evaluation of INTT

Nara WU : Miu Morita



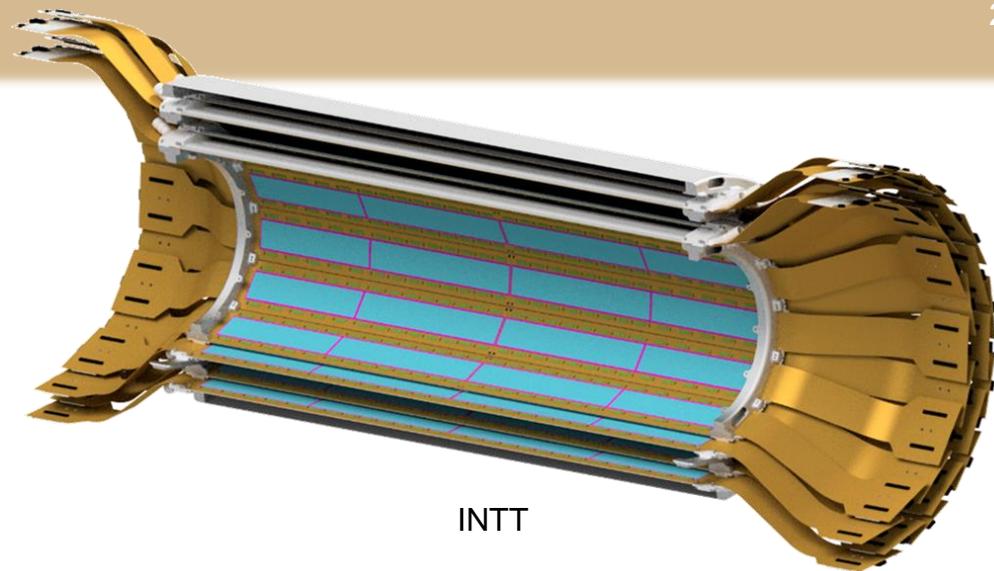
Parameters

FPHX chip

1. Threshold setting (DAC)
 2. Effect of noise
 3. Efficiency
 4. Bonded wire
- > is there anything else?

Sensor

- Rate (number of events per unit time)
- Efficiency (compare with PMT)



We have to check that if it's sufficient to meet the required performance of INTT

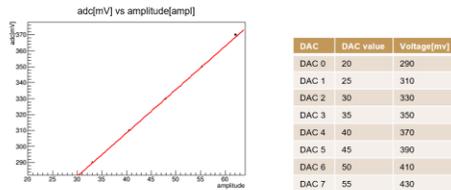
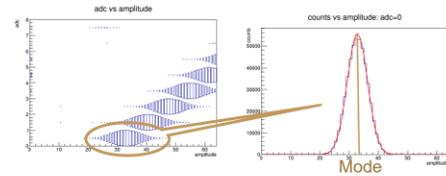




1. Threshold setting (DAC)

🍦 Calculate and Offset every channel 3

- It has positive relationship between amplitude(input) and adc(output)
- Decide amplitude Mode value by fitting gaussian each adc
- Guess offset using $Voltage[mV] = 4 * DAC\ value + 210$
- Slope means correlation coefficient between amplitude(input) and adc[mV](output)

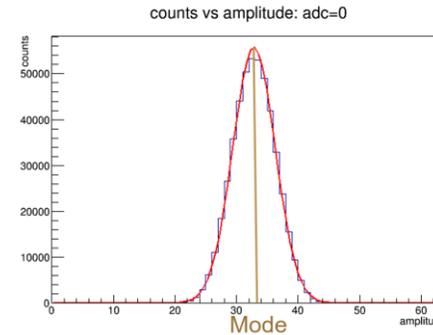


2020/08/05

HEPL in NWU: Miu Morita

🍦 Calculate and Offset every channel 5

- This is histogram whose X-axis is amplitude(input) when adc==0
- Fit gaussian and chose amplitude mode value

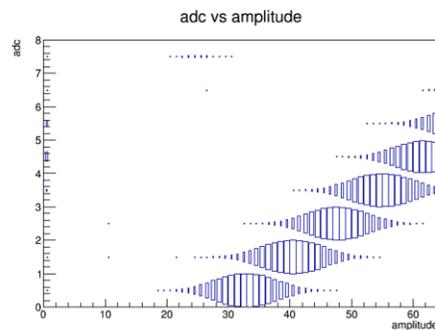


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HEPL in NWU: Miu Morita

🍦 Calculate and Offset every channel 4

- This is two-dimensional histogram adc(output) vs amplitude(input)
- Blue box issue hits number rate
- It has positive relationship between amplitude(input) and adc(output)

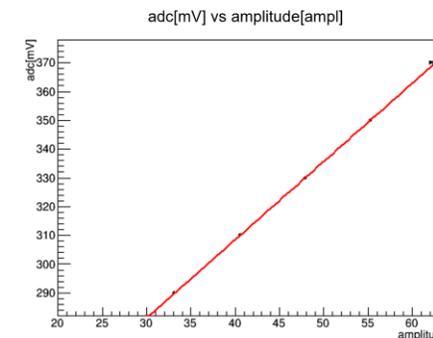


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HEPL in NWU: Miu Morita

🍦 Calculate and Offset every channel 6

- This is graph adc[mV] vs amplitude[amp]
- Plot amplitude mode value every adc
- It has positive relationship between amplitude(input) and adc(output)



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2. Effect of noise

Algorithm introduction : width

- For each channel of each chip :
 - Center line : average of events in "Block 0" (ADC==0)
 - Centers of the rest blocks are aligned to center line.
 - Amount of movement : Mean of each block - center line
 - Each event is filled in TH1F, and fit with gaussian.

Cheng-Wei Shih (NCUHEP, Taiwan)

Algorithm introduction : width

The Gaus width of most channels are less than 4
Gaus width > 4 will be shown in right plot

Cheng-Wei Shih (NCUHEP, Taiwan)

3. Efficiency

Algorithm introduction : ampl cut (not use so far)

- New entry criteria candidate : applying a ampl cut.

The width of gaussian is mainly contributed by the fluctuation around DAC0.

Cheng-Wei Shih (NCUHEP, Taiwan)

Which performance

Algorithm introduction : entry

Cheng-Wei Shih (NCUHEP, Taiwan)

Calibration tests, Ratio of successful chips

| ROC | port | LVDS = 1 mA | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|-----|------|-------------|-----|-----|-----|-----|----|-----|-----|
| NW1 | A2 | 3 | | | | | | | |
| NW1 | C3 | 29 | 20 | | | | | | |
| SW5 | A1 | 11 | | | | | | | |
| SW5 | A2 | 56 | 56 | 50 | | | | 102 | |
| SW5 | A3 | 3 | | | | | | | |
| SW5 | C1 | 3 | | | | | | | |
| SW5 | C2 | 4 | | | | | | | |
| SW5 | C3 | 115 | 122 | 115 | 215 | 115 | 15 | 15 | 185 |
| 7 | A1 | 7 | | | | | | | |
| 7 | A2 | 5 | | | | | | | |
| 7 | A3 | 5 | | | | | | | |
| 7 | C1 | 17 | | | | | | | |
| 7 | C2 | 3 | 57 | 53 | | | | | 53 |
| 7 | C3 | 3 | | | | | | | |
| NE2 | A1 | 8 | | | | | | | |
| NE2 | A2 | 37 | 405 | 5 | 104 | 8 | 4 | 4 | 4 |
| NE2 | C1 | 224 | 253 | 223 | | | | | 228 |

Data points with less than 10 runs not analyzed.

Definition of a chip with half entry :
 $12700 \times 40\% < \text{entry} < 12700 \times 60\%$
 total entries for a chip:
 $12700 \times 40\% < \text{entry}$
 Ratio of successful ratio:
 half entry / total entry

0<ch<128 (ch 0 ignored since noise data tends to be there as well)
 53 < ampl < 65 (only stable area)
 $\rightarrow 127 \times 10 \times 10 = 12700$ events/chip in ideal cases

Made by Genki.Nukazuka

4. Bonded wire

Algorithm introduction : un-bonded channel (I am working this)

- The un-bonded channel should be considered as bad channel, it can be checked by running calibration test without bias voltage.
- One un-bonded channel was found in BNL ladder (PPB2-L2N)
File : fphx_raw_20210212-0942_0.dat

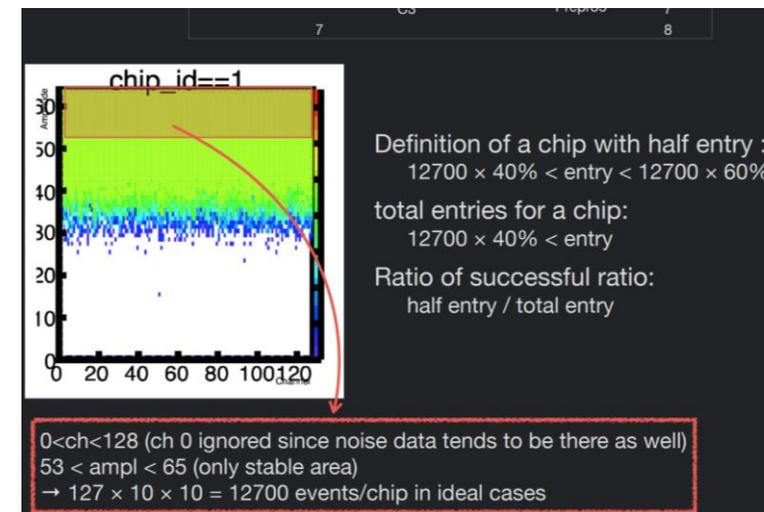
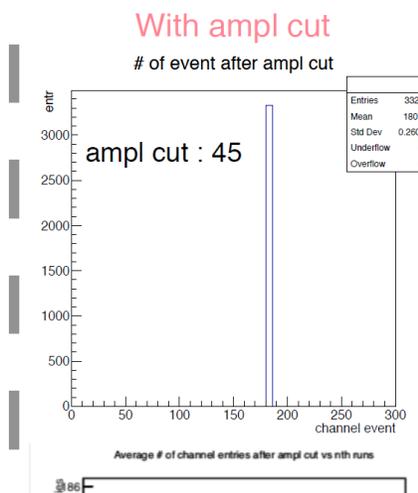
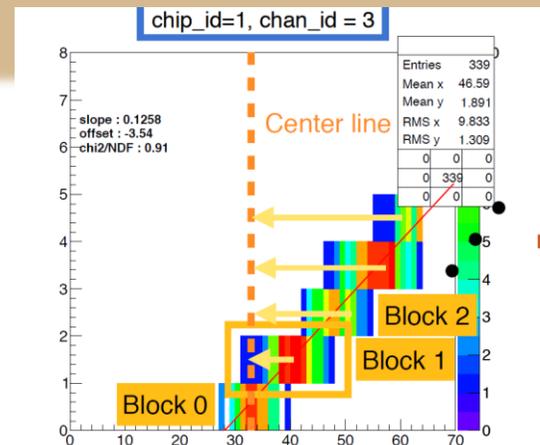
Calibration file without bias voltage

Cheng-Wei Shih (NCUHEP, Taiwan)



criteria

1. Threshold setting (DAC)
->What value is good?
2. Effect of noise
->I wonder it is good to stack blocks of different widths
3. Efficiency
->why they use these value?
4. Bonded wire
->What value do we set as threshold?



I think we discuss the value that we should use as criteria before proceeding with the evaluation

- We have 4 methods of calculation for evaluating FPHX chip now
- But the value of criteria of these is not decided with reason
- I think we discuss the value that we should use as criteria before proceeding with the evaluation

Back Up



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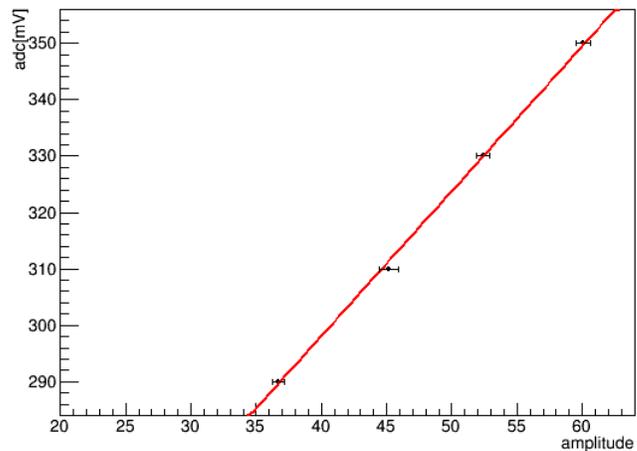




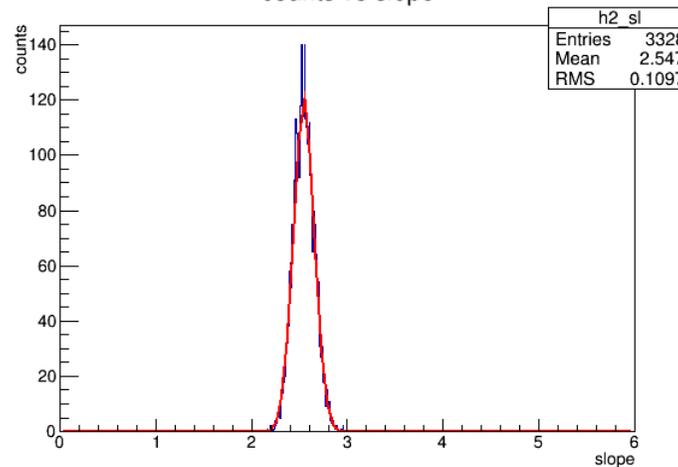
Slope and offset

| | | | |
|-----|----------|---------------|------|
| roc | roc_port | conversionbus | LVDS |
| NE2 | A2 | s8 | 2mA |

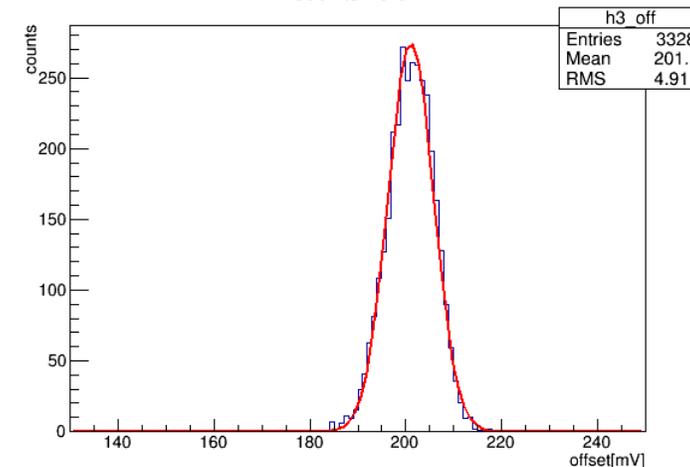
Graph



counts vs slope



counts vs off





Data Analysis

- Evaluate the threshold using the test pulse data
- Compare the threshold value w/ and w/o Bus Extender

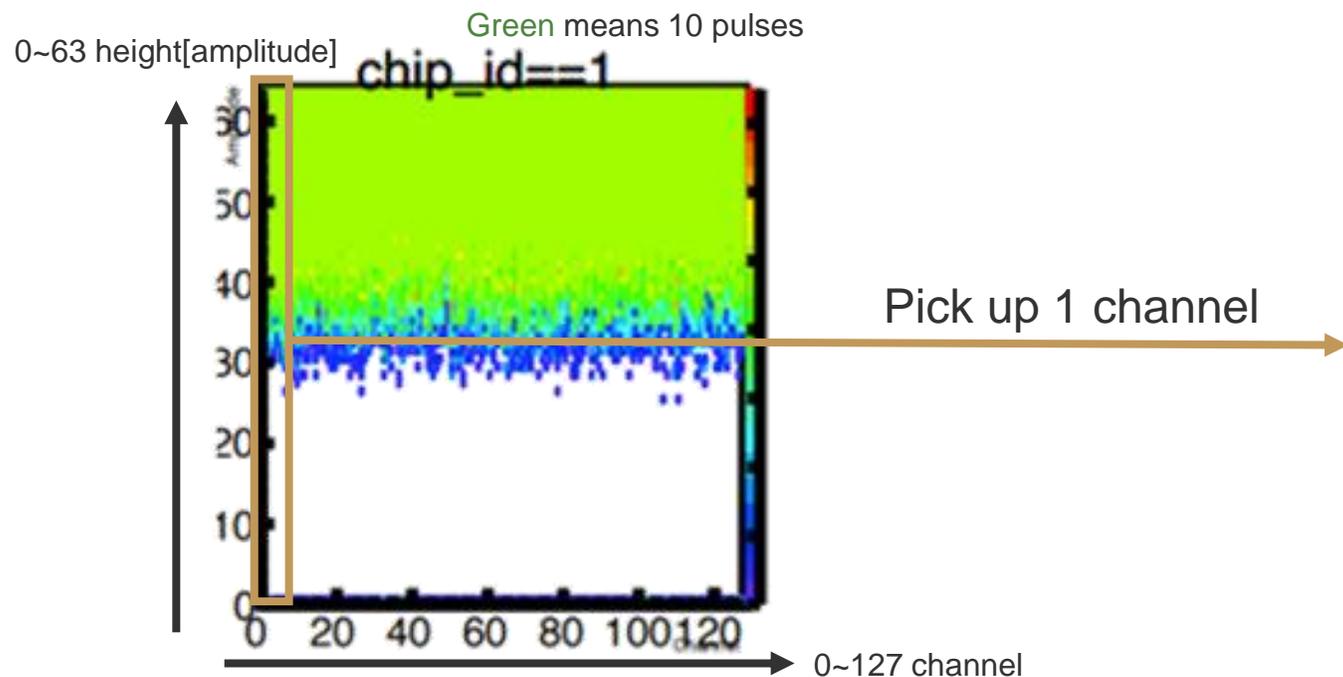
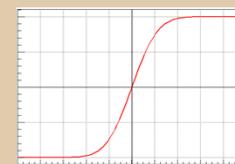
Calculate parameter from Fit function

Fit func : $f(x) = [p0] \times \text{erf}((x - [p1]) / [p2]) + 5$

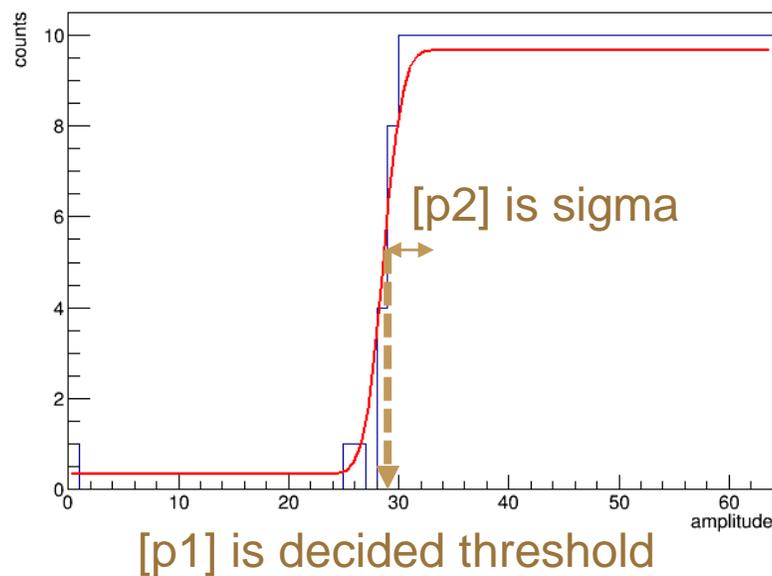
※[p0], [p1] and [p2] are parameters

Error func : erf(x)

$$\text{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt$$



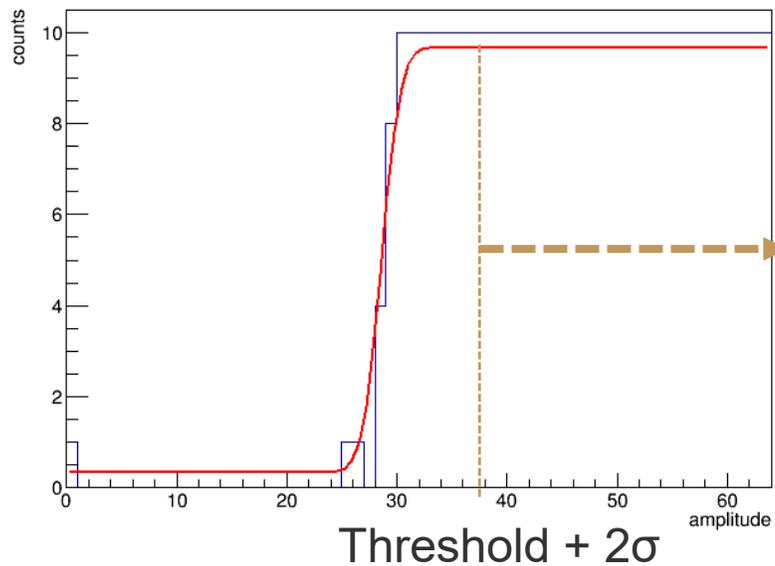
counts vs input signal height(chip1 channel0)





Rate

counts vs input signal height(chip1 channel0)

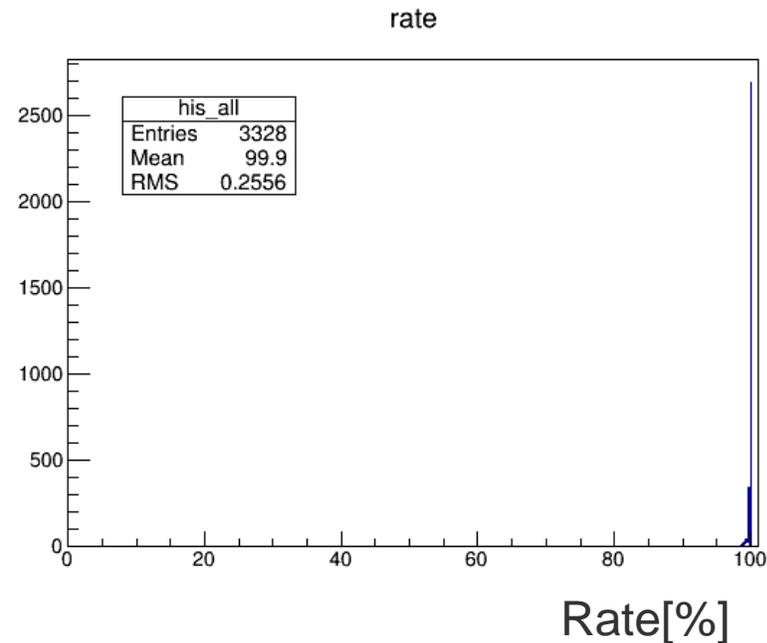


Rate calculation

$$rate(\%) = \left(1 - \frac{\Delta A}{\langle A \rangle}\right) \times 100$$

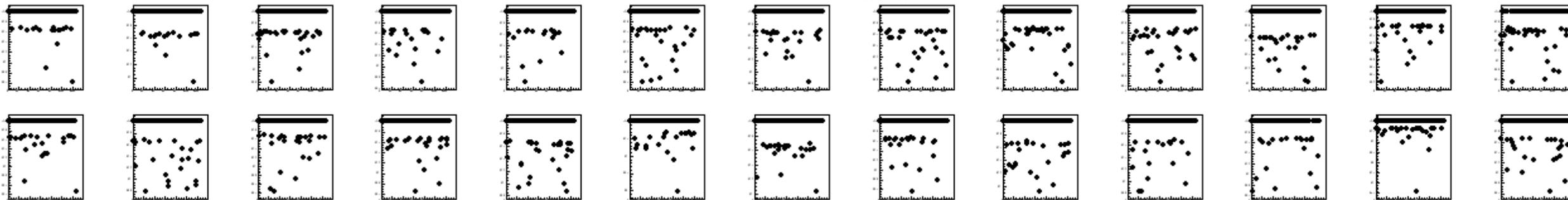
$$\Delta A = \frac{\sum_n \sqrt{(A_i - \langle A \rangle)^2}}{N}$$

A_j : actual data
 $\langle A \rangle$: 10
 ΔA : differential from 10 to actual data
 N : 64 - (threshold + 2σ)



Rate[%]

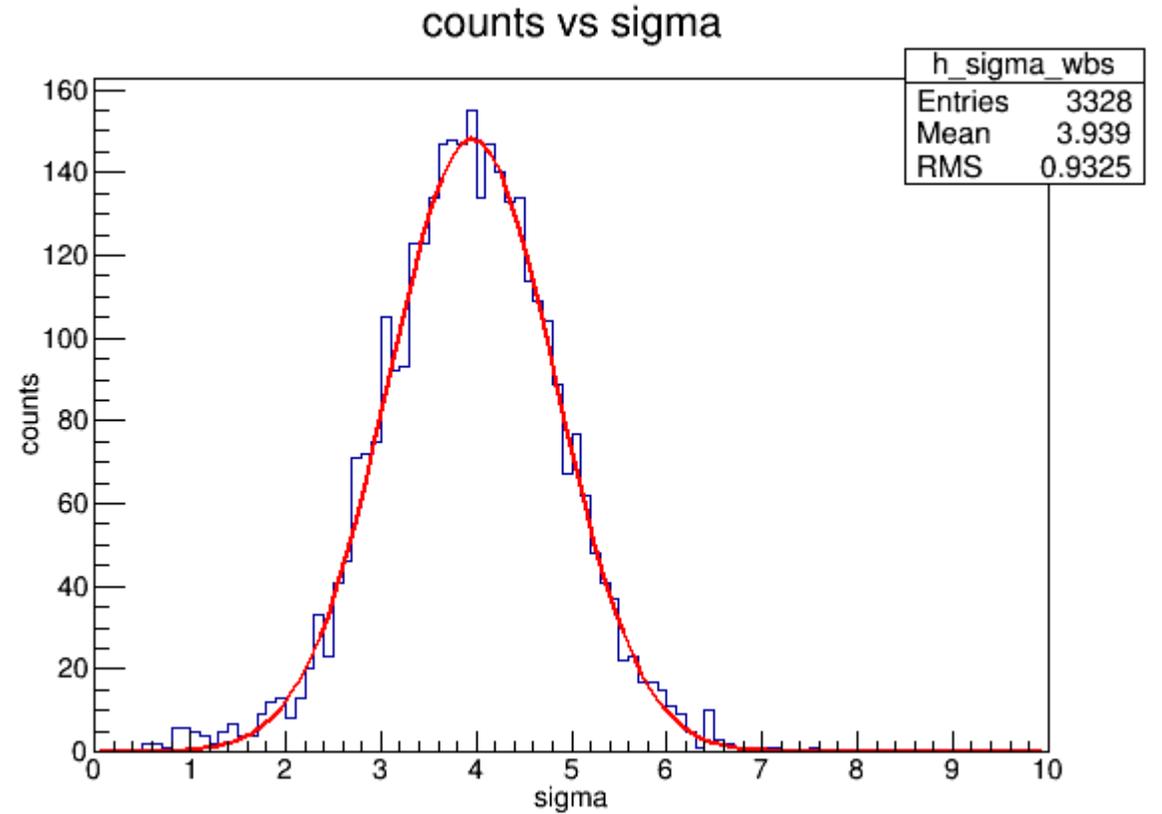
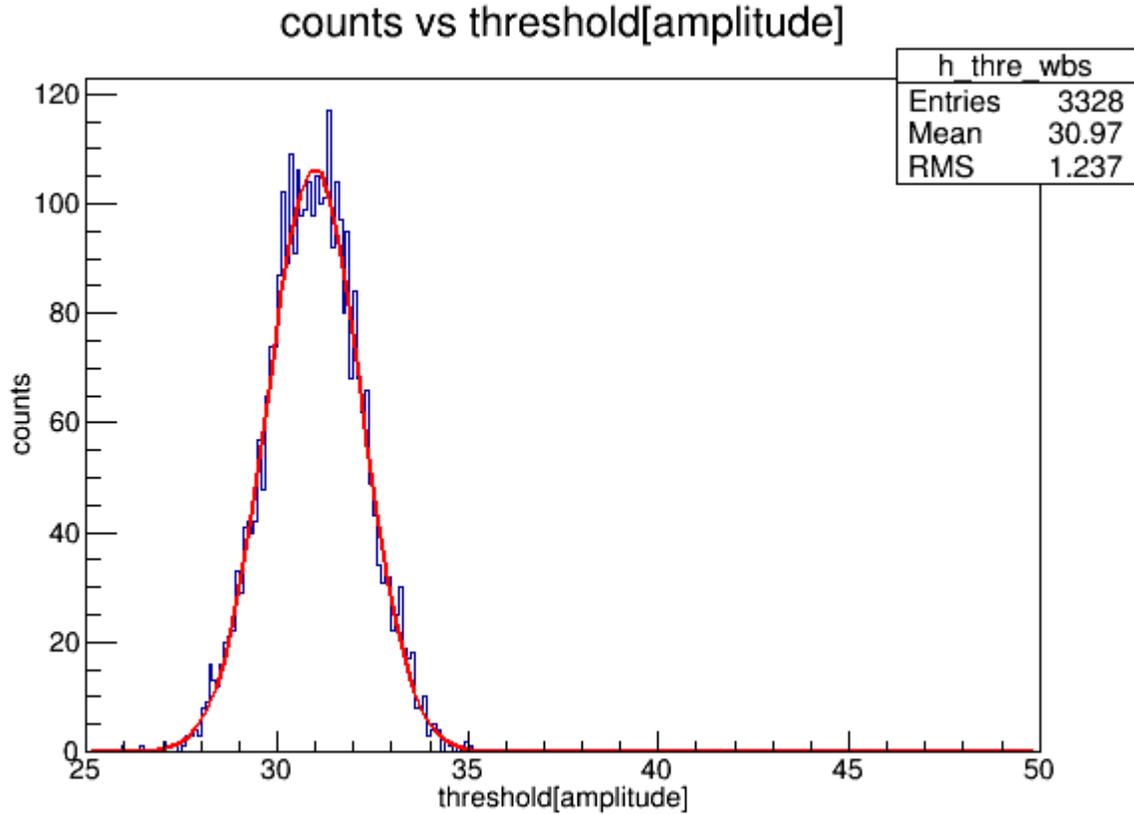
channel



Chip01 -----> 13
 Chip14 -----> 26



Threshold and sigma



Sigma[amplitude]