INTT weekly meeting

2021/08/10

Purdue University

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PURDUE
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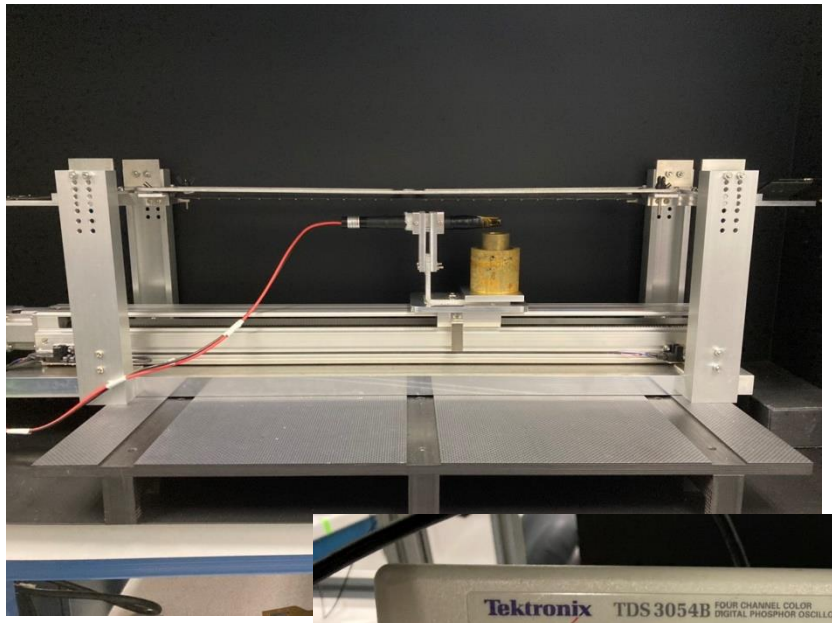
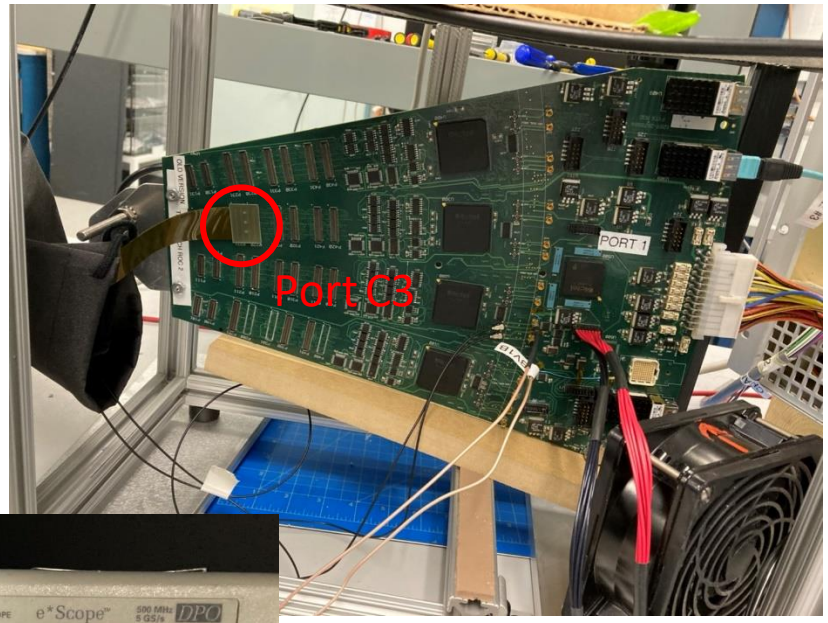
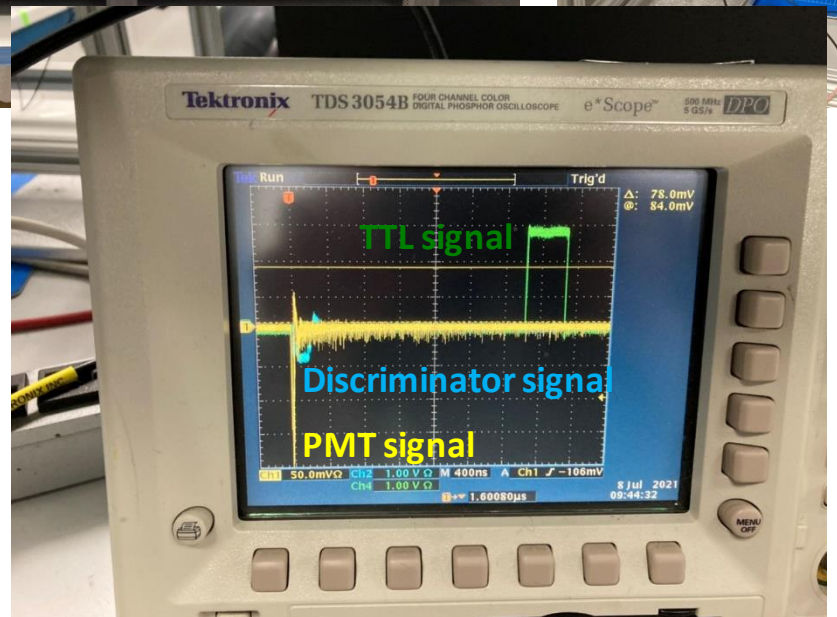
The setup of source test

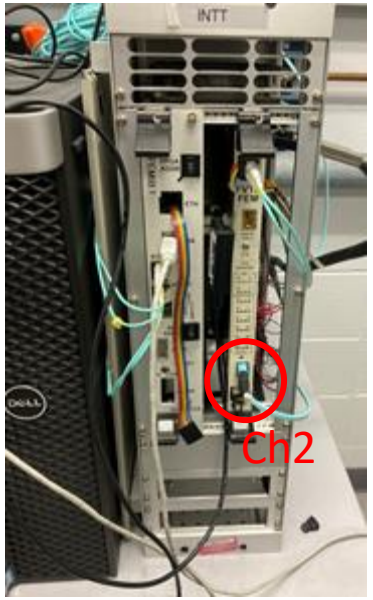
■ Source test fixture:

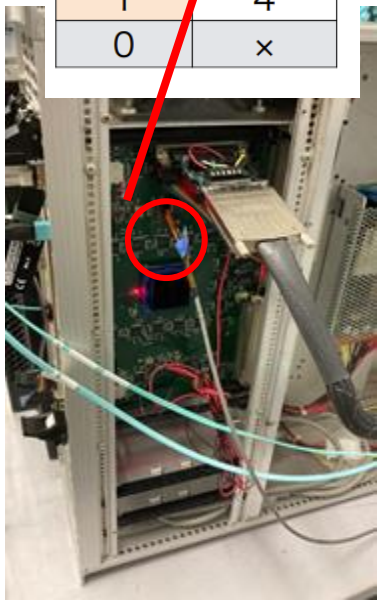




GND	GND
GND	GND
3	TRIG_IN
2	6
×	5
1	4
0	×

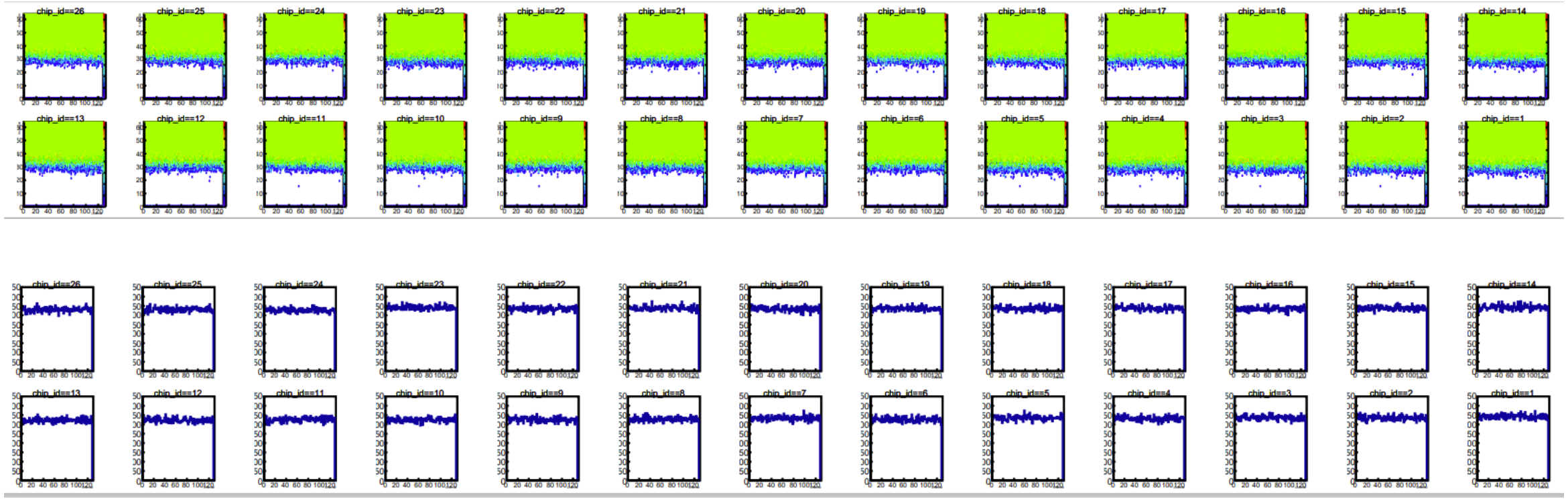






The setup of source test

■ Calibration test (before running the source test):

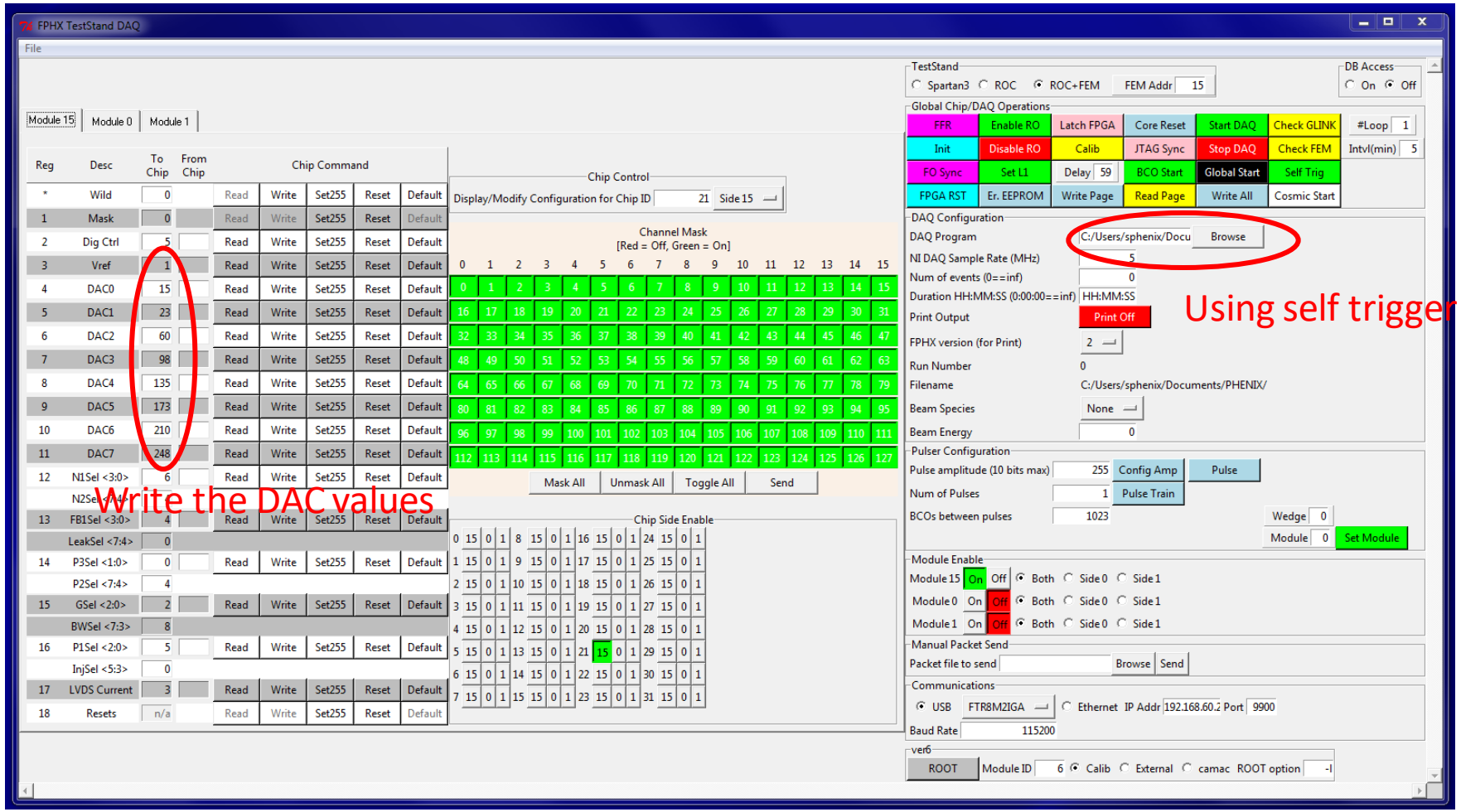


If getting a good result, we move on the source test

The setup of source test

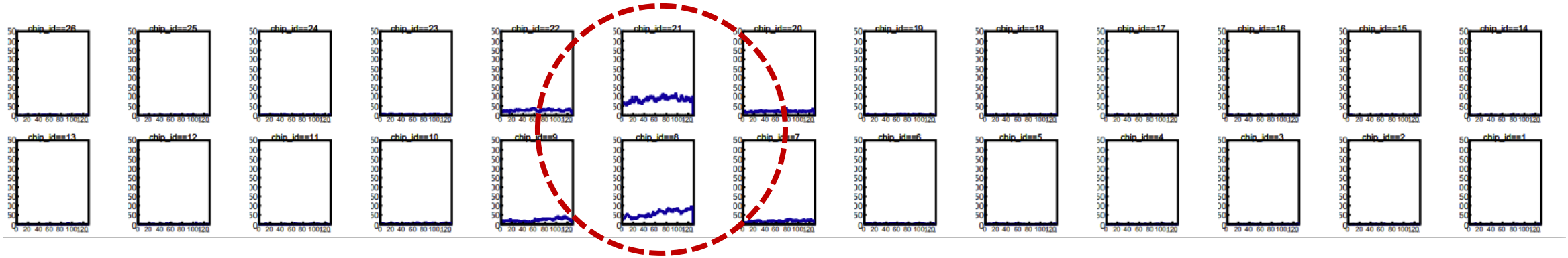
■ Steps for running source test:

1. FO Sync
2. FPGA RST
3. FFR
4. Init
5. Enable RO
6. Latch FPGA
7. Set L1 Delay (59)
8. BCO Start
9. Start DAQ
10. Self Trig
11. Unmask All
12. Send

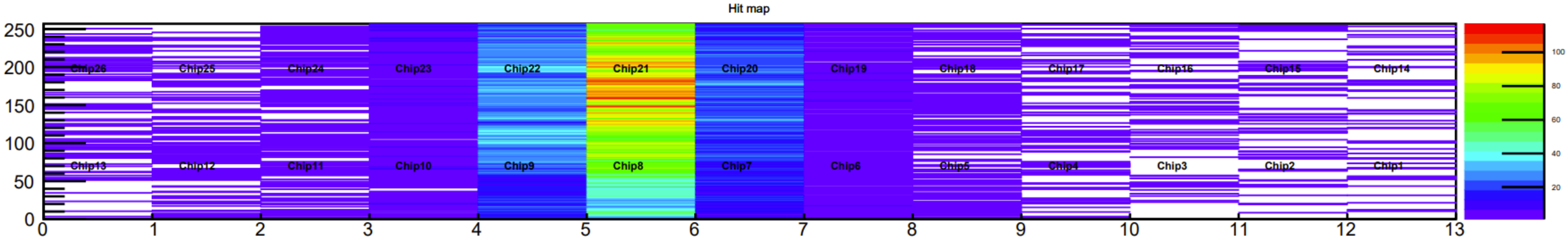


The setup of source test

■ Turn off the power of the control box:

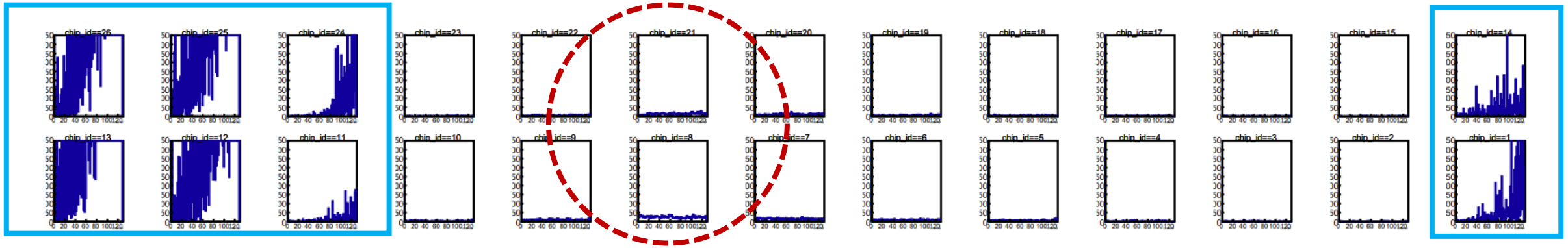


Radiation source fixed beneath the central point of chips 21 and 8



The setup of source test

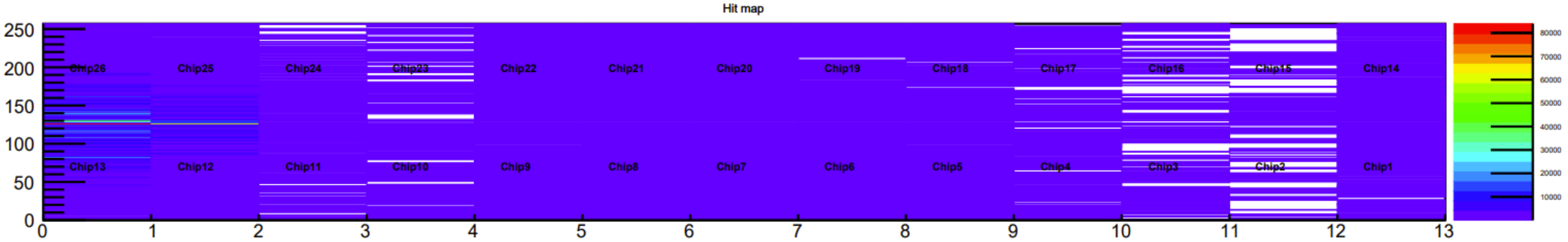
- Turn on the power of the control box:



Noise

Radiation source

Noise



Next step

- Fine-tune the clearance between the scintillator and sensors
- Try to find the solution dealing with the noise from the control box