

INTT weekly meeting

2021/08/10

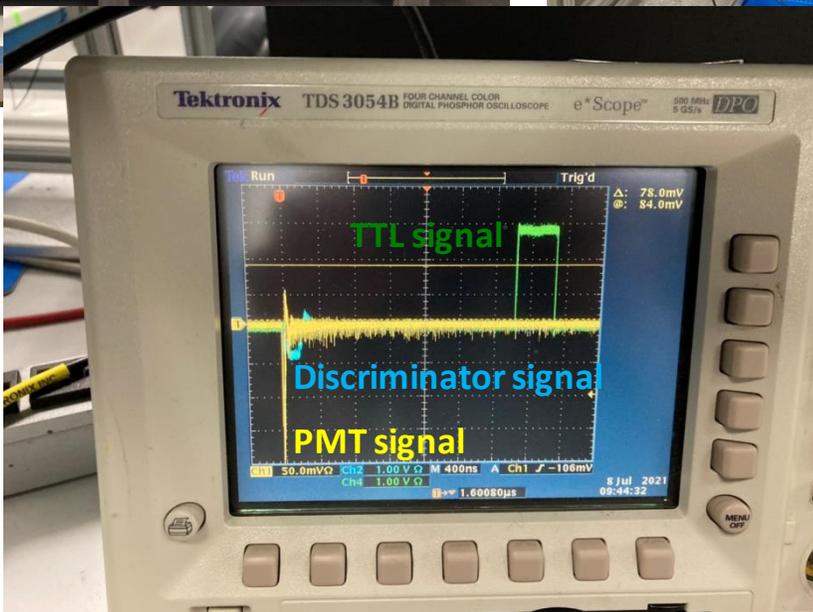
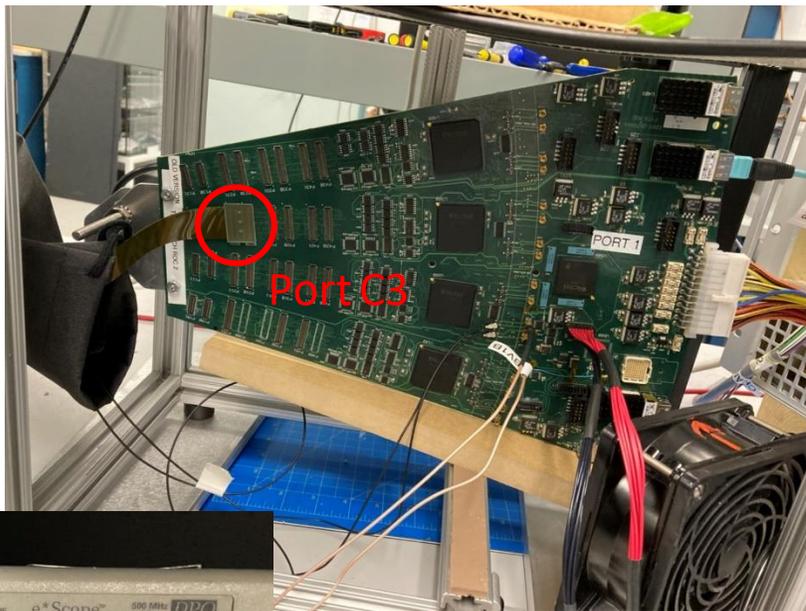
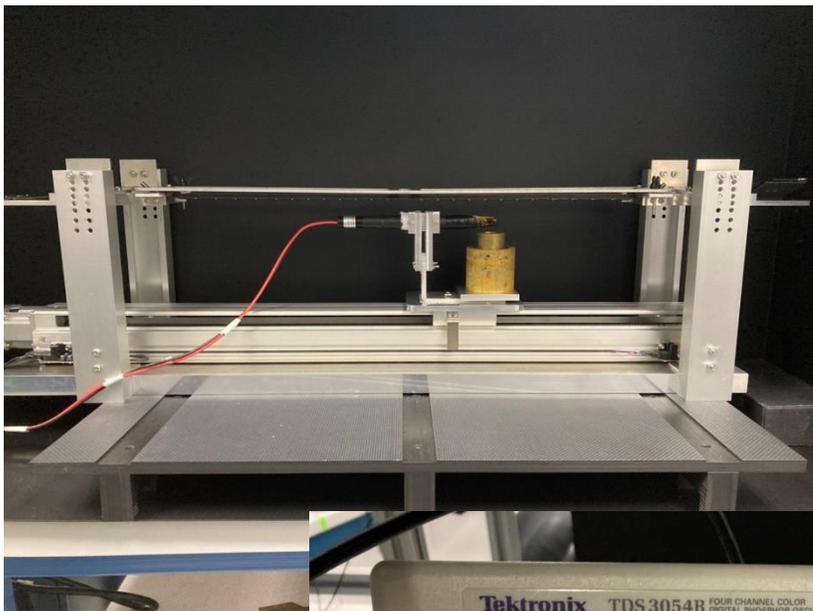
Purdue University

Han-Sheng Li

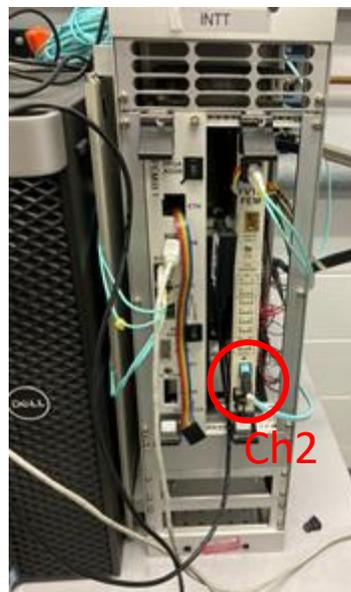
PURDUE
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The setup of source test

■ Source test fixture:

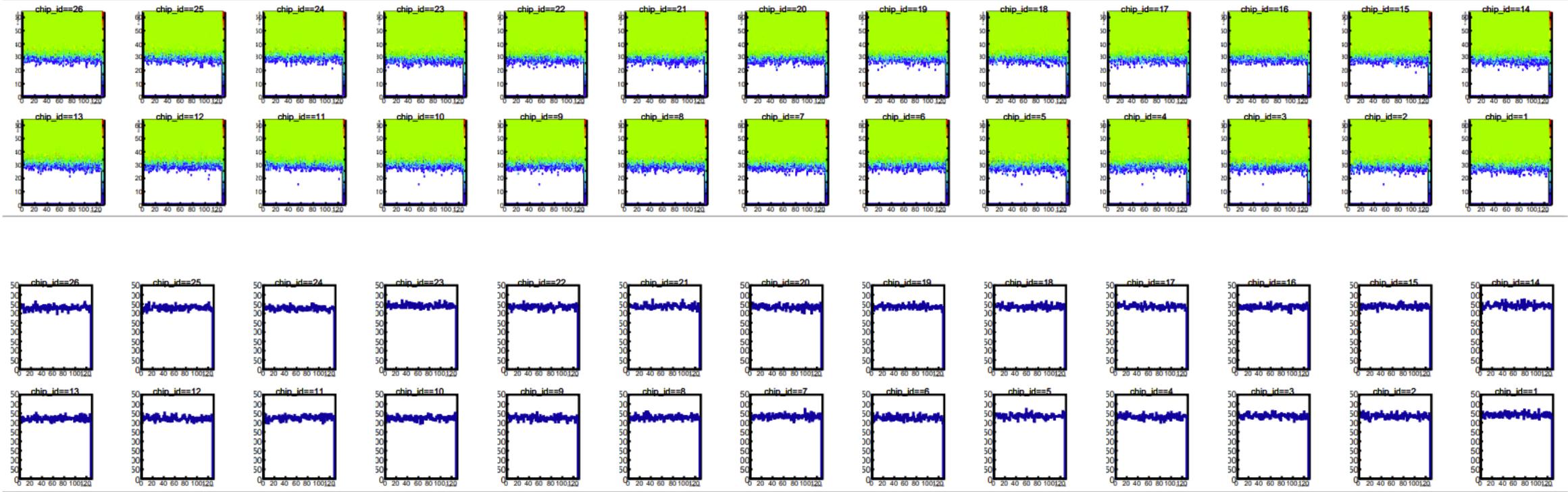


GND	GND
GND	GND
3	TRIG_IN
2	6
x	5
1	4
0	x



The setup of source test

■ Calibration test (before running the source test):



If getting a good result, we move on the source test

The setup of source test

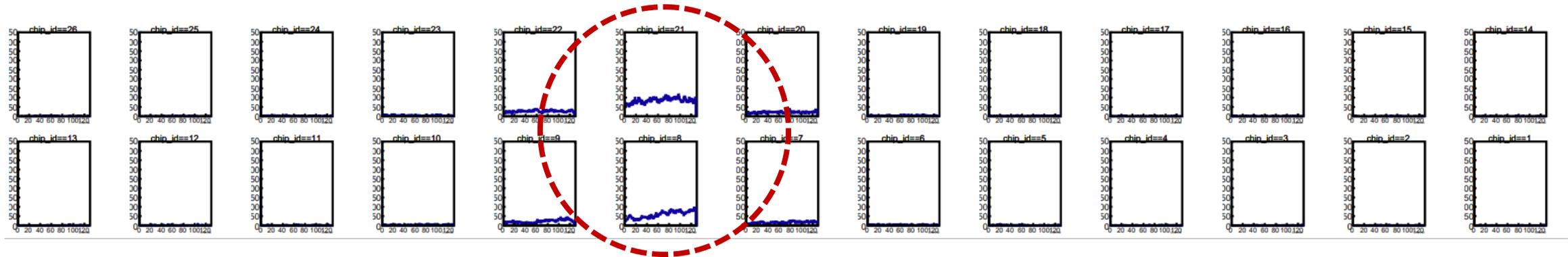
Steps for running source test:

1. FO Sync
2. FPGA RST
3. FFR
4. Init
5. Enable RO
6. Latch FPGA
7. Set L1 Delay (59)
8. BCO Start
9. Start DAQ
10. Self Trig
11. Unmask All
12. Send

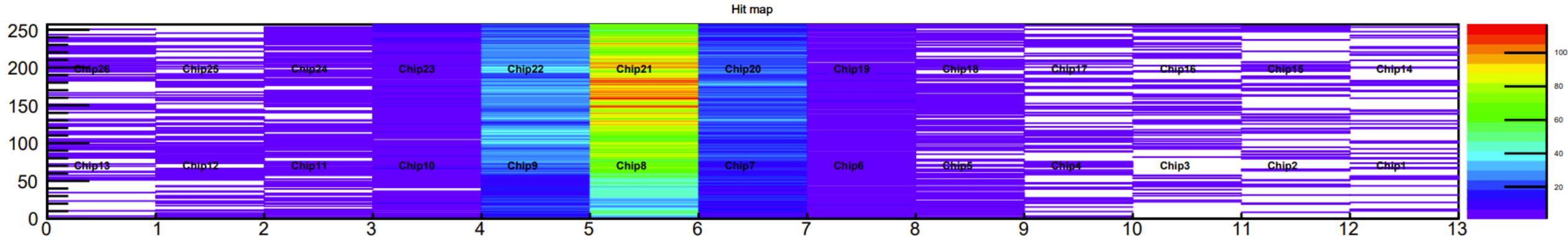
Reg	Desc	To Chip	From Chip	Chip Command
*	Wild	0		Read Write Set255 Reset Default
1	Mask	0		Read Write Set255 Reset Default
2	Dig Ctrl	5		Read Write Set255 Reset Default
3	Vref	1		Read Write Set255 Reset Default
4	DAC0	15		Read Write Set255 Reset Default
5	DAC1	23		Read Write Set255 Reset Default
6	DAC2	60		Read Write Set255 Reset Default
7	DAC3	98		Read Write Set255 Reset Default
8	DAC4	135		Read Write Set255 Reset Default
9	DAC5	173		Read Write Set255 Reset Default
10	DAC6	210		Read Write Set255 Reset Default
11	DAC7	248		Read Write Set255 Reset Default
12	NI Sel <3:0>	6		Read Write Set255 Reset Default
13	FBI Sel <3:0>	4		Read Write Set255 Reset Default
14	P3 Sel <1:0>	0		Read Write Set255 Reset Default
15	G Sel <2:0>	2		Read Write Set255 Reset Default
16	P1 Sel <2:0>	5		Read Write Set255 Reset Default
17	LVDS Current	3		Read Write Set255 Reset Default
18	Resets	n/a		Read Write Set255 Reset Default

The setup of source test

■ Turn off the power of the control box:

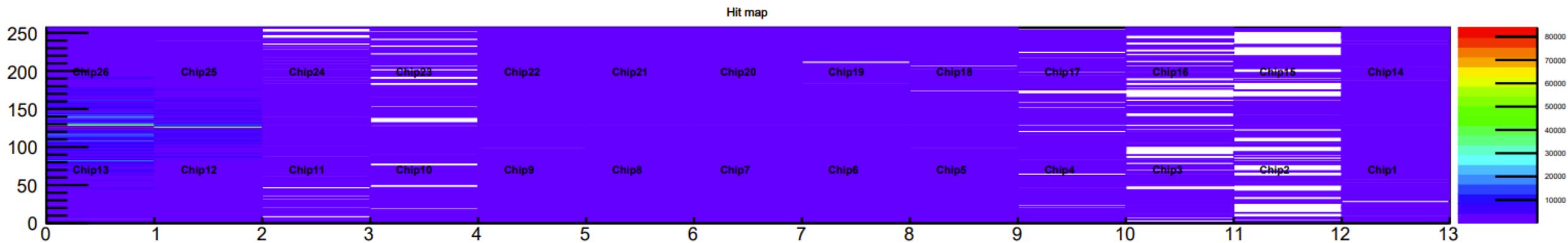
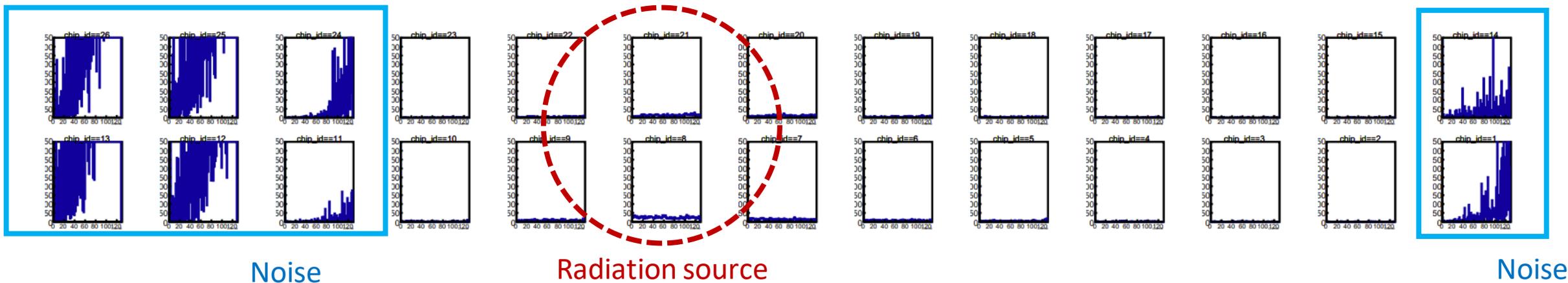


Radiation source fixed beneath the central point of chips 21 and 8



The setup of source test

■ Turn on the power of the control box:



Next step

- Fine-tune the clearance between the scintillator and sensors
- Try to find the solution dealing with the noise from the control box