INTT meeting Aug/17/2021

Stability of the calibration tests

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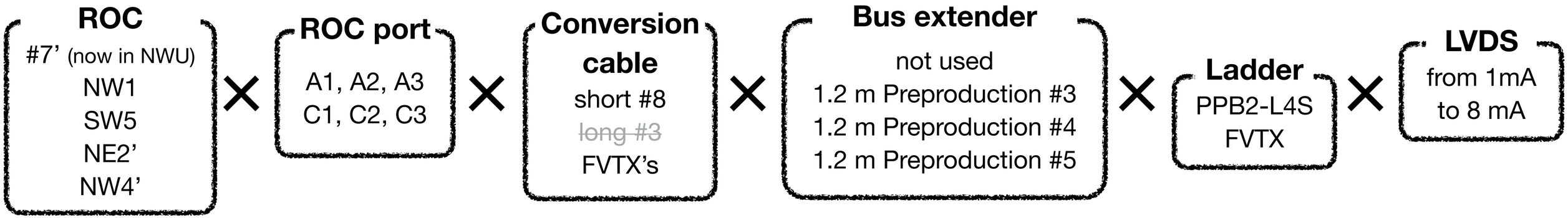
H. Imai, Y. Nakamura, G. Nakano

Calibration tests

We continued calibration tests with various conditions to understand our testbenches more:



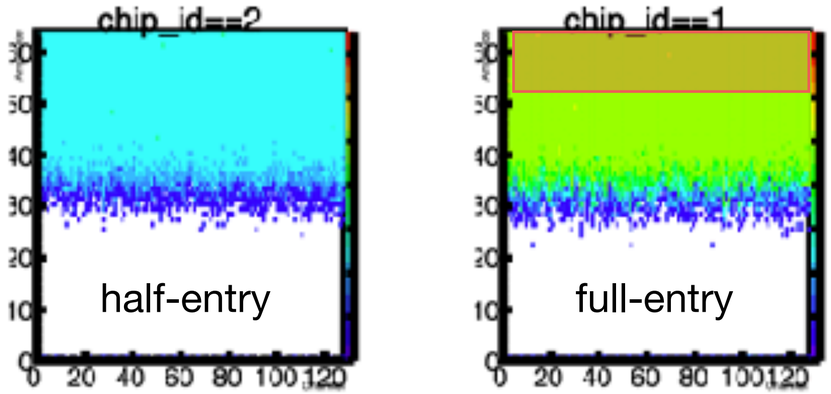
Upgraded ROCs are indicated by ‘

Today’s report:

- quick review of the calibration tests in the RIKEN testbench
- calibration tests with the FVTX silicon module
- calibration tests with cooling for the ladder

mainly for the less entry issue (better than half entry but not good enough)

Calibration tests at the RIKEN testbench



riken_fphx_raw_20210719-1618_0.dat

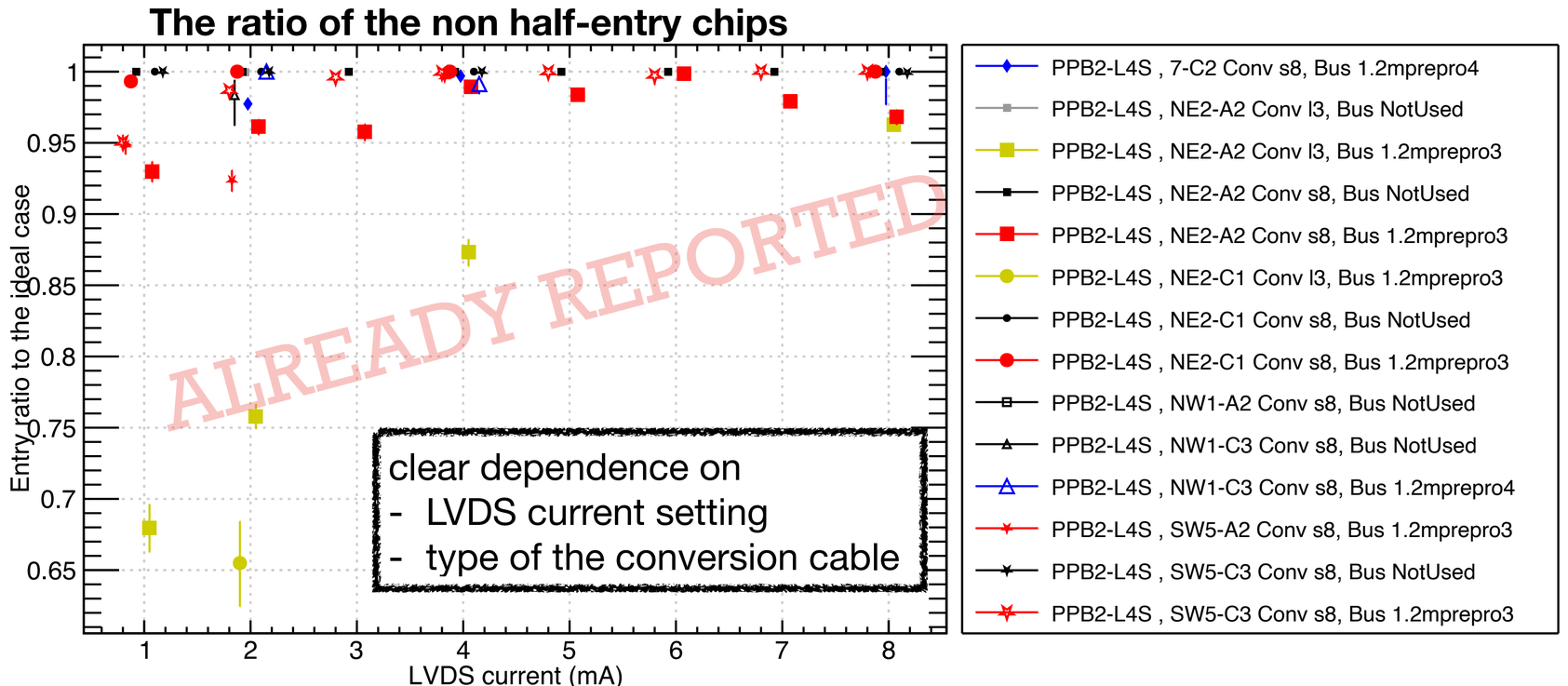
Sometimes, especially setup with a bus extender, we found chips having only half entry than expected.

I defined the half-entry chip as:

$12700 \times 40\% < \text{entry} < 12700 \times 60\%$

in the region

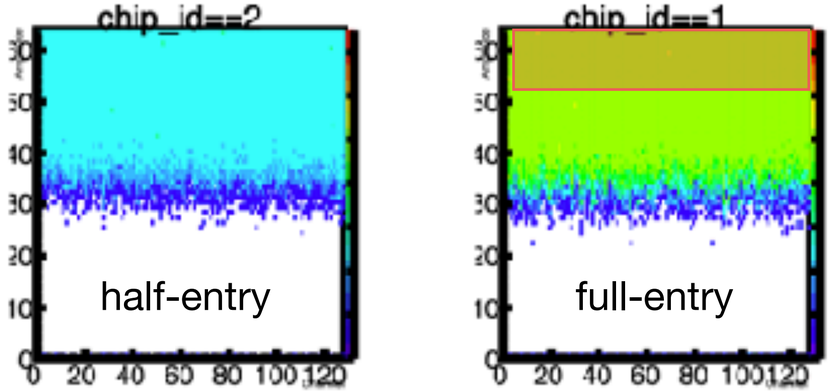
$0 < \text{ch} < 128$ AND $53 < \text{ampl} < 65$ (not a message for the ladder classification)



The ratio of the half-entry issue depends on
- existence of the bus extender
- LVDS current setting
- a type of the conversion cable.

The issue is more or less under control.
The co-axial conversion cable currently under development may improve the situation.

Calibration tests at the RIKEN testbench, less-entry issue



riken_fphx_raw_20210719-1618_0.dat

Sometimes, especially setup with a bus extender, we found chips having only half entry than expected.

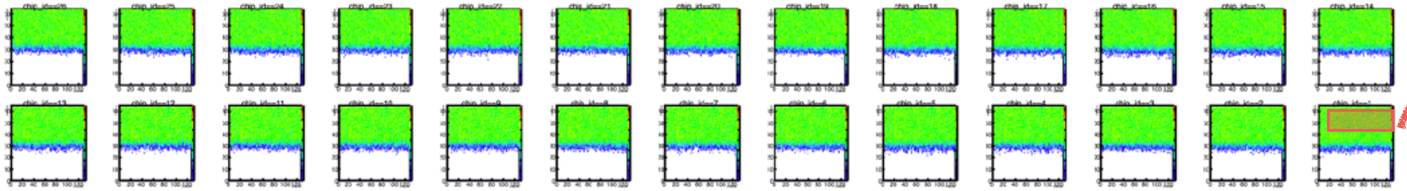
I defined the half-entry chip as:

12700 × 40% < entry < 12700 × 60%

in the region

0 < ch < 128 AND 53 < ampl < 65 (not a message for the ladder classification)

riken_fphx_raw_20210712-1716_0.dat



11243 entries while 12700 in the ideal case
→12% of data was not acquired.
Such data losses are also sometimes seen.

Definition of a chip with less entry :

12700 × 60% < entry < 12700 × 90%

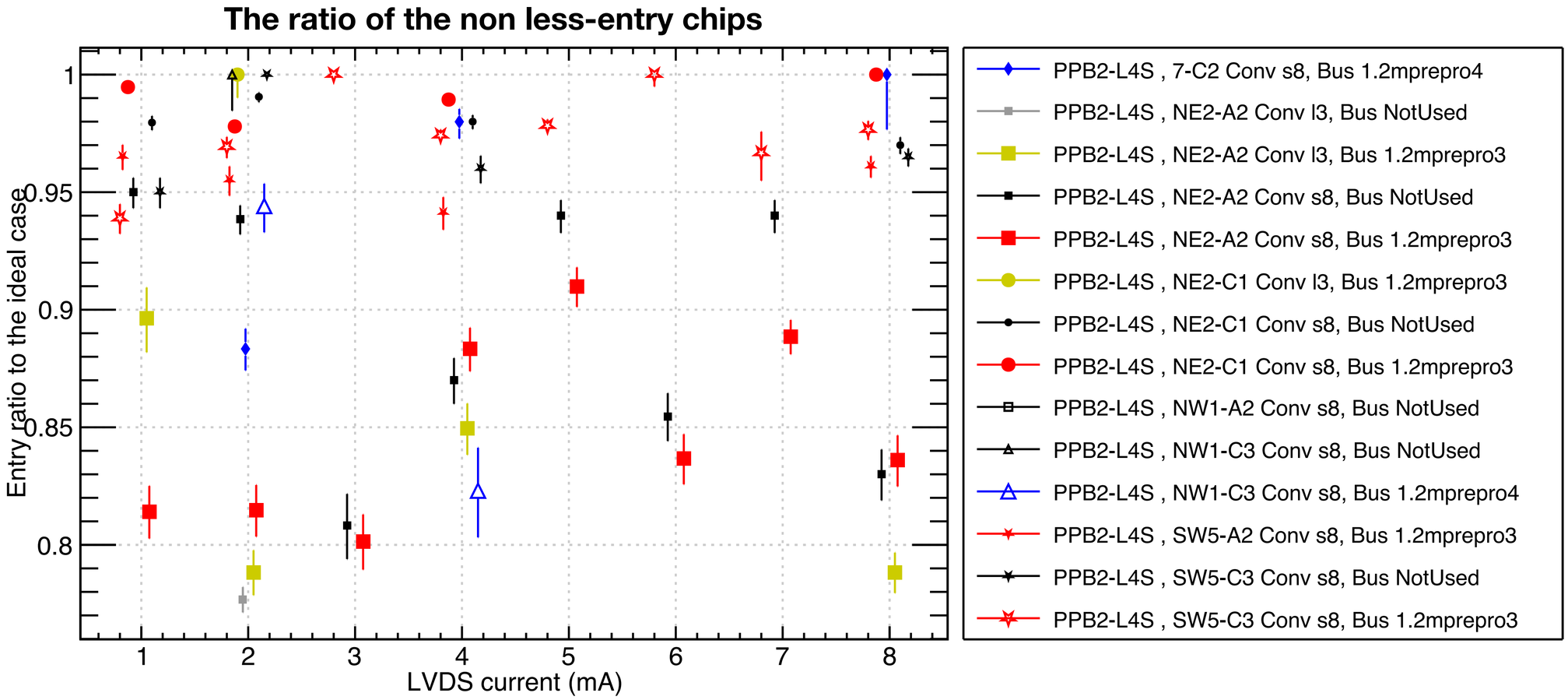
total entries for a chip:

12700 × 40% < entry < 12700 × 105% (additional 5% is for noise contamination)

Ratio of successful ratio:

less entry chips / total chips

Calibration tests at the RIKEN testbench, less-entry issue



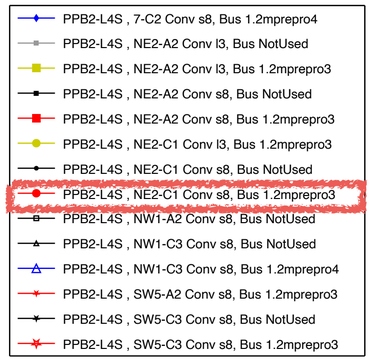
Very chaotic situation…

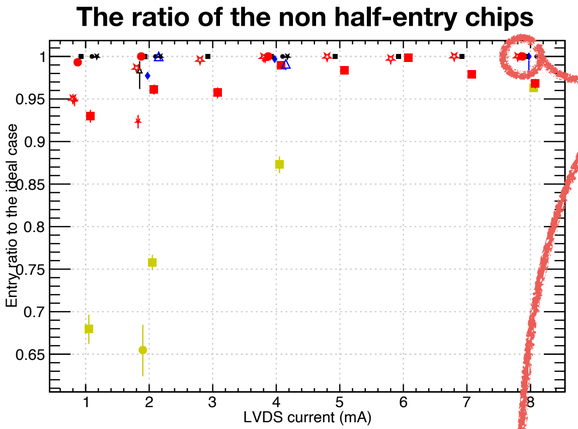
No correlation with the LVDS setting.

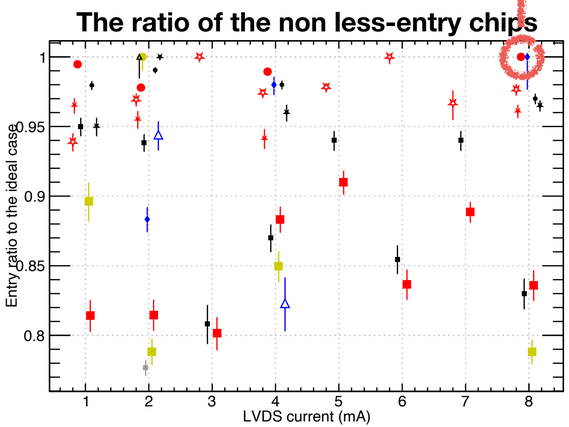
Even setup without a bus extender also shows down to 80%.

Calibration tests at the RIKEN testbench, less-entry issue

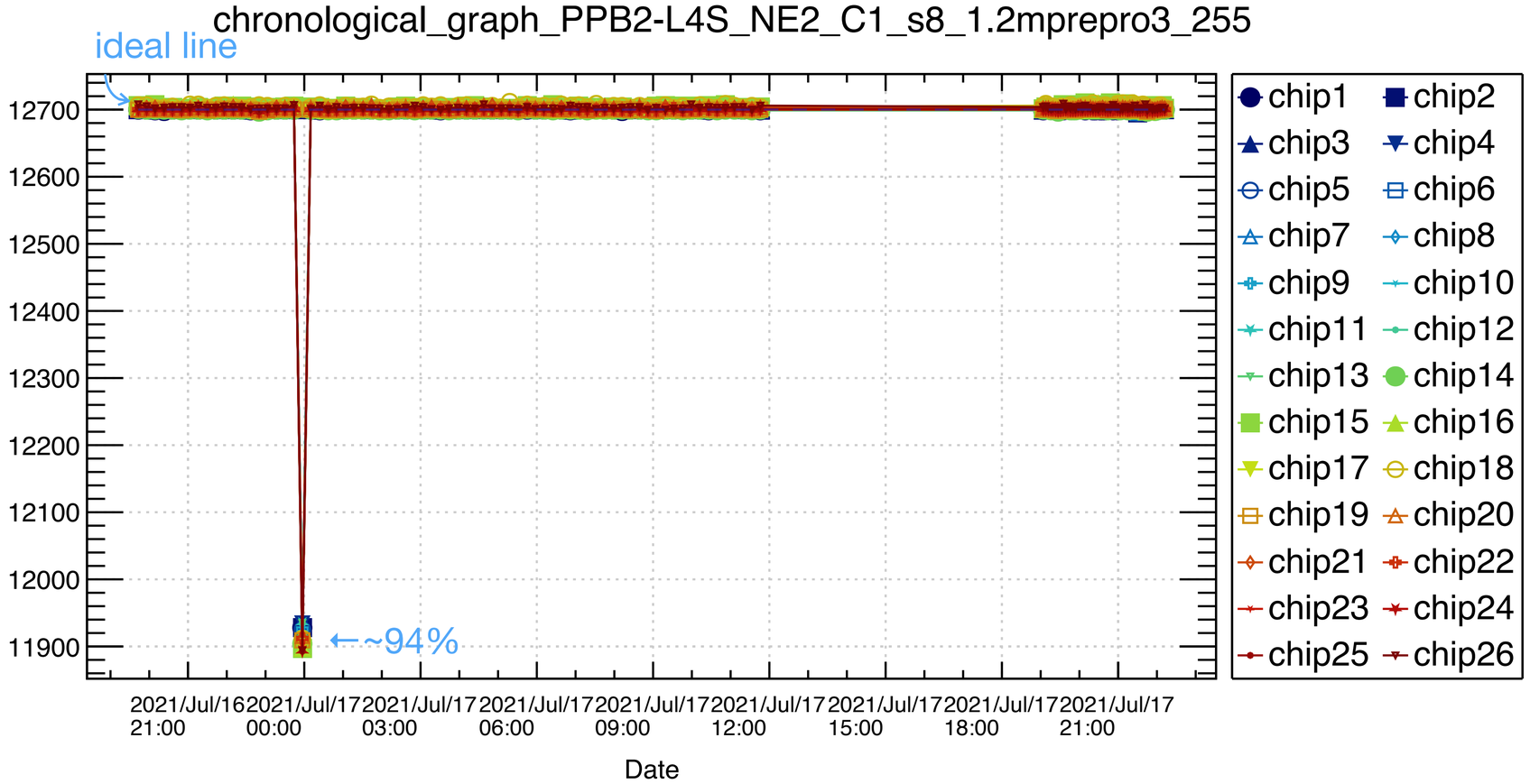
Ladder: PPB2-L4S
ROC: NE2(upgraded 1008 ROC)
ROC port: C1
Conversion cable: short8
Bus extender: 1.2 m Prepro#3
LVDS: 8 mA





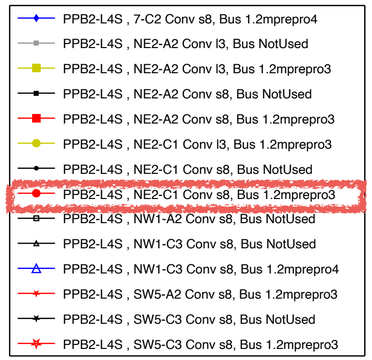


One of the best cases

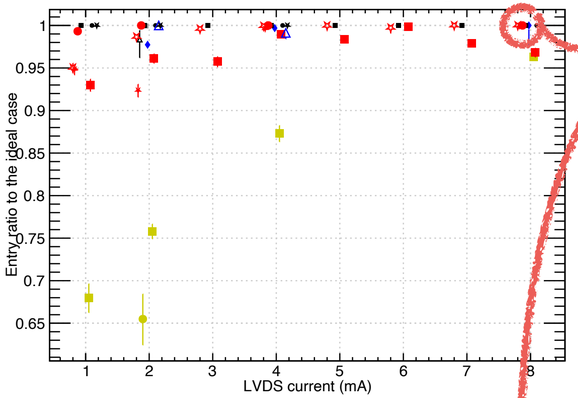


Calibration tests at the RIKEN testbench, less-entry issue

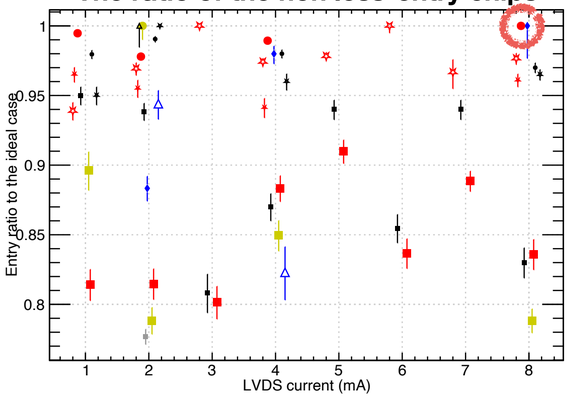
Ladder: PPB2-L4S
ROC: NE2(upgraded 1008 ROC)
ROC port: C1
Conversion cable: short8
Bus extender: 1.2 m Prepro#3
LVDS: 8 mA



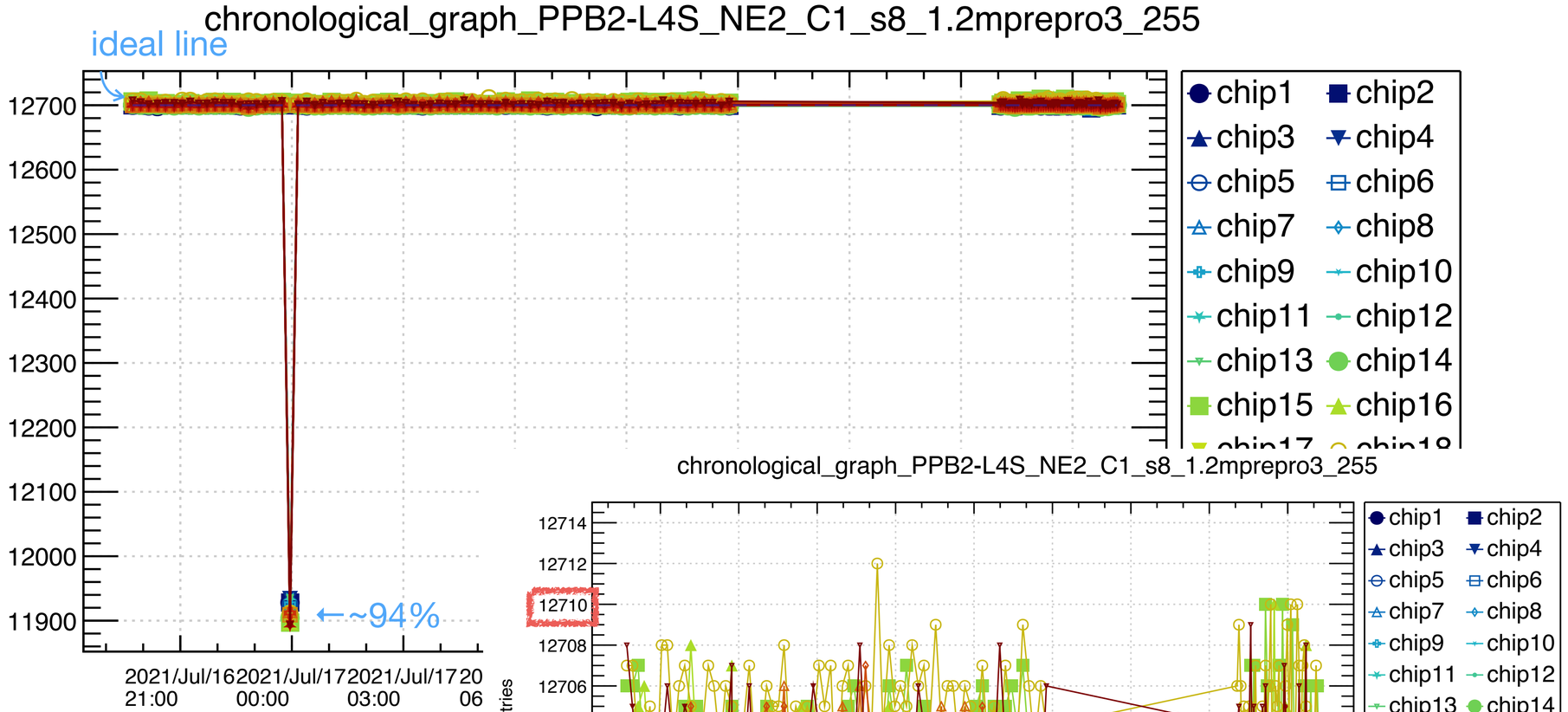
The ratio of the non half-entry chips

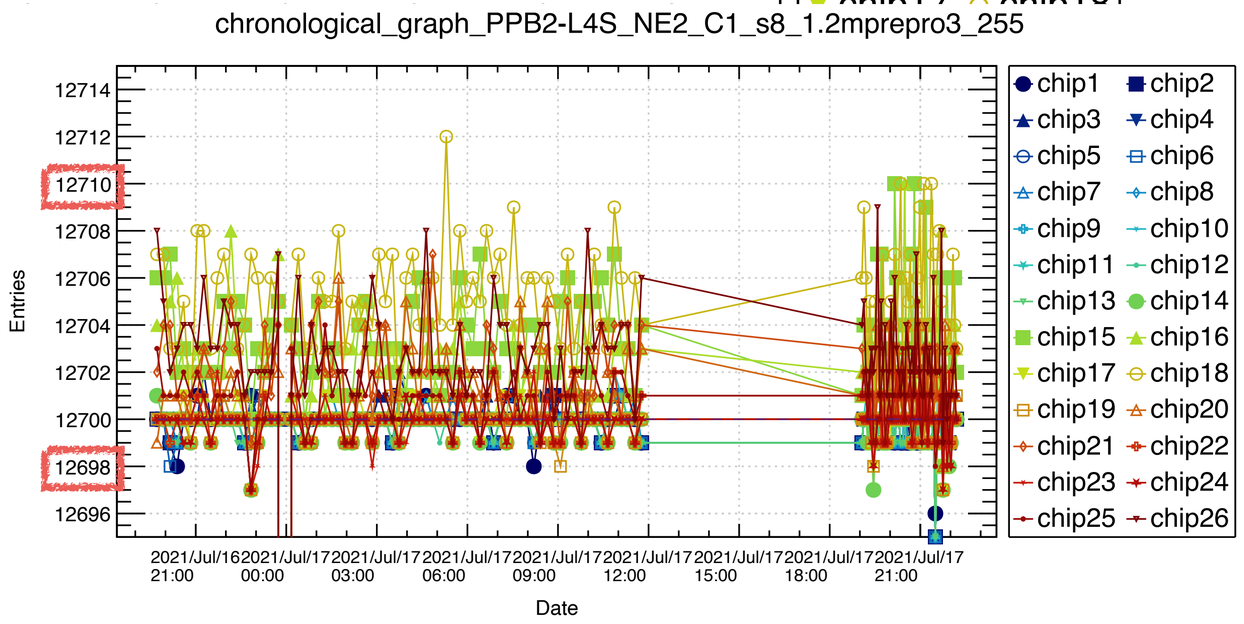


The ratio of the non less-entry chips



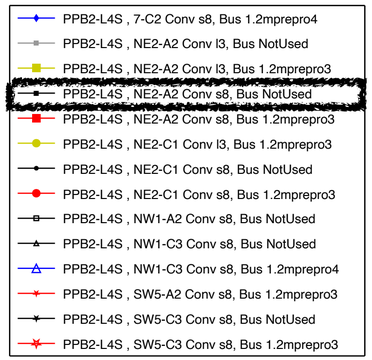
One of the best cases

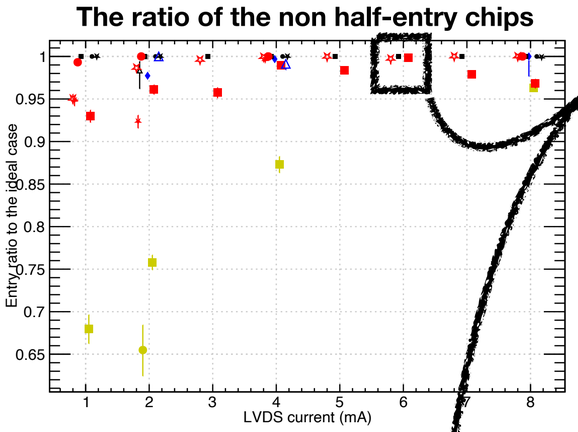


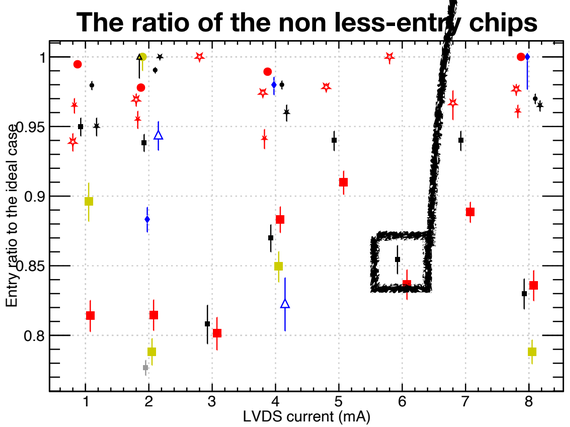


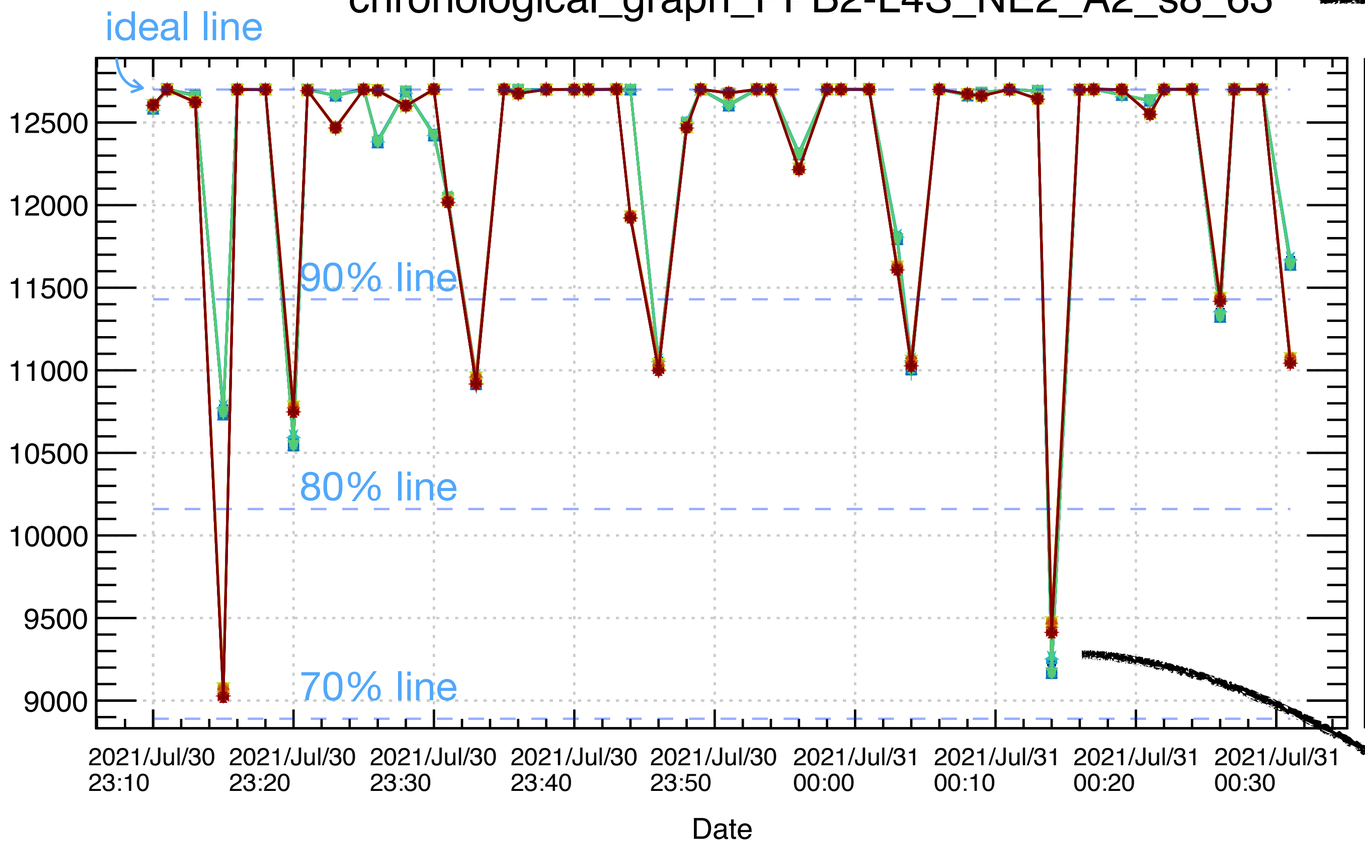
Calibration tests at the RIKEN testbench, less-entry issue

Ladder: PPB2-L4S
ROC: NE2(upgraded 1008 ROC)
ROC port: A2
Conversion cable: short8
Bus extender: Not used
LVDS: 6 mA

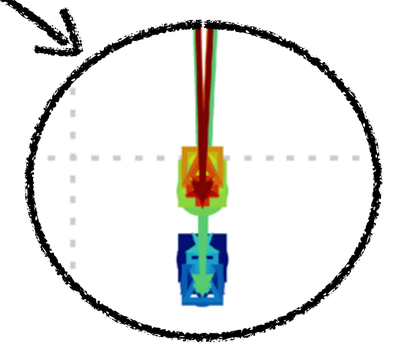






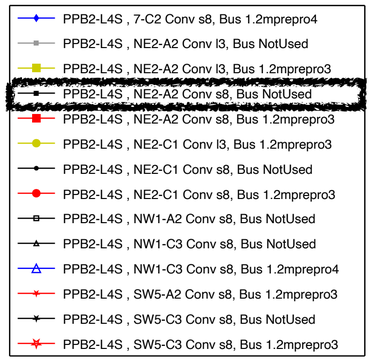


zoom

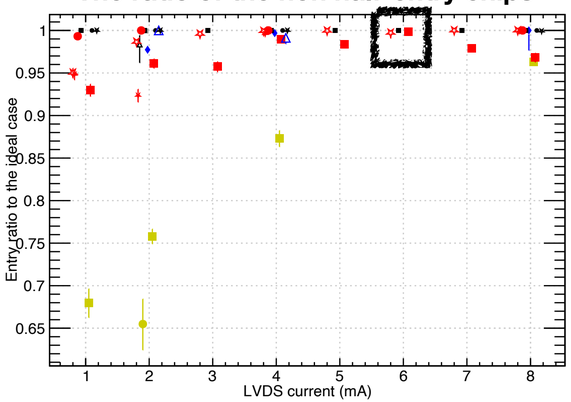


The less-entry chips appear randomly for time.
Chips on a side (#1-13 or #14-26) tend to behave similarly.

Calibration tests at the RIKEN testbench, correlations of chip events



The ratio of the non half-entry chips



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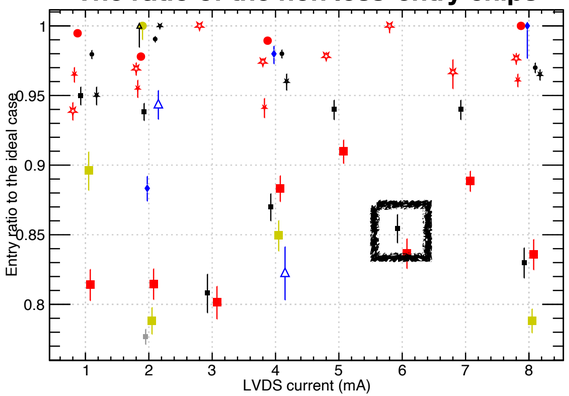
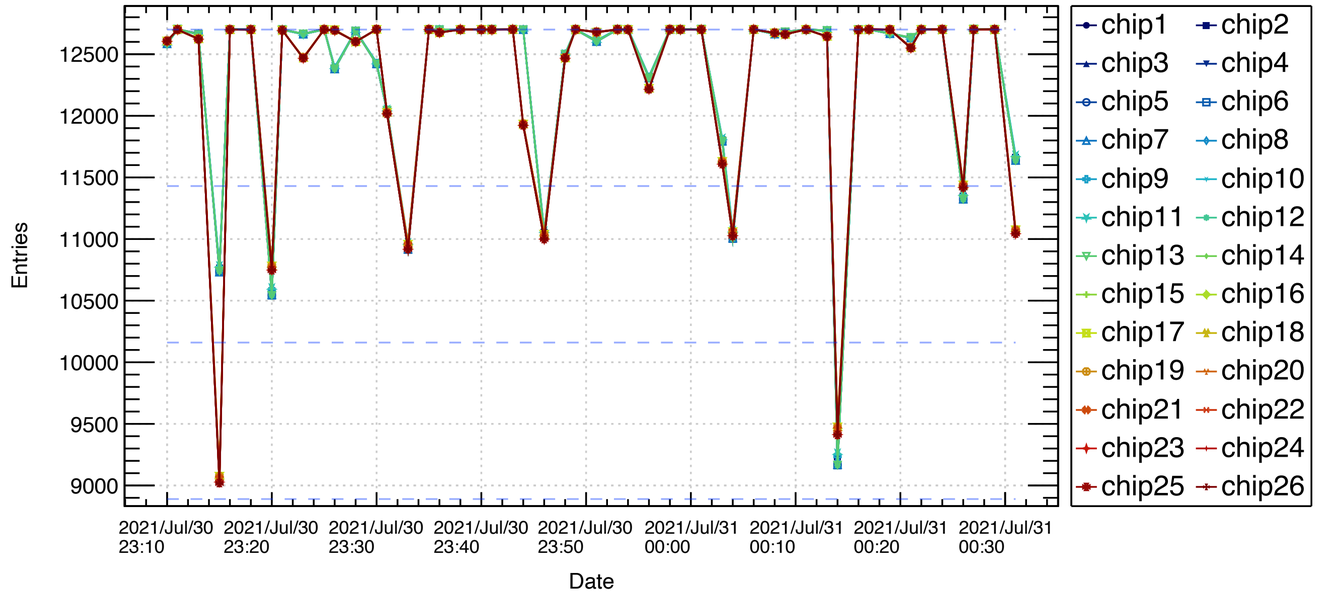
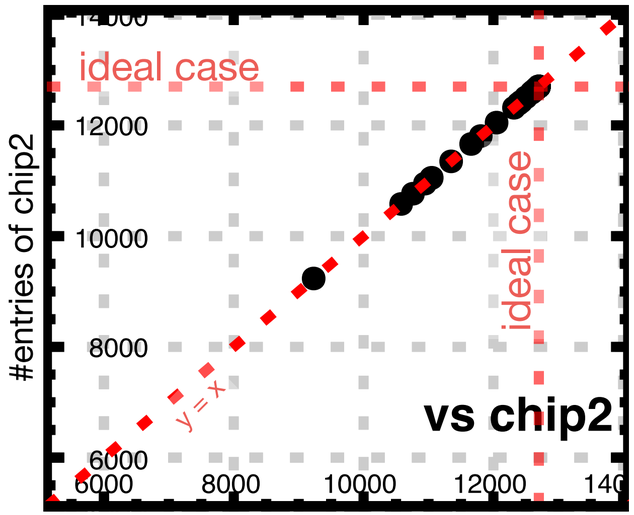


chronological_graph_PPB2-L4S_NE2_A2_s8_63

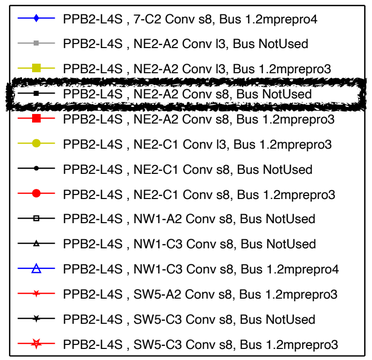


Correlation between #entries of the chip1 and the chip2



← #entries of the chip1 and chip2 are almost the same

Calibration tests at the RIKEN testbench, correlations of chip events



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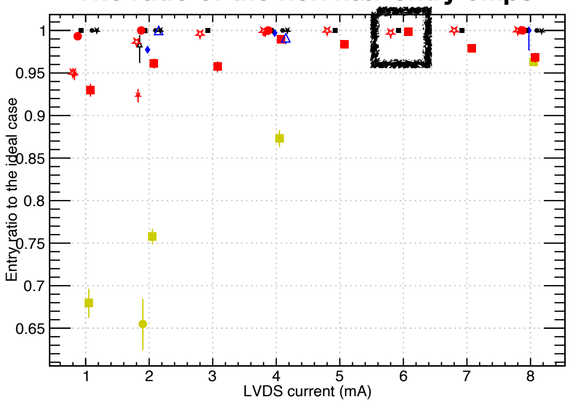
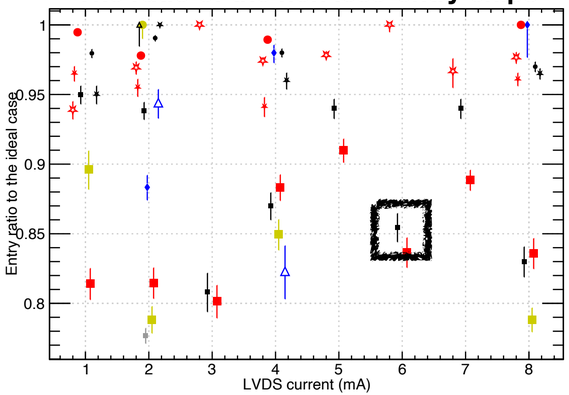
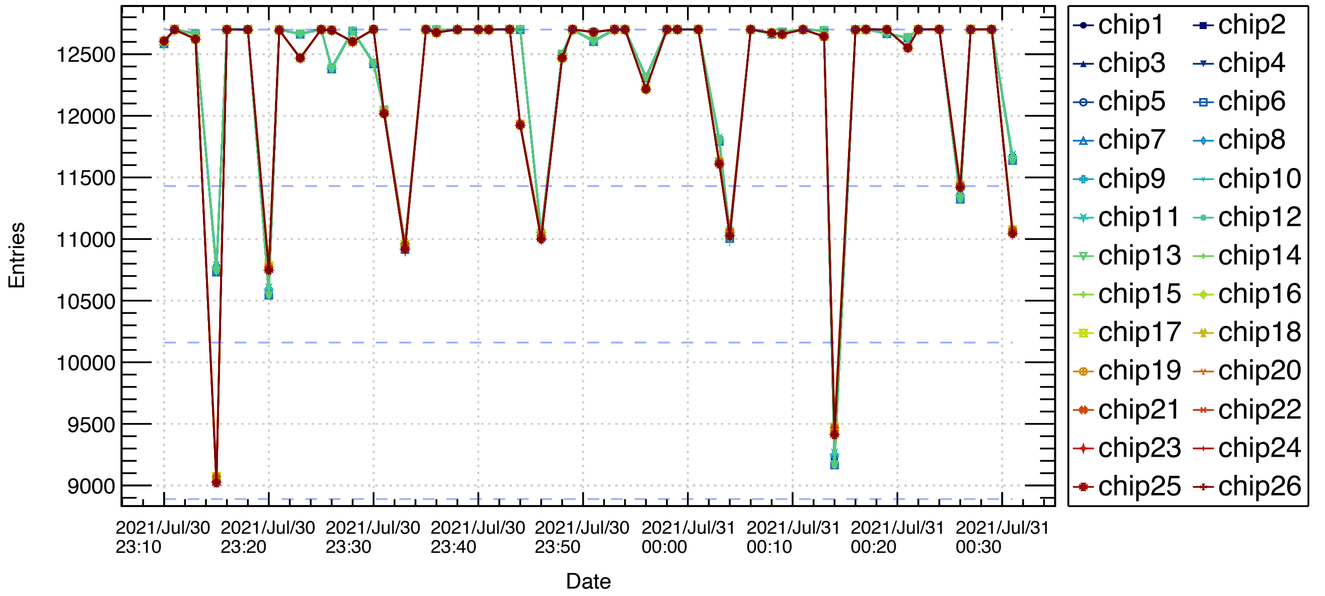


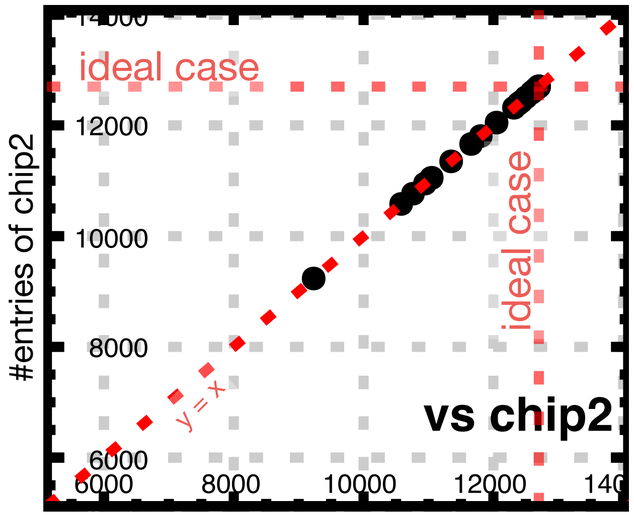
The ratio of the non less-entry chips



chronological_graph_PPB2-L4S_NE2_A2_s8_63

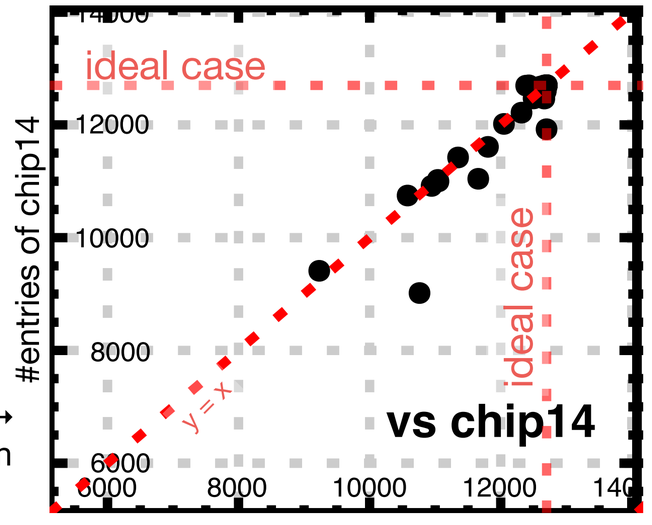


Correlation between #entries of the chip1 and the chip2

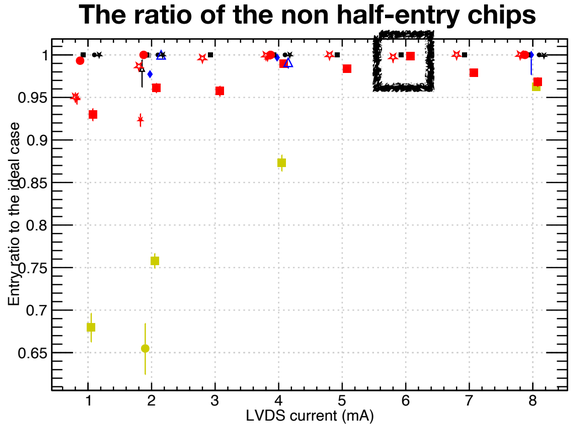


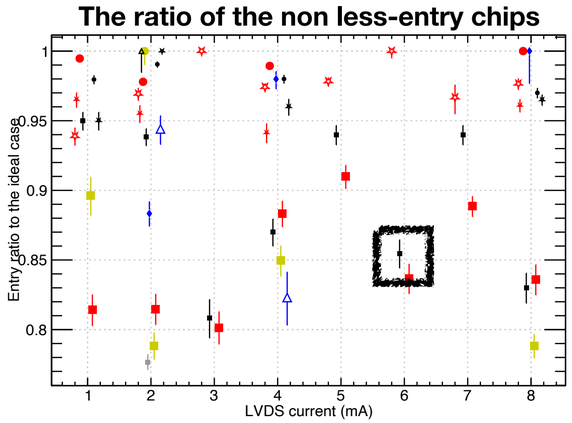
← #entries of the chip1 and chip2 are almost the same

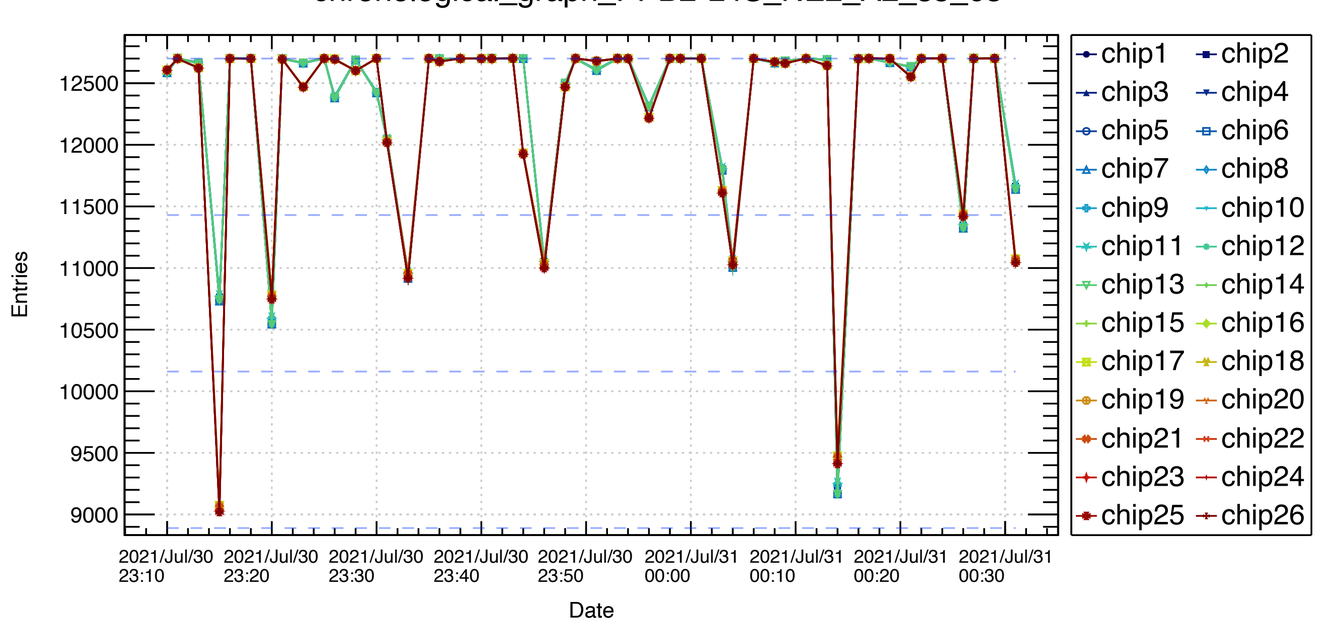
the similar correlation as chip1 vs chip2 can be seen with larger fluctuation →



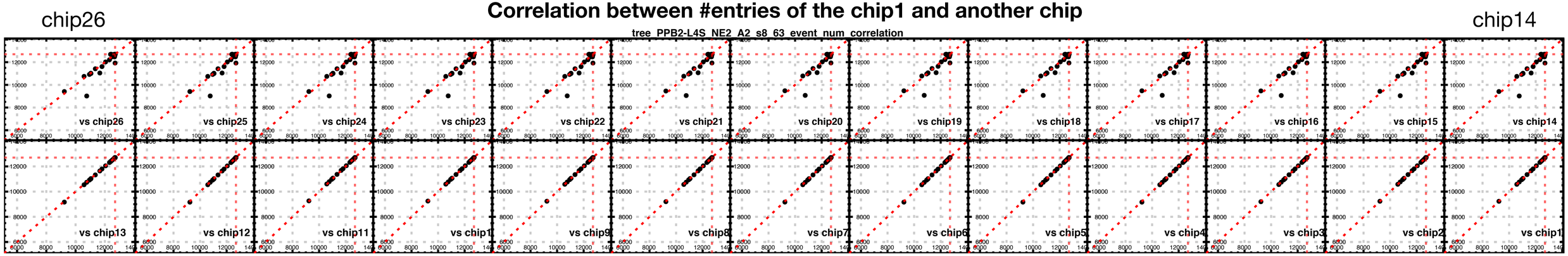
Calibration tests at the RIKEN testbench, correlations of chip events







chip26



chip14

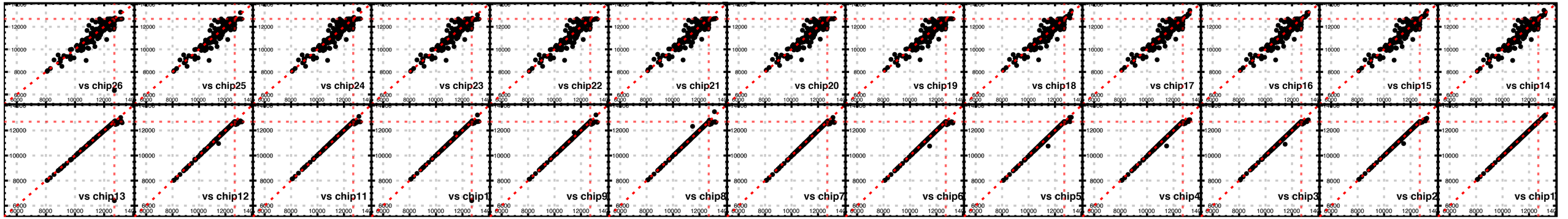
chip13

Chip2-13 have almost the same events as chip1's.
Correlations of chip14-26 distribute around y = x.

Calibration tests at the RIKEN testbench, correlations of chip events

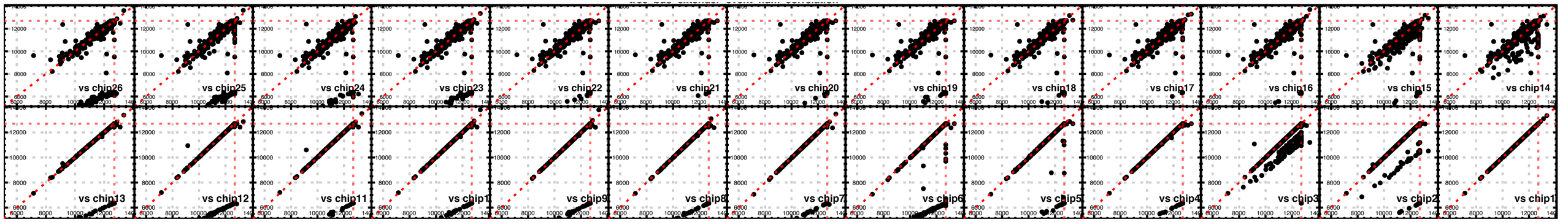
vs Chip1

Correlation of #entries of the chip1 and another chip without a bus extender.



Chip2-13 have almost the same events as chip1's.
Correlations of chip14-26 distribute around y = x.

Correlation of #entries of the chip1 and another chip with a bus extender.

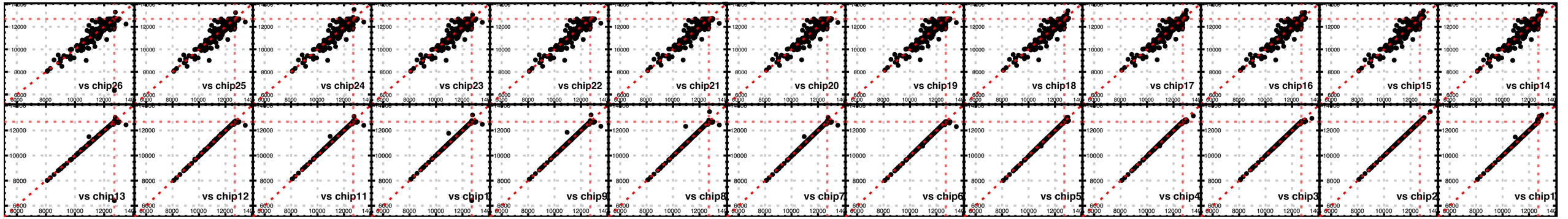


Islands due to half entry clearly seen.
Some slopes in the plots for chip2~13 seen.

Calibration tests at the RIKEN testbench, correlations of chip events

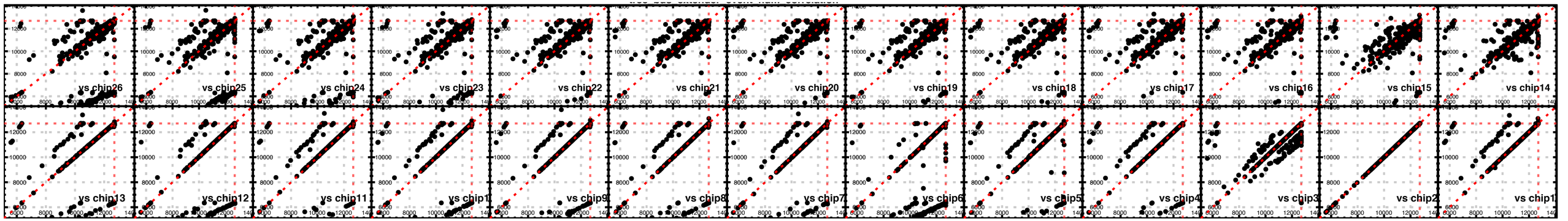
vs Chip2

Correlation of #entries of the chip2 and another chip without a bus extender.



Almost the same as “vs chip1”.

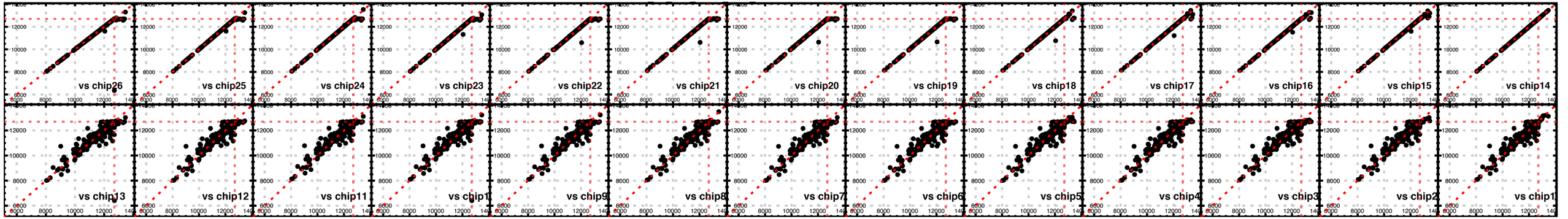
Correlation of #entries of the chip2 and another chip with a bus extender.



Calibration tests at the RIKEN testbench, correlations of chip events

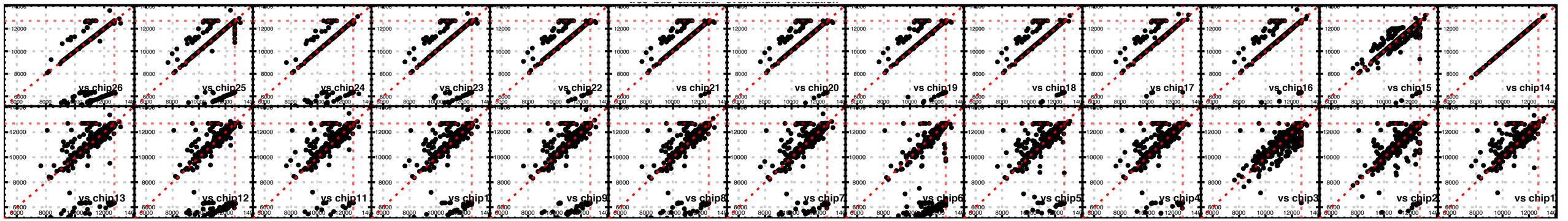
vs Chip14

Correlation of #entries of the chip14 and another chip without a bus extender.



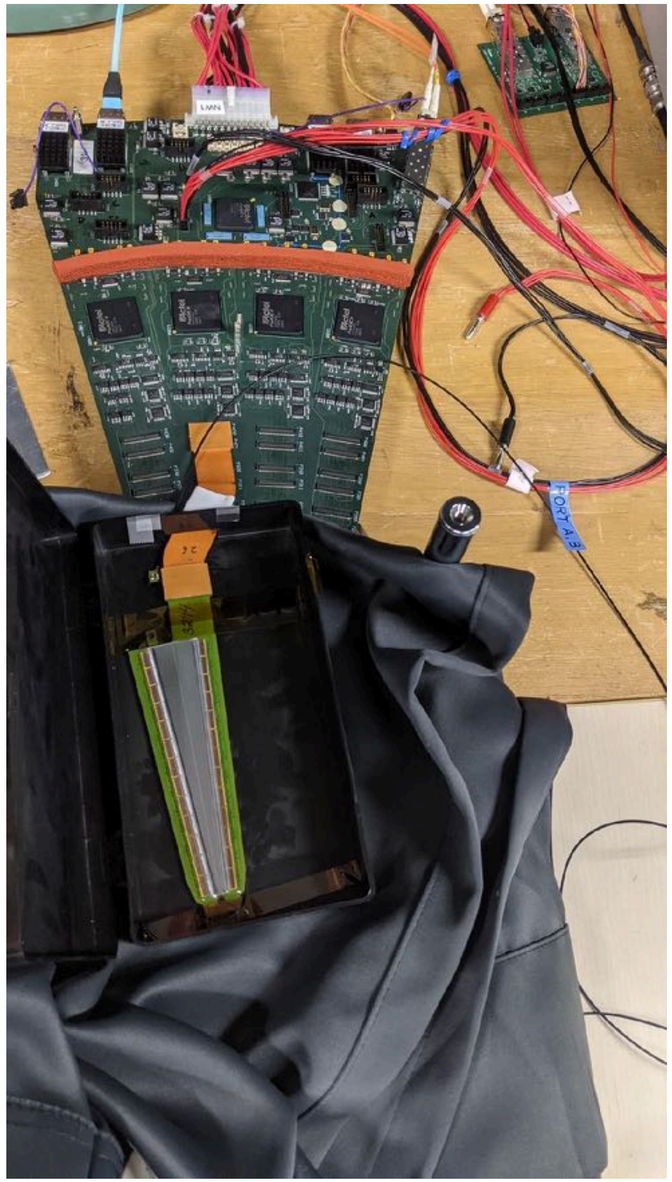
Chip15-26 have almost the same events as chip14's.
Correlations of chip1-13 distribute around y = x.

Correlation of #entries of the chip14 and another chip with a bus extender.



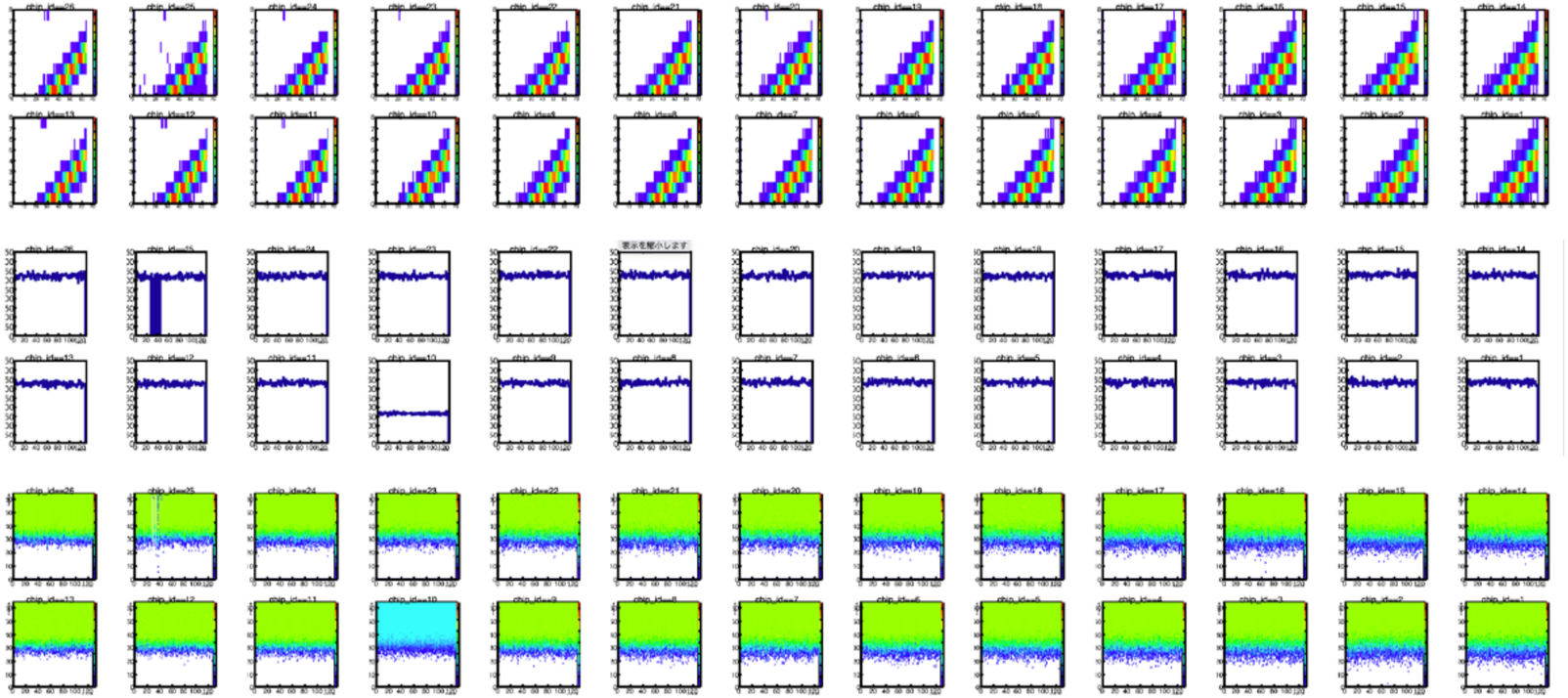
Chips on a side tend to have almost the same entries.

Calibration tests at the RIKEN testbench, What about FVTX?



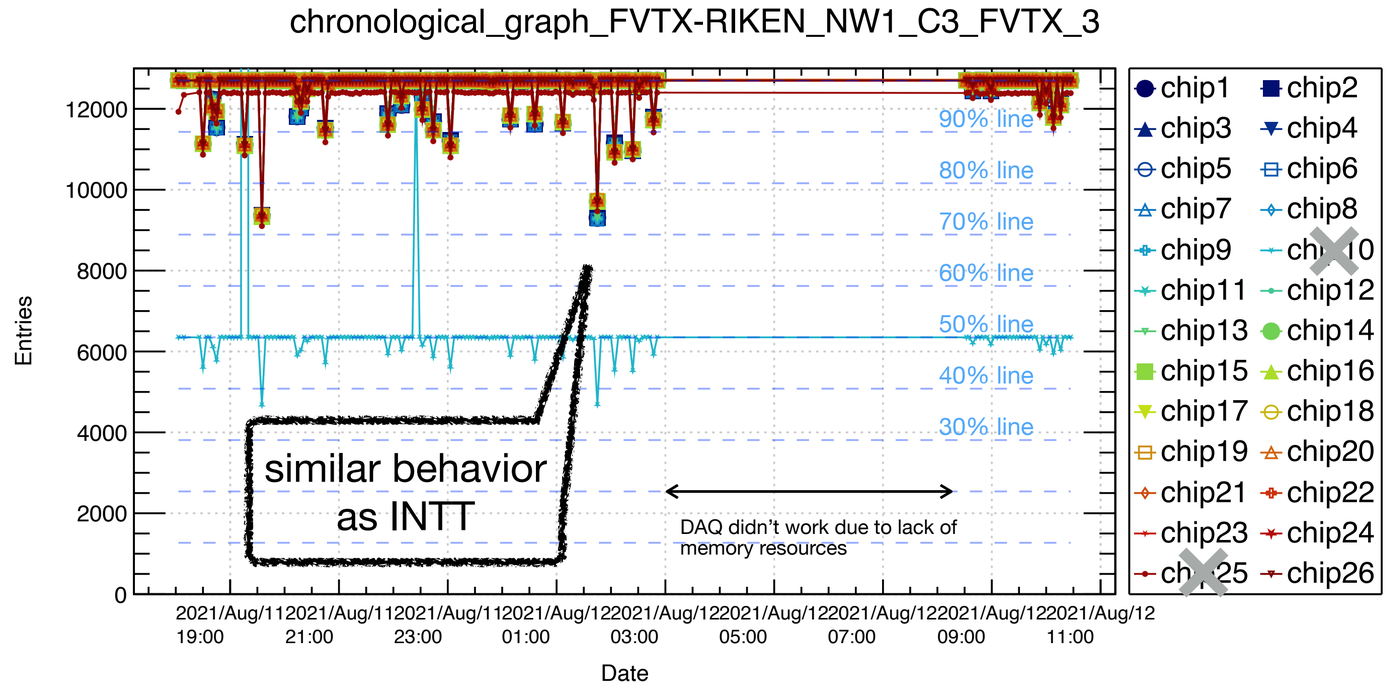
Ladder: FVTX
ROC: NW1 (1008 ROC)
ROC port: C3
Conversion cable: FVTX's

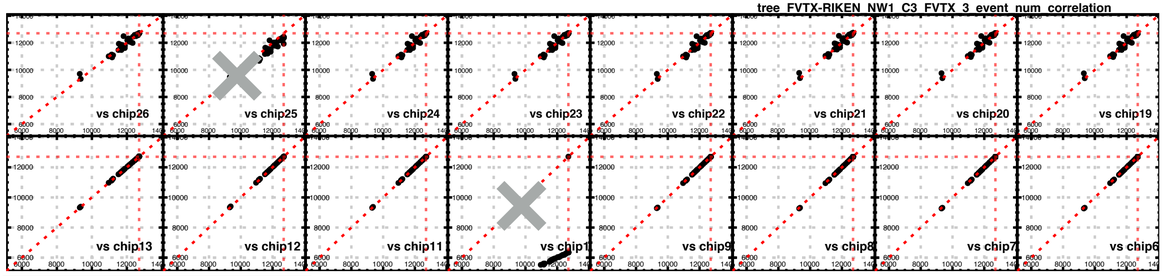
riken_fphx_raw_20210811-1803_0.dat



chip10: always half entry → somewhere dead?
chip25: some channels are dead

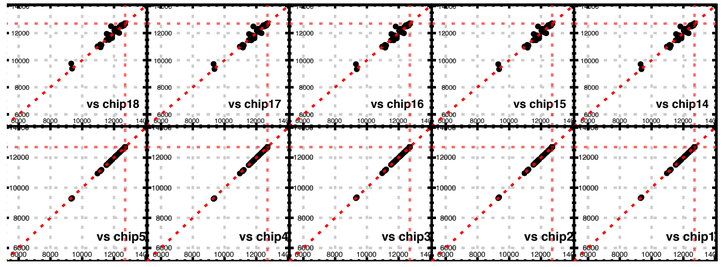
Calibration tests at the RIKEN testbench, What about FVTX?

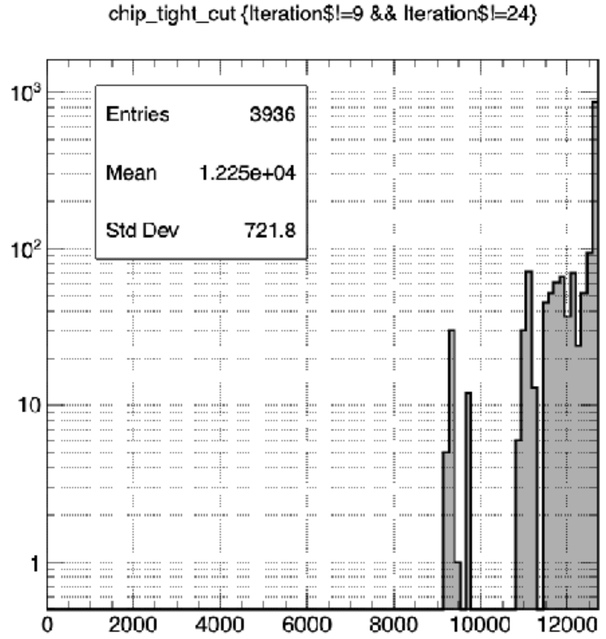




vs Chip1

Chip2-13 have almost the same events as chip1's.
Correlations of chip14-26 distribute around y = x.





#Chips with 60%~105% entry：3936

#Chips with 60%~90% entry ：168

→ Successful ratio: 95.7%

Even FVTX sometimes have less-entry than the ideal case.
INTT silicon module must be fine since FVTX was operated successfully.
Where is the problematic point?

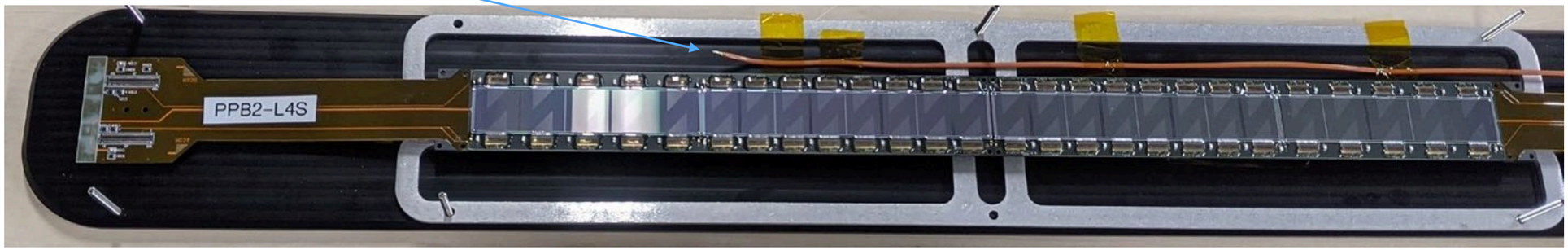
Calibration stability and ladder temperature

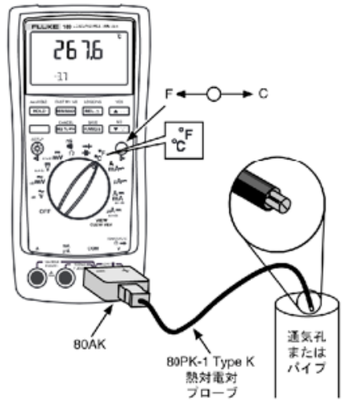
Calibration stability and ladder temperature

Key features: 80BK-A

- Type-K thermocouple with standard shrouded banana jack
- Convenient one piece construction
- Compatible with DMMs with temperature measurement functions
- Measurement range: -40 to 260ºC
- Accuracy: +/- 2.2 °C or 2% whichever is greater ((0 to 260 °C)

Differences between INTT testbenches and 1008 environment may be related to the less-entry issue. Since there is no cooling system for the ladder, we tried calibration tests with a new cooling system for the ladder. Ladder temperature around the ladder was monitored with a thermocouple sensor (type-K, FLUKE 80BK-A, -40 °C ~ 260 °C).





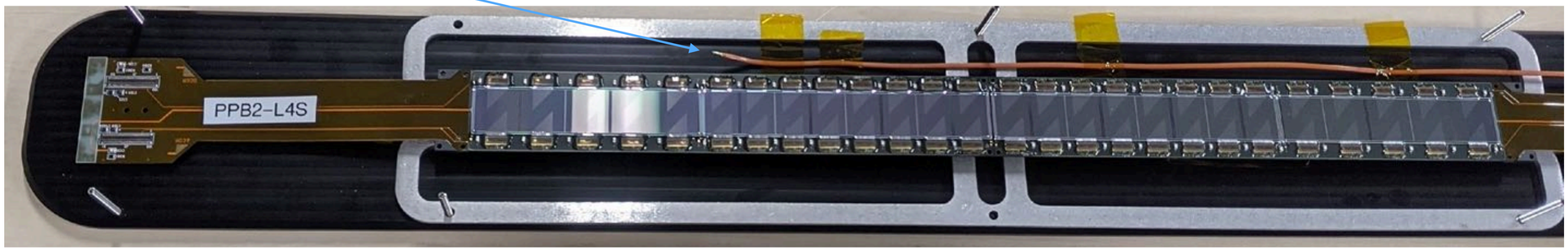
The thermocouple was installed next to the ladder. The transportation box was closed and shaded during the measurements.

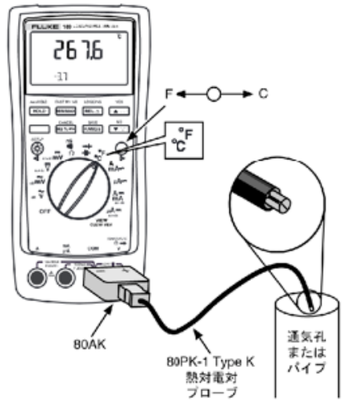
Calibration stability and ladder temperature

Key features: 80BK-A

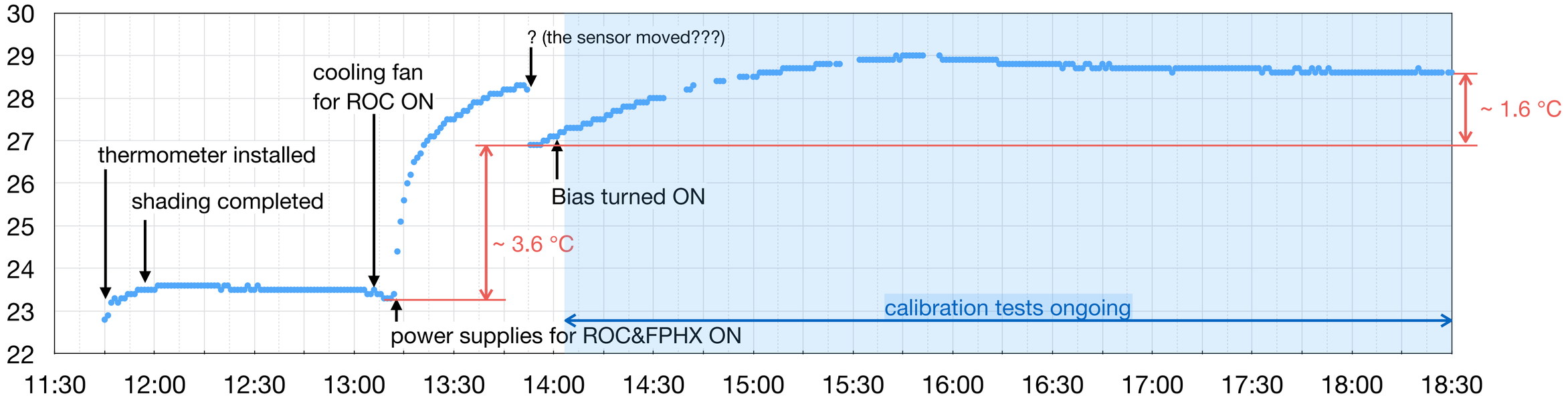
- Type-K thermocouple with standard shrouded banana jack
- Convenient one piece construction
- Compatible with DMMs with temperature measurement functions
- Measurement range: -40 to 260ºC
- Accuracy: +/- 2.2 °C or 2% whichever is greater ((0 to 260 °C)

Differences between INTT testbenches and 1008 environment may be related to the less-entry issue. Since there is no cooling system for the ladder, we tried calibration tests with a new cooling system for the ladder. Ladder temperature around the ladder was monitored with a thermocouple sensor (type-K, FLUKE 80BK-A, -40 °C ~ 260 °C).



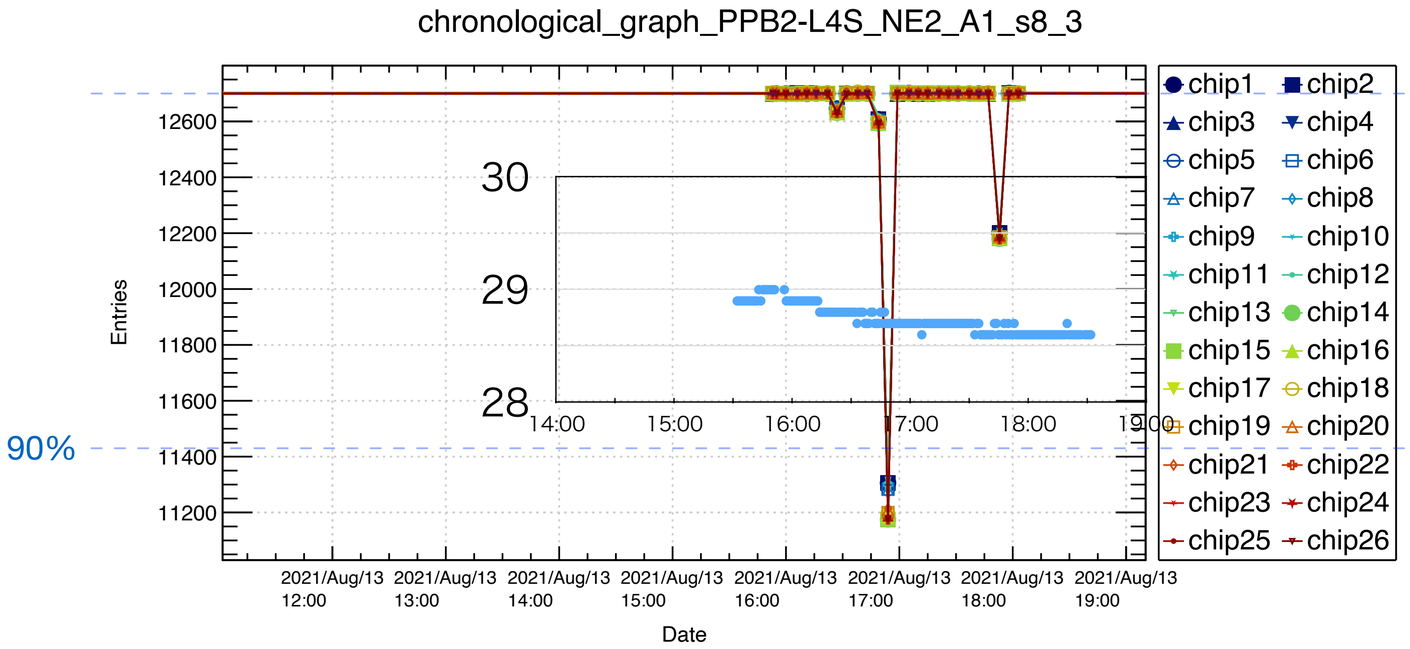


The thermocouple was installed next to the ladder. The transportation box was closed and shaded during the measurements.

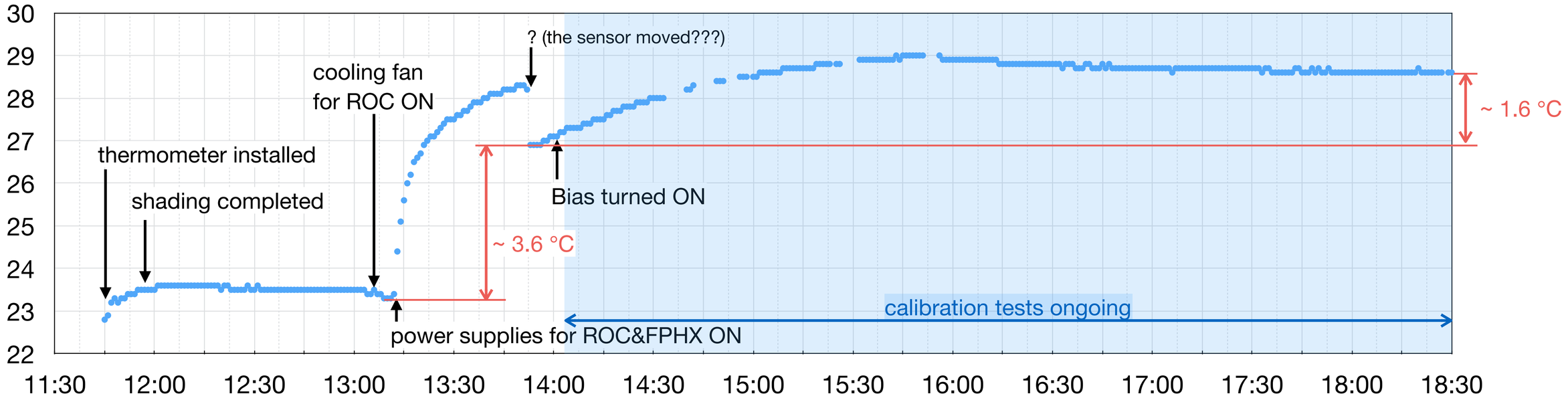


Calibration stability and ladder temperature

Ladder: PPB2-L4S
ROC: NE2(upgraded 1008 ROC)
ROC port: A1
Conversion cable: short8

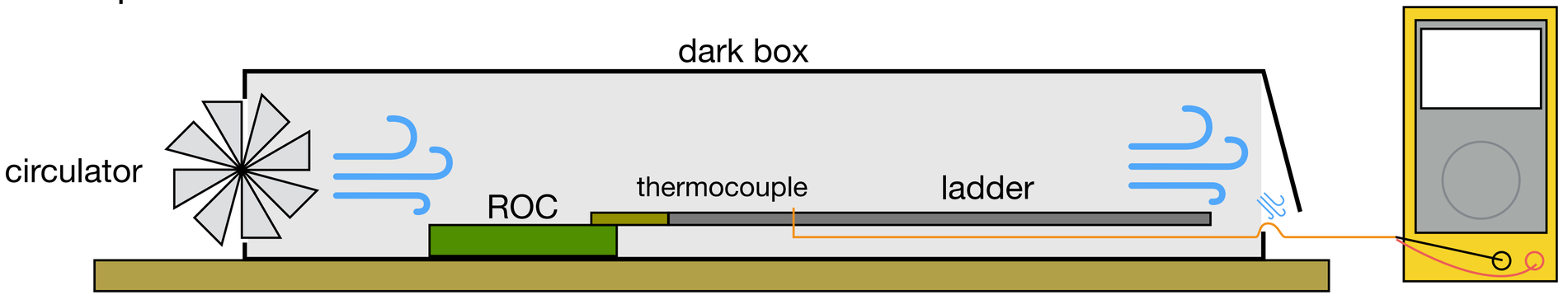


#Chips with 60%~105% entry：676
#Chips with 60%~90% entry ：26
→ Successful ratio: 96.2%



Calibration stability and ladder temperature, Ladder cooling

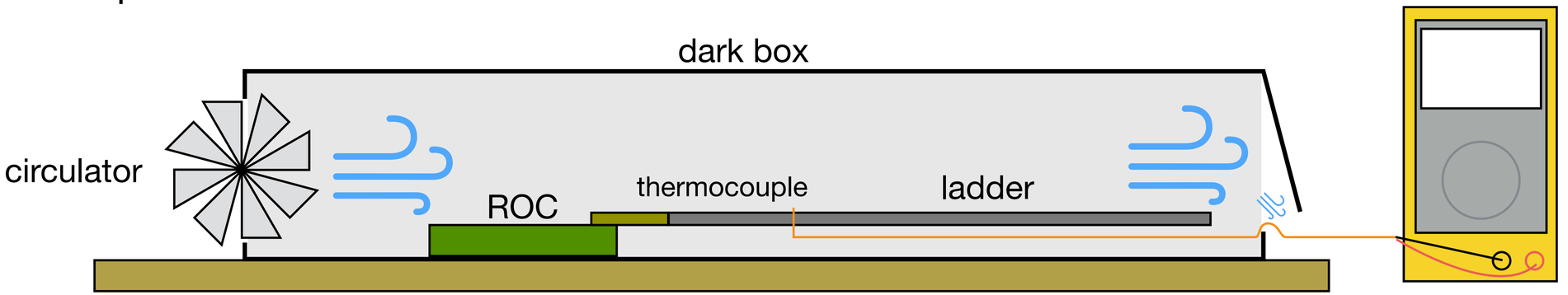
The setup was modified to cool ladder down.



The setup

Calibration stability and ladder temperature, Ladder cooling

The setup was modified to cool ladder down.

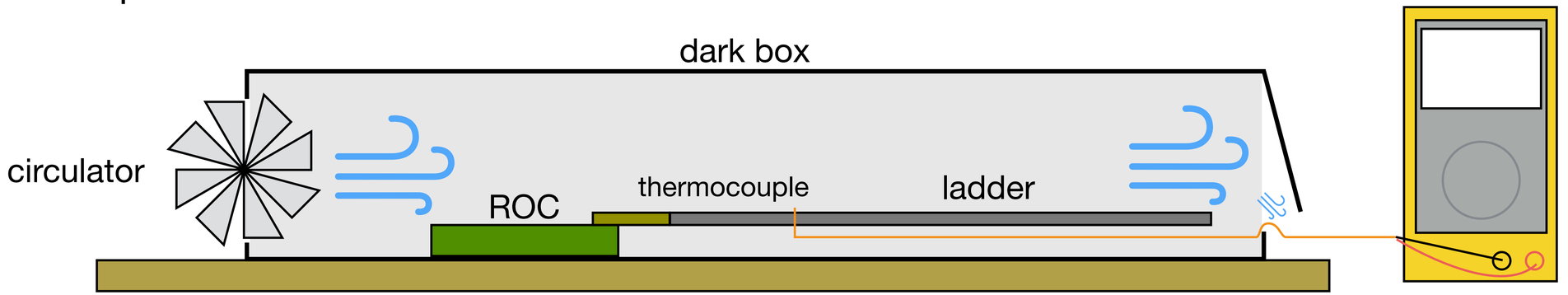


The setup

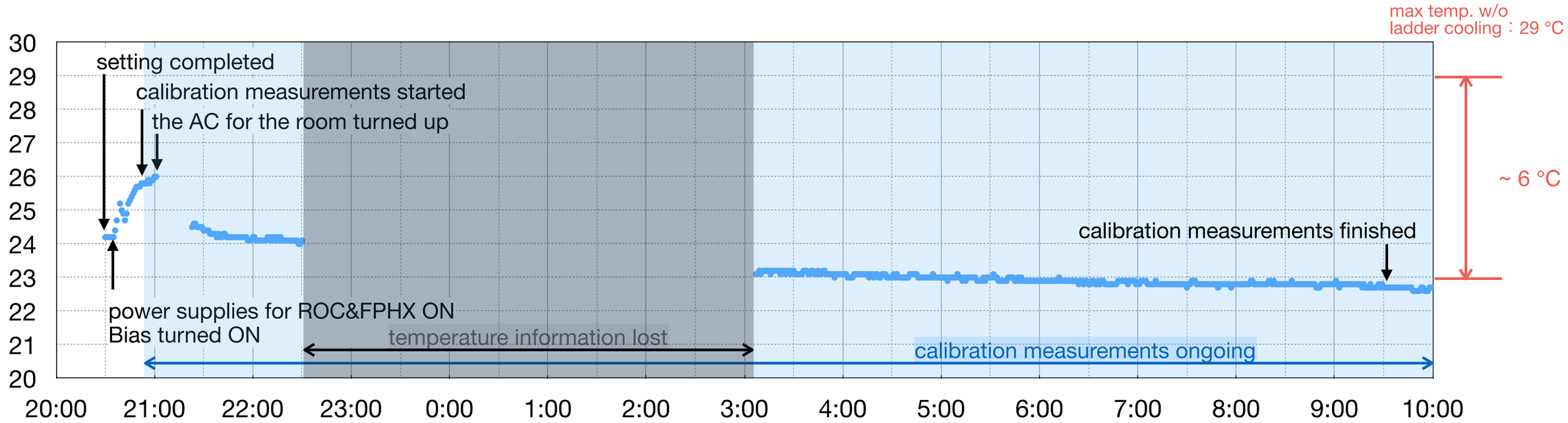
View from downstream

Calibration stability and ladder temperature, Ladder cooling

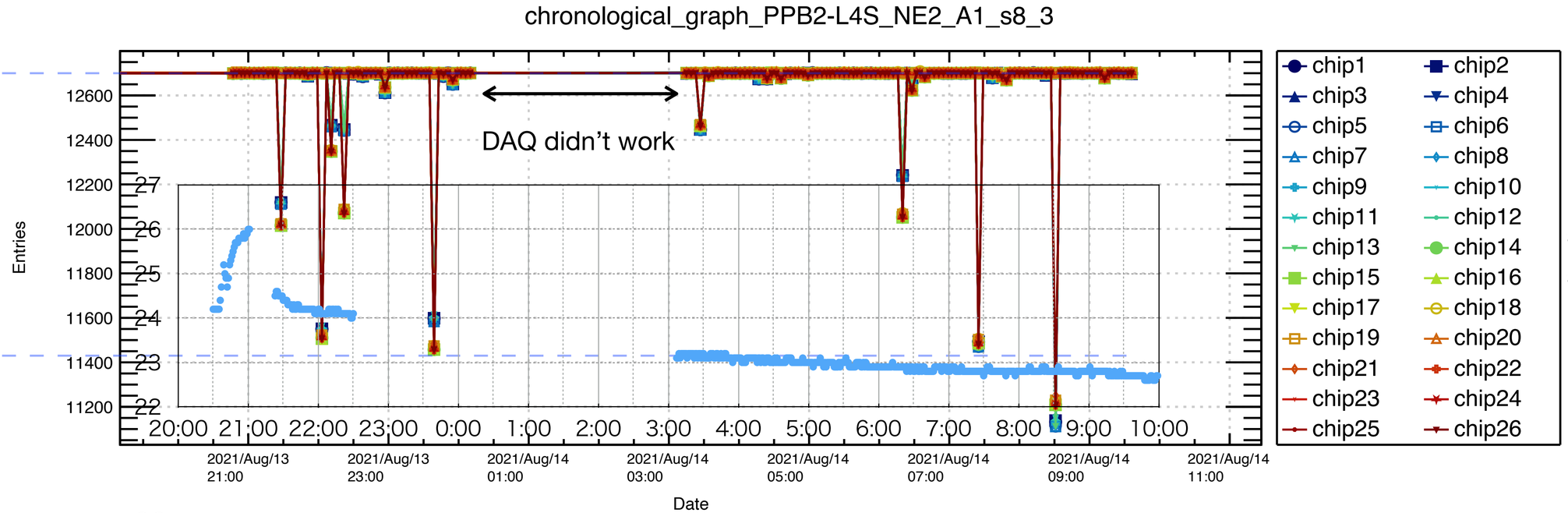
The setup was modified to cool ladder down.



The setup



Calibration stability and ladder temperature, Ladder cooling

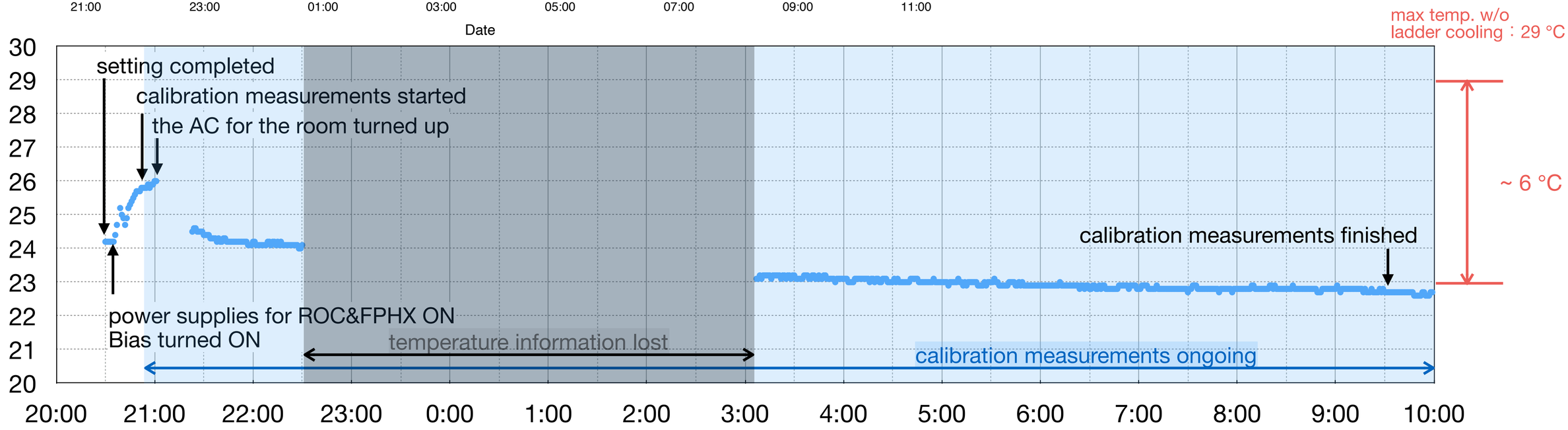


#Chips with 60%~105% entry：4030

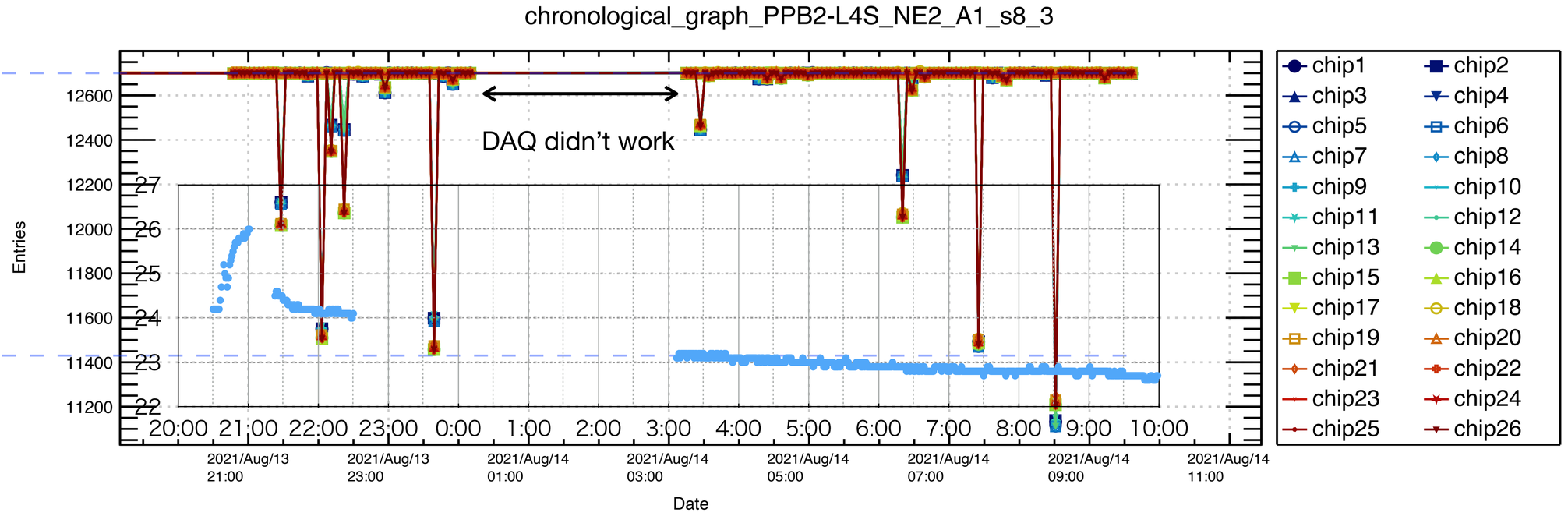
#Chips with 60%~90% entry ：26

→ Successful ratio: 99.4%

The ratio might be better???



Calibration stability and ladder temperature, Ladder cooling



Ladder: PPB2-L4S
ROC: NE2(upgraded 1008 ROC)
ROC port: A1
Conversion cable: short8

	Date	#Run	#Less-entry chip	#chip	Good chip ratio
w/ cooling	Aug/13-14	155	26	4030	99.4%
w/o cooling	Jul/16	26	0	156	100.0%
w/o cooling	Aug/13	26	26	676	96.2%
w/o cooling (total)		52	26	832	96.9%

The ratio with the cooling might be higher than those without the cooling.
Note.
Measurements on 7/16 shows 100%.
Some measurements also shows 100%.

Calibration stability, next step

The new cooling system for the ladder worked well, but the results were not conclusive.
For better stability for the calibration measurements, we are going to try

- more powerful cooling for ROC
- better GND condition
- new cable for BCO board