

# STAR Forward Calorimeter Frontend and Readout, and application at EIC

T. Camarda, T. Ljubicic (BNL), O. Tsai (UCLA),  
G. Visser (Indiana U.)

8/23/2021

## Overview



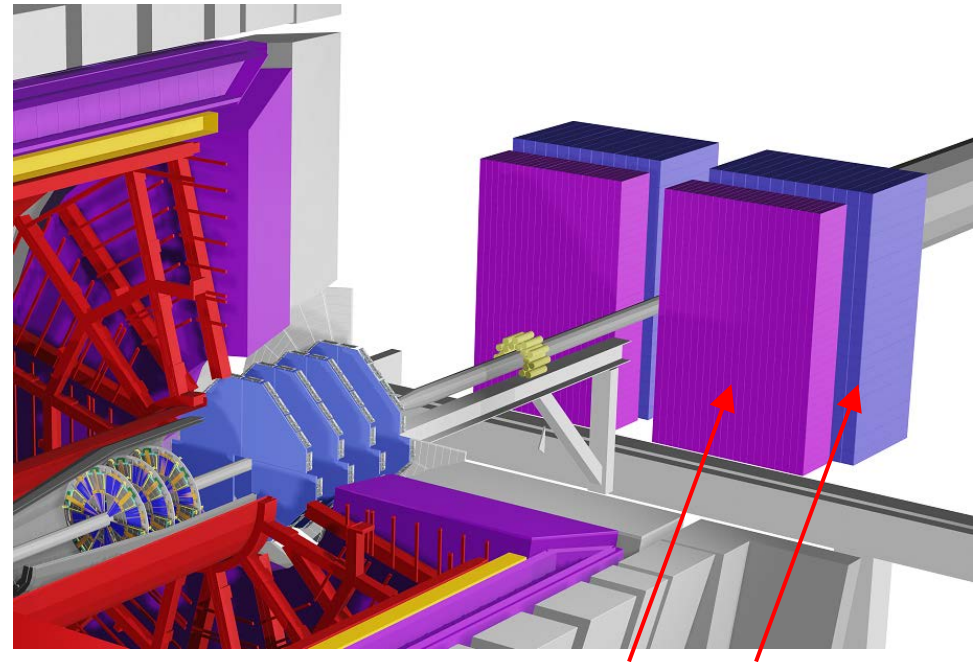
Rear view of Noth HCAL before FEE installation

### ECAL:

44 × 34 towers 5.6 cm square, split in two halves N/S of beampipe  
FEE boards 2 × 2 towers, 374 FEE boards  
depth (SiPM+FEE+cables) less than 5 cm

### HCAL:

26 × 20 towers 10 cm square, split in two halves N/S of beampipe  
FEE boards 1 × 2 towers, 260 FEE boards  
depth (SiPM+FEE+cables) less than 5 cm

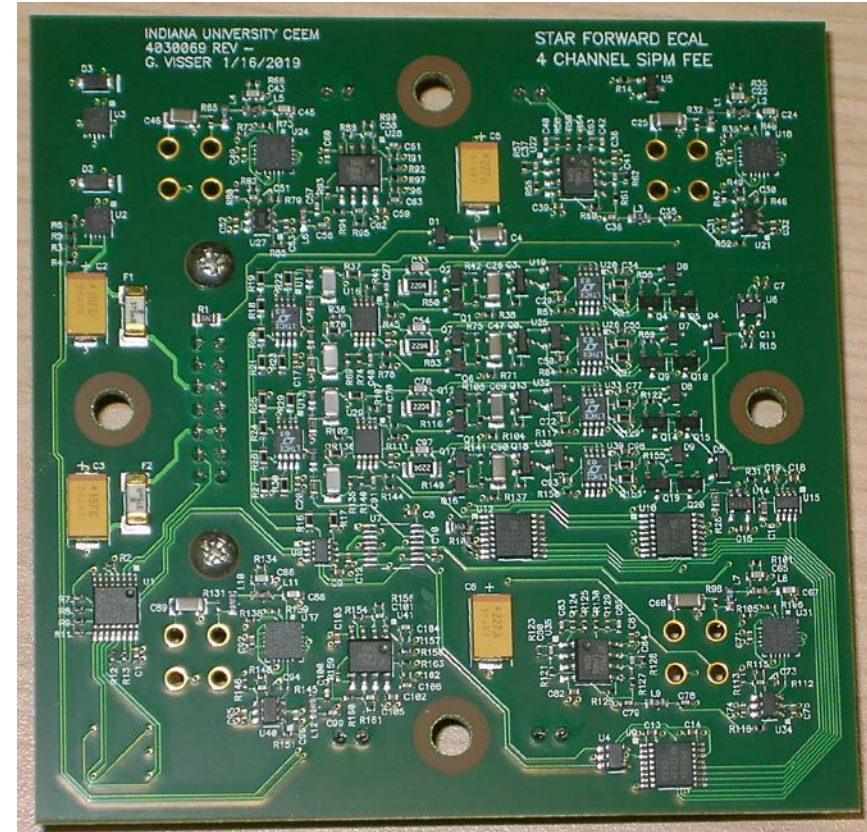


Cutaway view of STAR with ECAL & HCAL

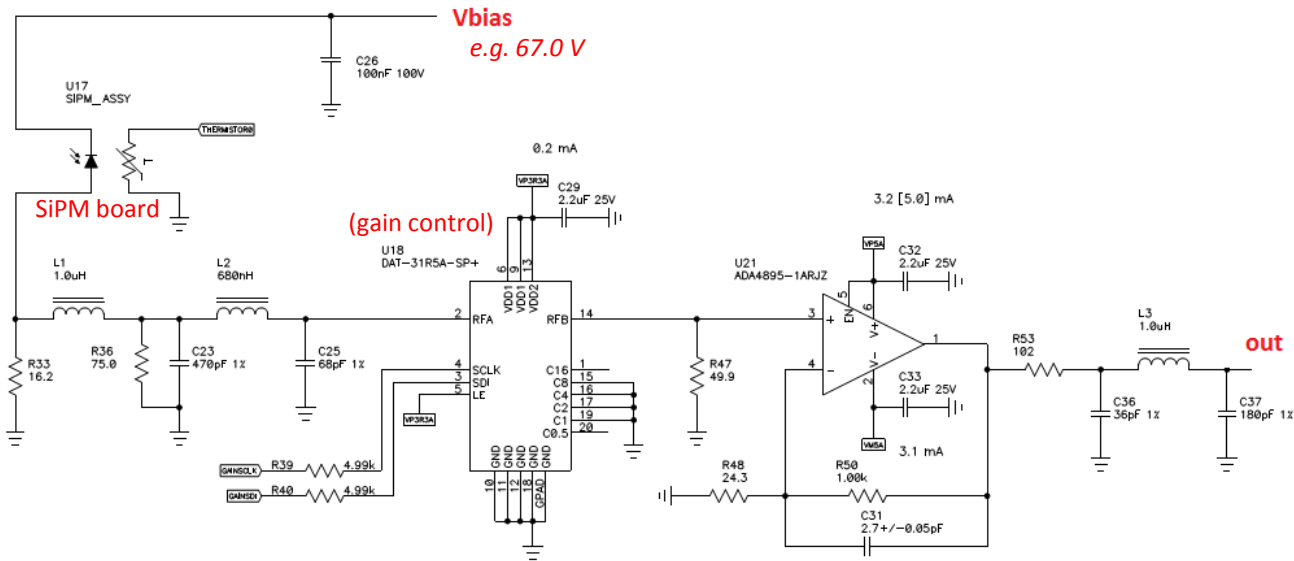
## Design goals

- Frontend amplifier and signal shaping on detector
- SiPM bias voltage control on detector
  - Including simple local analog temperature compensation
  - Including SiPM current monitoring
- Separate SiPM/thermistor and FEE boards
  - Production at two sites UCLA / IU
  - Lower cost to replace SiPM (for upgrade or rad. damage)
  - Multichannel FEE with loose tolerance on tower(SiPM) positions
- Services (+/-6 V, +80 V, I<sup>2</sup>C controls) on low cost multidrop flat cable
- Differential signal output for reasons of size, cost, and noise immunity
  - Micro-ethernet cable on detector
  - 3M loose pair CL2 cable the rest of the way to ADC's
- Waveform digitizer readout (BNL – “DEP” board)
  - “80” (75.06 = 8×RS) MSPS, 12 bits
  - Pulse arrives already shaped from FEE
    - DEP is **general purpose** (in fact we use also for preshower)
    - Shaping the pulse on detector makes best use of driver/cable dynamic range
  - Triggered readout in STAR, but DEP is also intended as a development platform for streaming readout

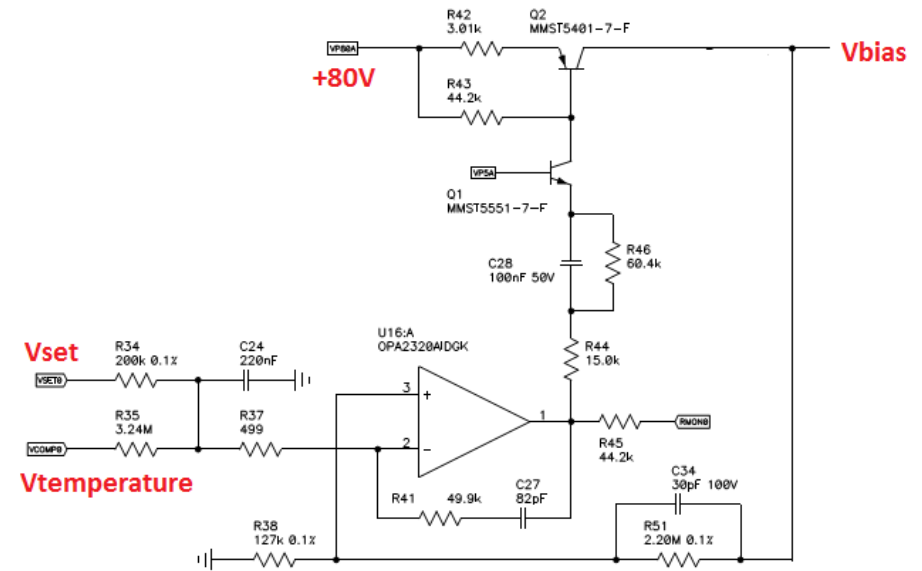
## FEE Implementation – ECAL



## Frontend and bias



- ECAL 4x, HCAL 6x 3x3 mm<sup>2</sup> SiPM's
- SiPM with small load resistor, followed by voltage amplifier
  - for best possible linearity – *speed and linearity of the amplifier are not involved in sweeping charge out of SiPM*
  - load resistance  $\ll 50 \Omega$  is best
- some shaping before any amplifier – so that amplifier *does not have to linearly follow pulse as fast as SiPM produces*
- more shaping after amplifier – noise limiting
- for STAR we included gain control as thought necessary for cosmic ray calibration. omit/simplify for EIC application...



- simple but precise and low noise bias voltage regulator
- inherent current limiting – no series resistor needed to protect SiPM
  - more stable bias voltage  $\rightarrow$  more stable gain
- fast recovery 3  $\mu$ s to 2 mV after full scale signal pulse
- current monitor (not shown above) – optional, but useful!
- Vset and **slope** of Vtemperature set by DAC's

## FEE Connections

SiPM board per tower, glued to light guide. Connection from FEE by pogo pins. Large tolerance of transverse location (several mm). **Easy blind installation** (*once dimensions verified by fixture*).

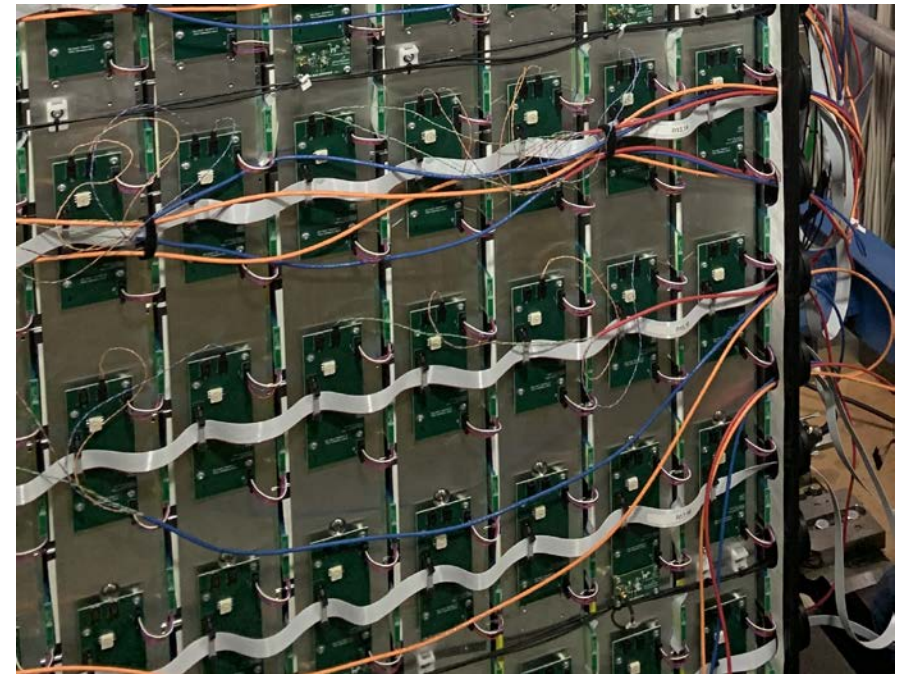


Cooling of FEE: Air is drawn out from top of the enclosure. Enters at bottom, through baffles for light tightness.

Power inside detector: 180 mW/ch (e.g.  $\frac{1}{2}$  ECAL is 136 W)



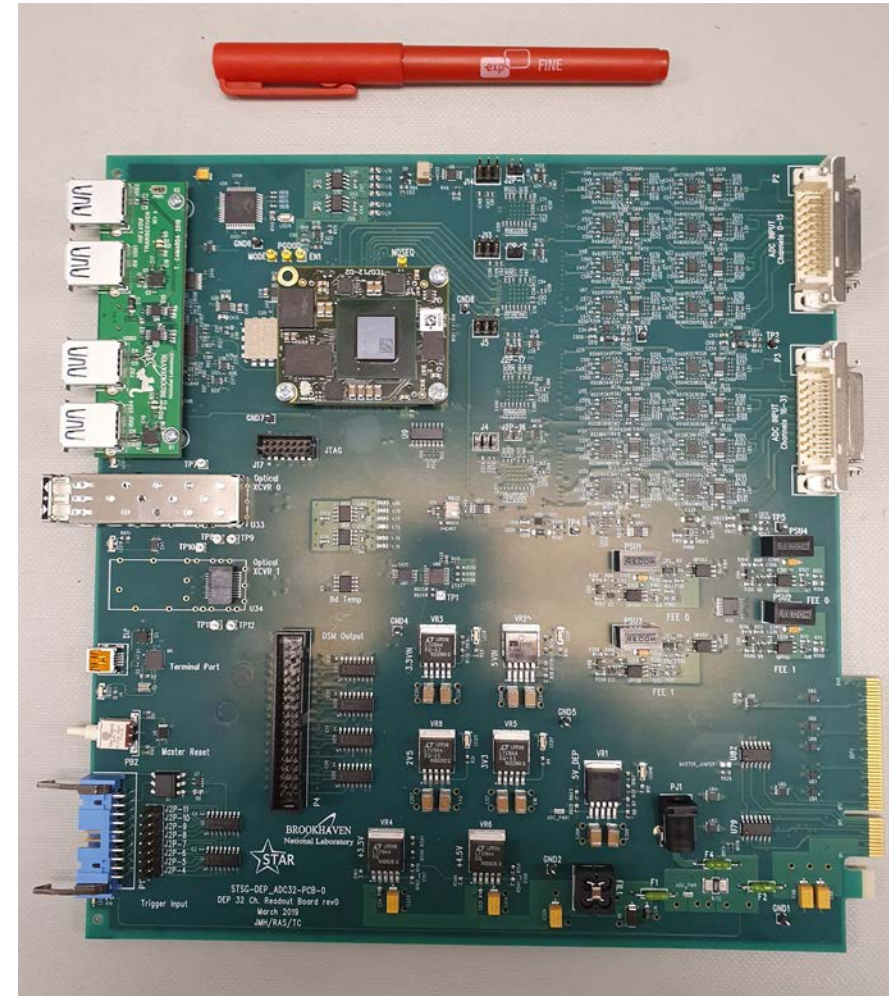
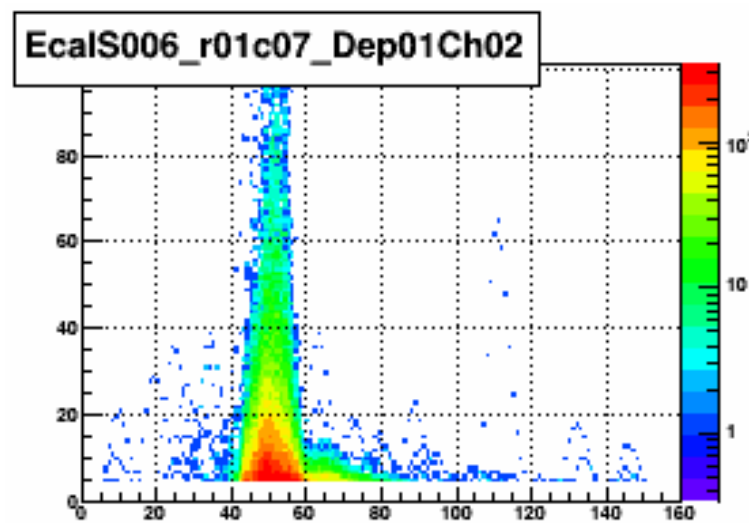
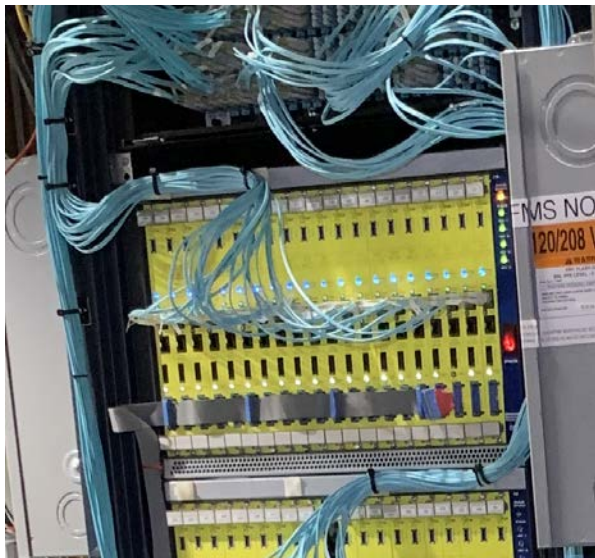
Patchpanel boards on sides of detector: Transition to long signal cables. Group power rows into power groups. +80V power supplies.



HCAL: Same concepts, except short cable connection to SiPM board instead of pogo pin connection. Much more room than ECAL.

## DEP ADC Board

- 32 channel 80 MSPS 12 bit ADC (P/N AD9637); pin compatible 14-bit upgrade
- high CMR line receiver inputs (same as GlueX ADC125)
- FPGA on Trenz Module – upgradeable!
- 2× 3.2 Gb/s fiber links ( $\approx 512$  MB/s) to DAQ PC
  - In practice w/ current receiver/PC we measure  $\approx 460$  MB/s, plenty for STAR, room for improvement for future
- Expect  $\approx 40$  bits per hit for summary info (amplitude, time, etc.) for a streaming mode readout
- This is “DEP ADC” – there is also “DEP IO” a trigger processor with fiber input instead of ADC
- DEP ADC also includes 2× opto-isolated I<sup>2</sup>C masters for FEE controls

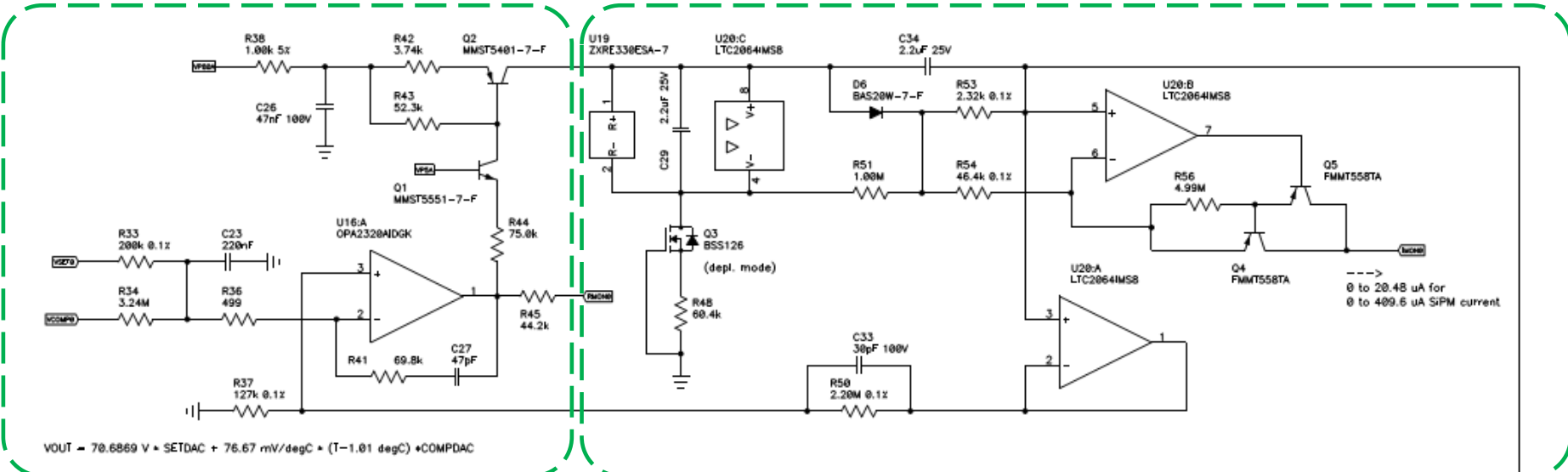


BACKUP SLIDES



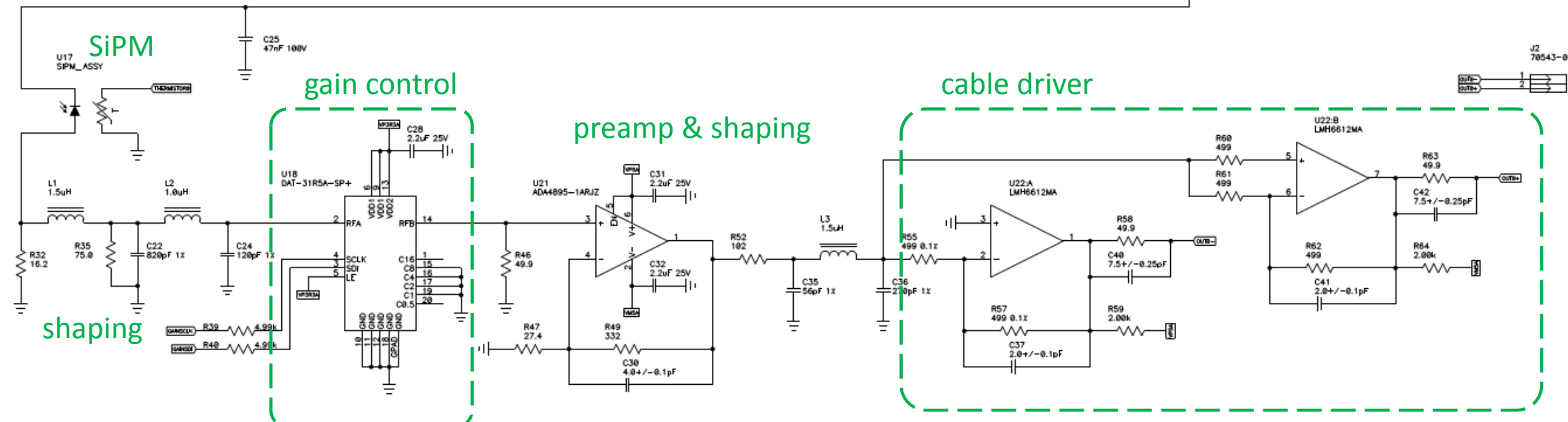


# BACKUP – complete bias and signal schematic of one channel



bias regulator

current monitor



shaping

gain control

preamp & shaping

cable driver