Preliminary Roman Pot DAQ considerations

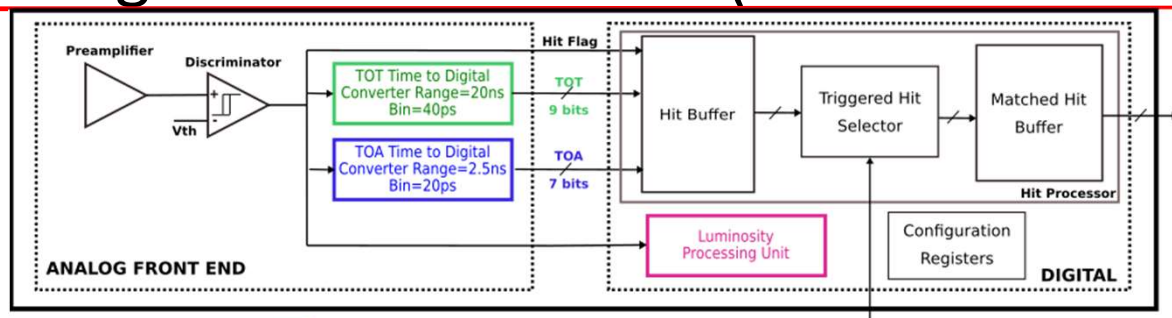
Outline:

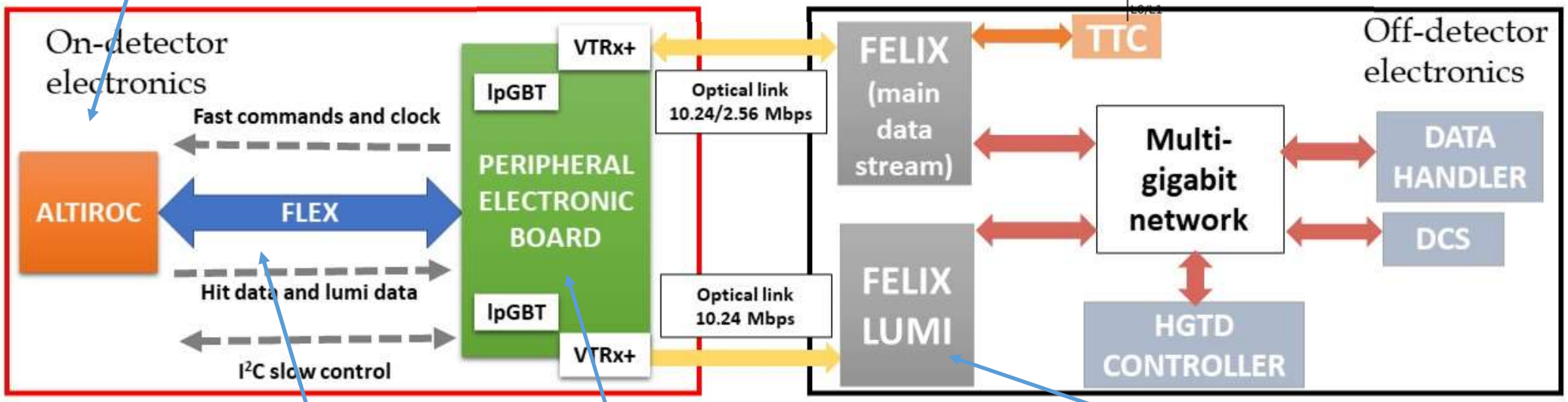
1) The ATLAS readout system for timing detector (HGTD) using DC LGAD
2) Key numbers / extrapolation for Roman Pots at EIC

ATLAS HGTD design and architecture (DC-LGAD sensors)

1 module = 2 ASIC ALTIROC (225 chan each) ATLAS HGTD 16000 ASIC

Timing data only when a hit, read from ASIC only on L0 trigger accept (1 MHz, latency 10 µs)





E-link (< 1m) from ASIC to peripheral electronics
- up : Data with 3 different speeds
- Down : I2C control (slow control parameters)
- Fast command (calibration, trigger, reset info), 8 bits at 40 MHz
- Clock

E-link speed (Mbps)	Number of e-links
1280	1856
640	4864
320	9344

7 (@1280 Mb/s) or 14 (@640 MB/s) or 28 (320 Mbs) e-links fed in one lpGBT with 10.24 Gb/s output optical link for data
1 down link at 2.56 Gb/s shared by 16 ASICs

FELIX board (developed by BNL) for ATLAS upgrade Phase I/II, 16 or 32 10 Gb/s input links

ATLAS HGTD design and architecture

ATLAS ASIC occupancy from a few per mil to 10 % depending on radius

ATLAS average event size from 150 to 250 kBytes

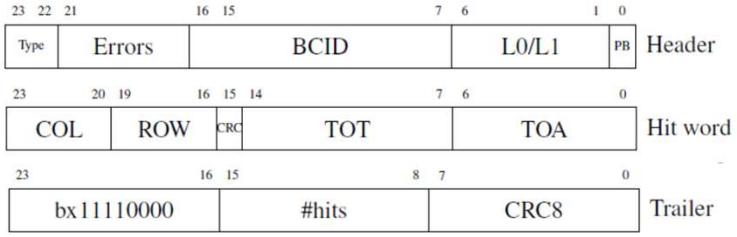
ATLAS Data format :

8 bits fast commands (@ 40 MHz)

Command	Bit field	Description
IDLE	10101100	IDLE frame
TRIGGER	10110010	L0 or L1 trigger
BCR	10011001	Bunch Counter Reset
TRIGBCR	01101001	Trigger and BCR
CAL	11010100	Calibration Pulse
GBRST	11001010	Global Reset
SYNCLUMI	01100110	Synchronize luminosity stream
SETTRIGID	01010011	Set Trigger ID
TRIGID	01xxxx01	Trigger ID

Table 2: Fast commands

Data format : 24 bits word with 8b10b encoding.

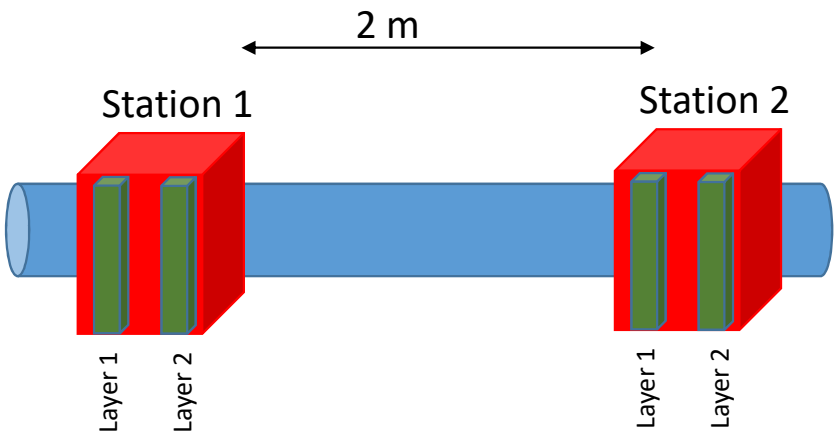


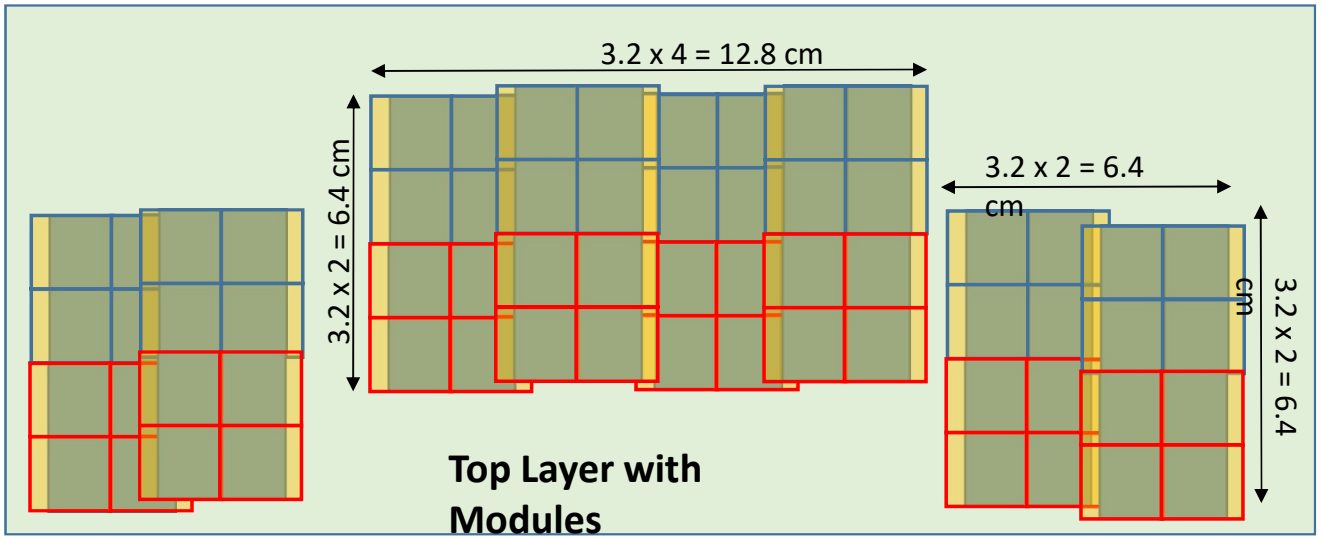
16 bits of timing information / per pixel

Slow control parameters through I2C 960 with 8 bits registers :

- 4 per pixels → 900 registers
- 60 for global slow control

Roman pots detector





Baseline for detector

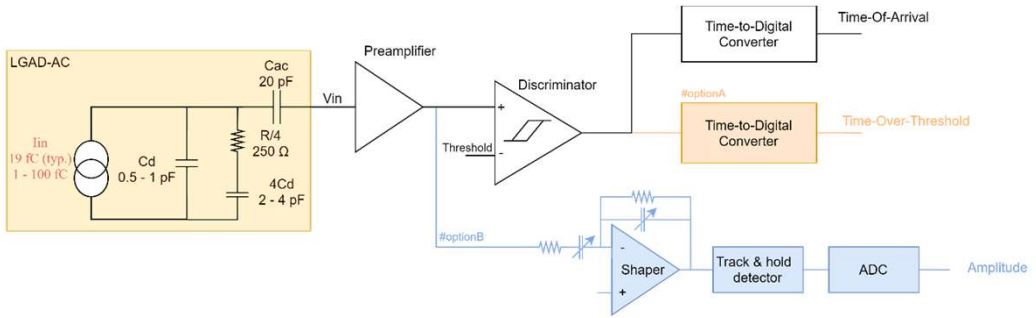
- Two stations with two layers and 0.5x0.5 mm2 pixels of AC-LGAD (charge sharing)
- In each layer : 32 quad modules per layers, 1 module is 4 ASICs → 128 ASIC per layer
- Total : 128 Modules / 512 ASICs (524 288 Channels)
- ASIC size : 1.6 x 1.8 cm^2 with 1024 channels (32x32)

Extrapolation to EIC Roman Pots readout

Two architectures for the Front End under study :

- ATLAS HGTD like (option A) with TOA + TOT.
  As needed to read neighbour pixels of the hit one discri threshold might not low enough and deteriorate position resolution.
- ASC measurements instead of TOT measurement but need to control power dissipation. Gated ADC and logic to read the 8 neighbours

Proto expected to be submitted end 2021/early 2022



Trigger-less acquisition

Expected vey low occupancy : < 30 hits/pixel/s (not including the neighbours, so a factor of ×9 should be accounted for in the readout, especially when using ADC
(assume threshold at >5 sigma of noise)

If 32 bits data for a hit

→ data rate is 30x32*1024=~1 Mbits/s per ASIC or 9 Mbits/s with neighbours

→ 128 Mbits/s per layer or 1152 Mbits/s (Still to validated by simulation)

→ Total detector data rate 512 Mbits /s 4608 Mbits/s

Slow control information : similar numbers of parameters as ATLAS

Extrapolation to EIC Roman Pots readout

Data transmission from ASIC to DAQ

- No radiation hardness needed in EIC and low ASIC rate with respect to ATLAS : using lpGBT is not well suited
- Commercial concentrator or custom FPGA board ? One board per layer would have do deal with 128 ASICs and < 200 Mbytes/s of data