Readout of CyMBaL tracker for Athena@EIC

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Athena DAQ WG meeting

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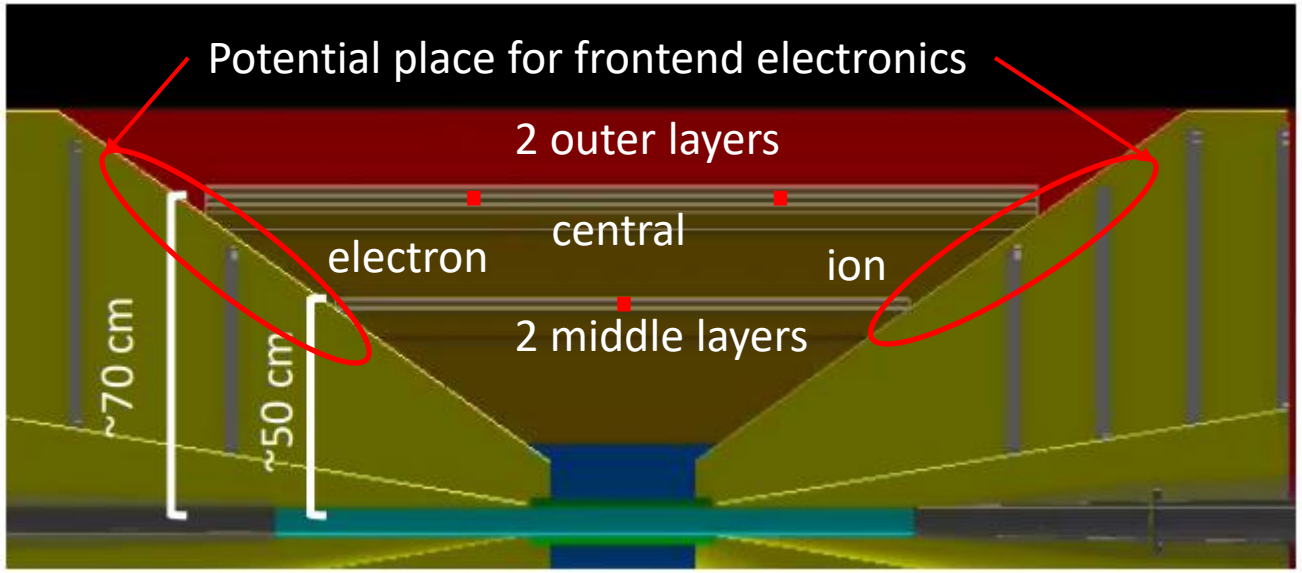
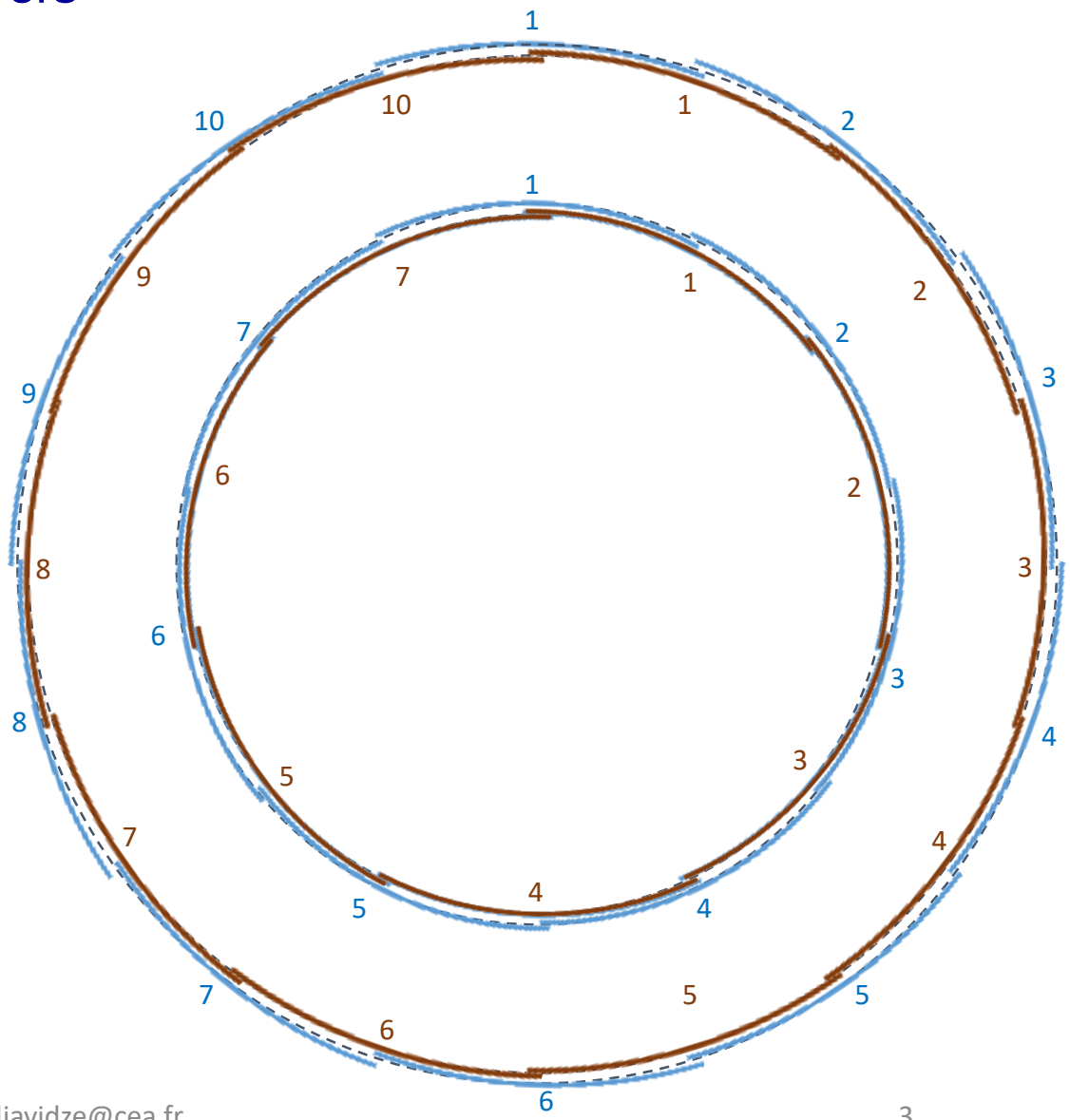
CyMBaL (CYlindrical Micromegas BArrel Layers) tracker for Athena@EIC

- 4 layers
  - → 2 middle and 2 outer
  - → 2D strip readout
    - Z + C strips per layer
  - → Middle layers built in 2 modules along Z (beam) axis: electron side and ion side
  - → Outer layers built in 3 modules along Z (beam) axis: electron side, central and ion side
    - On-going study on how to connect central modules to electronics (flex cables?)
- Number of channels
  - → 1.45 mm pitch: 66 000 strips
    - 28K Z-strips & 39K C-strips
    - Assume as a baseline
      - May vary though
- Environment
  - → Scarce space for electronics
    - Can nevertheless be placed on both sides
  - → Magnetic field
  - → Material budget restrictions
    - Impact on cooling
  - → Radiation?

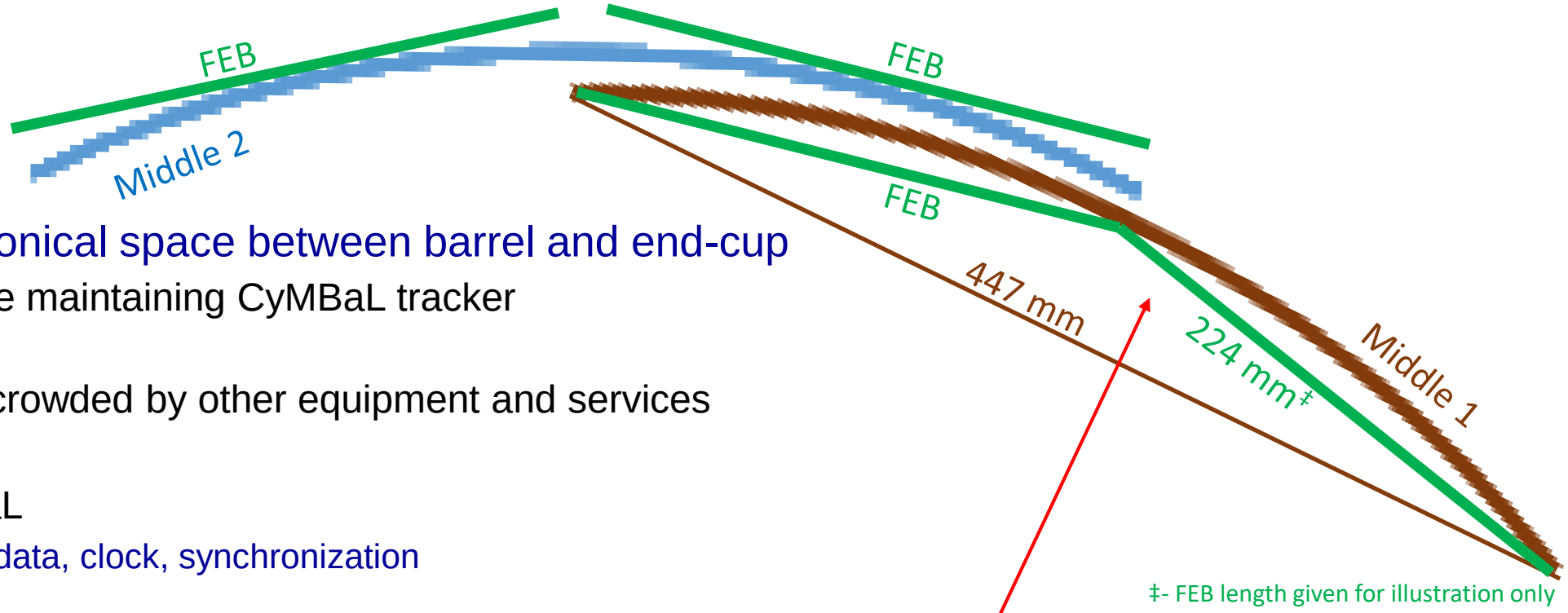


CyMBaL tracker for Athena@EIC

- Same base detector to assemble middle and outer layers
  - → Curved according to layer radius
  - → Active area: ~650 mm length x ~465 mm width
    - 1.45 mm pitch
    - 448 “C” strips + 320 “Z” strips
- Two middle layers
  - → 2 x 7 base detectors each
  - → Radial distance 15 mm
- Two outer layers
  - → 3 x 10 base detectors each
  - → Radial distance 15 mm
- Avoid dead zones
  - → Tilted detectors ensuring overlap

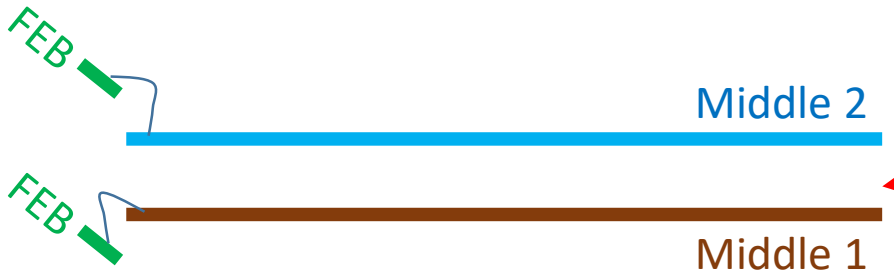


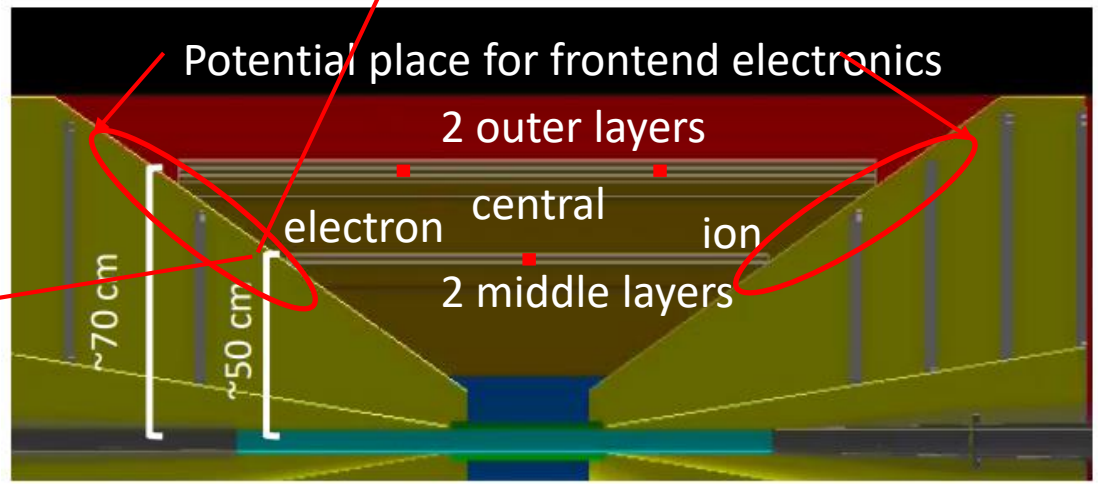
Space for CyMBaL module electronics



- Place FEBs in the conical space between barrel and end-cup
  - → Fixed on structure maintaining CyMBaL tracker
    - Not shown
  - → Probably will be crowded by other equipment and services
  - → Proper to CyMBaL
    - Readout link: data, clock, synchronization
    - LV, HV, gas
    - Cooling?
    - Slow control and monitoring?
      - Through readout link for FEB?

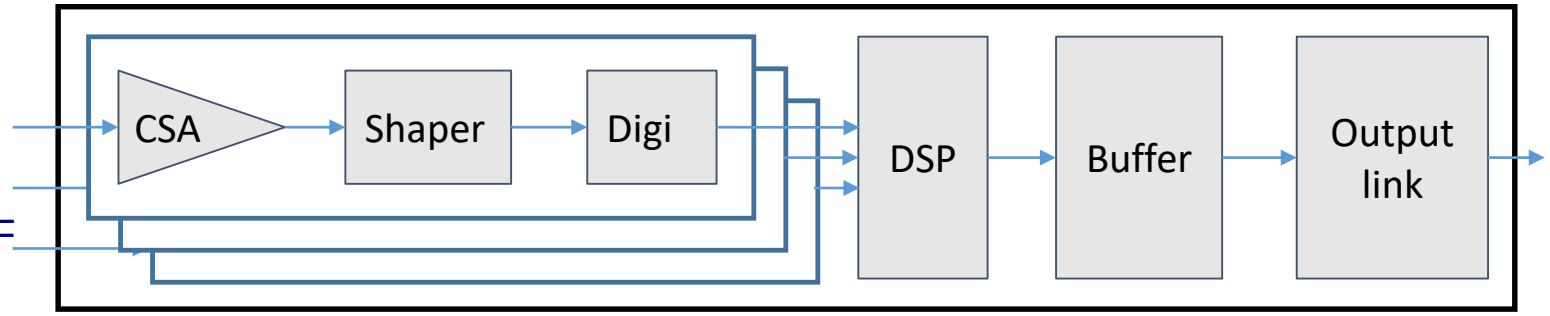
‡- FEB length given for illustration only





CyMBaL tracker frontend

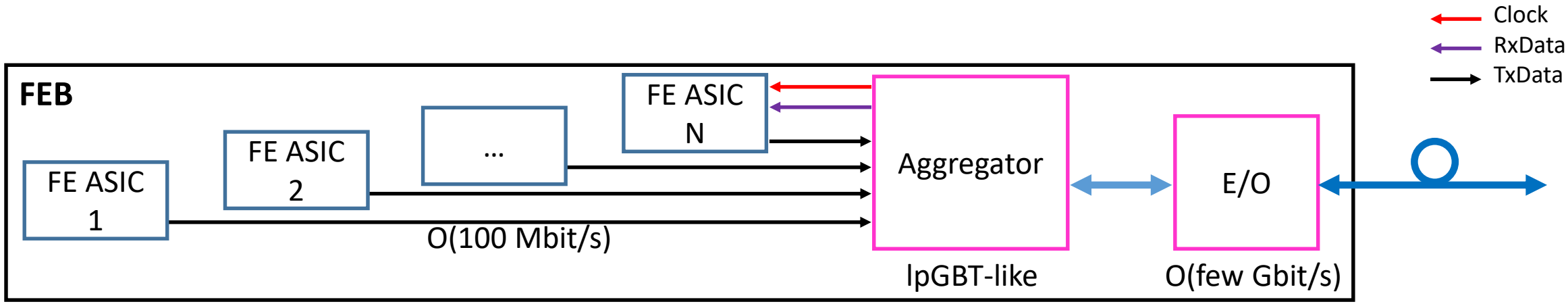
- FEBs based on multi-channel MPGD ASICs
  - → Compatible with streaming readout
  - → Typical characteristics
    - Gain: 10 down to 4 mV/fC
    - Peaking time: 75 to 300 ns
    - Detector capacitance: up to 400 pF
    - 10-12 bit ADC and/or 10-bit TDC
  - → On-chip zero suppression
    - Possibly with common mode noise subtraction
    - Sampling ZS: signal shape around ToT
    - Peak finding ZS: amplitude, time and ToT



- Existing ASICs
  - → 32-channel Sampa: sampling
  - → 64-channel VMM3a: peak finding
- Next generation ASIC
  - → On-going common initiative between Brazilian institutes (Sampa) and Irfu (AGET, Dream)
    - Most probably a 64-channel sampling ASIC with common mode correction
    - See for example: https://indico.cern.ch/event/1040996/contributions/4402636/

CyMBaL tracker frontend (cont.)

- LHC-like frontend organization?
  - → A bi-directional link for clock, synchronization (run control), data, slow control
  - → Assumes existence of lpGBT-like aggregator ASIC or requires a new development
    - Point to point connections between frontend ASICs and an aggregator ASIC
      - Downstream path is only partially shown



It is not clear if there will be a central (Athena, EIC) group responsible for aggregation / frontend link

CyMBaL tracker frontend data rate: **sampling readout**

- Sampling ASIC with 12-bit sample per channel
- Signal shape ZS

  → 500 ns readout window when signal is above threshold

- 32-channel ASIC (e.g. Sampa) and 256-channel FEB (e.g. sPhenix FEE for TPC)

Channel rate kHz		Sampling MSPS	Number of samples	32-chanel ASIC Mbit/s	256-chanel FEB Gbit/s	Remarks
2	(physics)	20	10	19	0.16	5-10 Gbit/s aggregation link unjustified
10	**(safe)**			**92**	**0.75**	
50	(Clas12)			460	3.7	5-10 Gbit/s aggregation link justified

- New development: 64-channel ASIC and 512 FEB

Channel rate kHz		Sampling MSPS	Number of samples	64-chanel ASIC Mbit/s	512-chanel FEB Gbit/s	Remarks
2	(physics)	50	25	46	0.4	5-10 Gbit/s aggregation link unjustified
10	**(safe)**			**230**	**1.9**	**5 Gbit/s aggregation link is enough**
50	(Clas12)			1 150	9.5	20 Gbit/s aggregation link needed

CyMBaL tracker frontend data rate: **peak-finding readout**

- Peak-finding ASIC
- ZS with time-amplitude readout
  → Assume 12-bit timing, 8-bit ToT and 12-bit amplitude

- 64-channel ASIC (e.g. VMM3a) and 512-channel FEB (e.g. Atlas NSW FEM8)
  → Or a new development

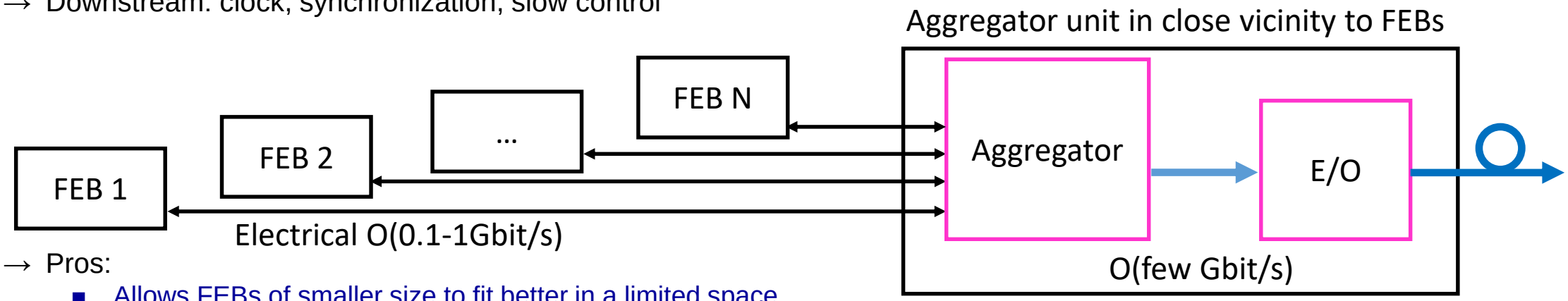
Channel rate kHz		64-chanel ASIC Mbit/s	512-chanel FEB Gbit/s	Remarks
2	(physics)	5	0.04	5-10 Gbit/s aggregation link unjustified
10	**(safe)**	**25**	**0.2**	
50	(Clas12)	125	1	2 Gbit/s aggregation link is enough

Good knowledge of channel occupancies (physics, background, noise) is important

A question on aggregation: local concentrator card

- High speed FE-BE connections assume enough aggregated bandwidth to justify multi-Gbit/s links
  - → 5-10 Gbit/s or higher
  - → Especially if the use of lpGBT for EIC is envisaged

- Is a local concentrator card needed?
  - → Upstream: only data aggregation, no data treatment
  - → Downstream: clock, synchronization, slow control



  - → Pros:
    - Allows FEBs of smaller size to fit better in a limited space
      - e.g.256-channel or even 128-channel FEBs rather than 512-channel FEBs
    - Potentially lower power consumption
    - Could be used by several sub-detectors
  - → Cons:
    - More boards to produce and maintain
    - More complex communication protocol between FEBs and aggregator unit

If there is an interest, should there be a central group to define/design the aggregator?

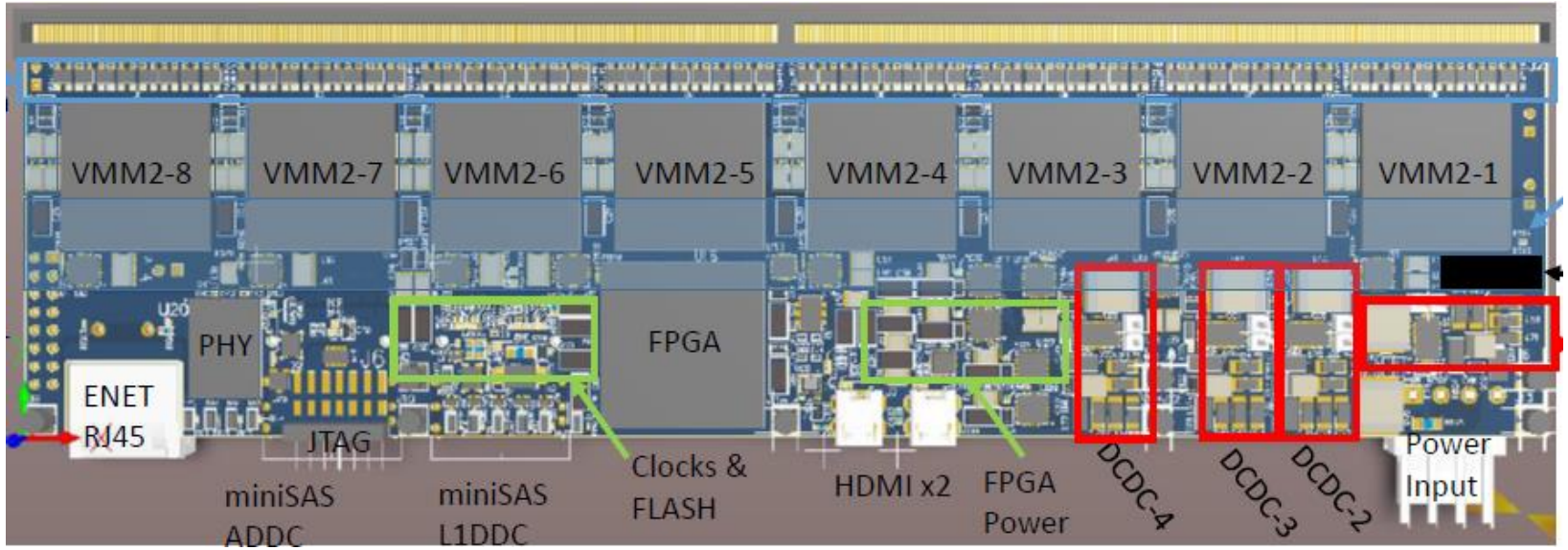
CyMBaL tracker readout: 64-channel ASIC and 512-channel FEB

- Assume integration of 8 64-channel VMM3a or next generation 50 MSPS chips
- System with 66K channels
  - → 1 056 ASICs
  - → 132 FEBs
  - → With a backend link per FEB: 5 32-link Felix equivalents
- Assume 10 kHz channel occupancy, total data bandwidth produced by frontends
  - → Signal shape readout: ~250 Gbit/s
  - → Time-amplitude readout: ~30 Gbit/s

Illustration: Atlas FEM8 prototype with 8 VMM3a: 215 x ~60

8 VMM3a size chips can fit to
220 mm long FEB
Compatible with example on page 4

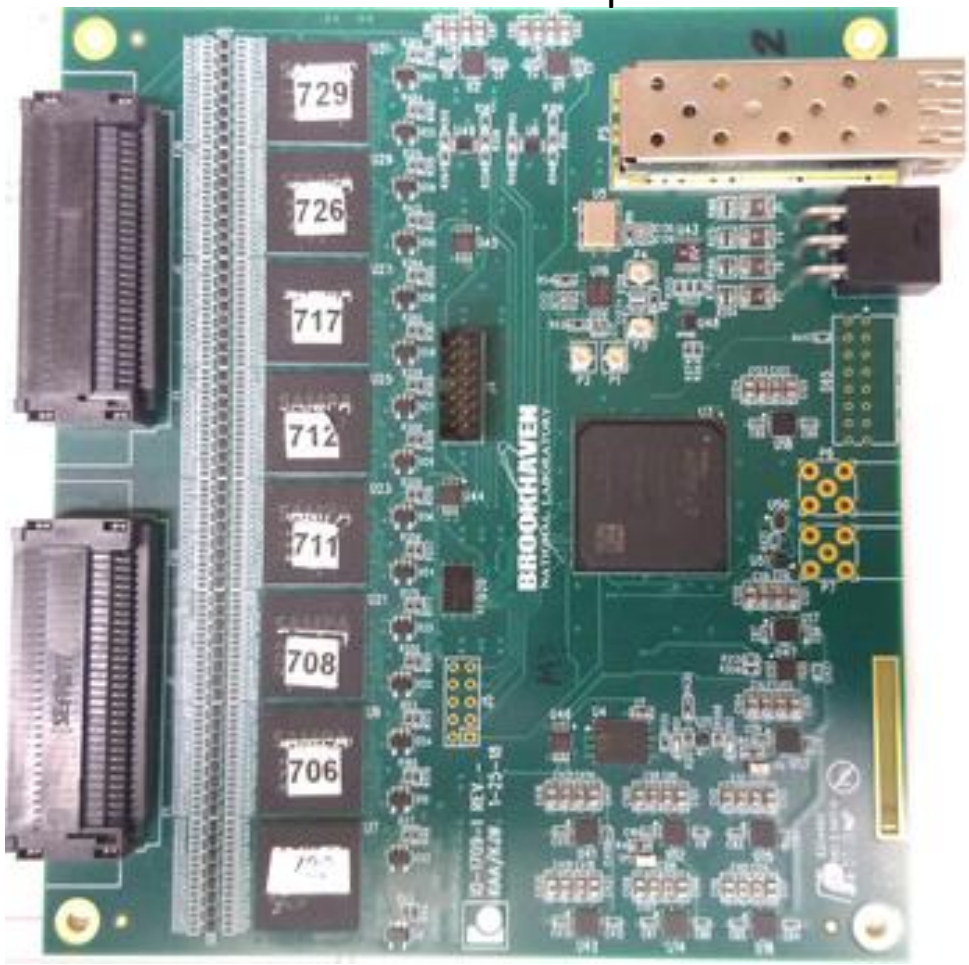
Assuming 8 double-row connectors:
0.8 mm pitch



CyMBaL tracker readout: 32-channel ASIC and 256-channel FEB

- Assume integration of 8 32-channel Sampa or next generation 50 MSPS chips
- System with 66K channels
  - → 2 112 ASICs
  - → 264 FEBs
  - → With a backend link per FEB: 9 32-link Felix equivalents
- Assume 10 kHz channel occupancy,
  total data bandwidth produced by frontends
  - → Sampa @ 20 MSPS: ~100 Gbit/s
  - → New ASIC @ 50 MSPS: ~250 Gbit/s

Illustration:
sPhenix TPC FEE with 8 Sampas: 140 x 140



8 Sampa size chips can fit to 150 mm long FEB
(Max size allowed to fit all 264 FEBs on tracker periphery)

Assuming the use of 8 double-row connectors: 0.8 mm pitch

CyMBaL tracker costing

- Assume 66K-channel system
- Assume 64-channel detector cables, 64-channel ASIC and 512-channel FEB
  → A FE-BE link per FEB
  → Cooling is not taken into account

Item	Quantity	Unit price $	Total price k$
Short FE cables	816	50	40.8
Long FE cables	240	100	24
ASIC	1 056	50	58.8
FEB	132	1 000	132
FE-BE link	132	100	13.2
Backend	6	7 000	42
BE servers	6	7 000	42
LV	1	7 000	7

- Total: $355k: $5.5/channel
  → Very rough estimation, expect more $8/channel
  → More likely $10/channel if 32-channel cables, 32-channel ASICs and 256-channel FEBs

Open questions on common services

- The frontend – backend communication links
  - → If lpGBT is considered, it has to be associated with an optical transceiver
    - VTRX+ with one 2.5 Gbit/s down-link and four 10 (5) Gbit/s up-links
      - Part of the Versatile Link+ elaborated by CERN
    - Will the Versatile Link+ from CERN available for EIC?
      - lpGBT and VTRX+ devices, and very importantly support
    - Is the use of VTRX+ justified?
      - Bandwidth, radiation
  - → Can a commercial optical transceiver be used with lpGBT?
    - Protocol and radiation
      - Atlas RPC collaboration considers replacement of VTRX+ by a commercial SFP+ optical transceiver
        - → A possible candidate: Avago AFBR-709SMZ Compatible Module SFP+ 10GBASE-SR 850nm 300m DOM LC MMF from FS
          - 10 Gbit/s with FEC5
- Radiation levels need to be understood
  - → TID, neutrons and SEE (latch-up, SEU)
  - → At what extent commercial components can be used
- Magnetic field
  - → Qualified power regulators

Will there be a central group(s) taking care of these questions?

Summary

- Not yet a complete knowledge of Micromegas cylindrical barrel tracker environment
  - → Construction, occupancy, space, radiation
  - → Figures below to be taken with caution
- Assuming 66K channel tracker as a baseline
  - → @ 10 kHz channel hit rate front-end link bandwidth – at least factor 5 above expected rates from physics
    - Signal shape readout at 50 MSPS: ~250 Gbit/s
    - Time-amplitude readout: ~30 Gbit/s
    - Further data reduction could / must be done either in FEP (if any) or in the on-line filtering farm
- Assuming 64-channel MPGD ASIC and 512-channel FEB
  - → 1 056 ASICs
  - → 132 FEBs
  - → 6 Felix equivalents with 32-links
- Open questions on central support for
  - → Common FE-BE link
  - → FE aggregation – design of a common aggregator unit
  - → Precision clock distribution validation metrics
  - → Magnetic field and radiation compatible components