

ATHENA DAQ

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1. The ATHENA Detector (22 + 2 pages)

1.1 DAQ and readout electronics (1 page)

The EIC collider will provide ep and eA collisions at rates up to 500 kHz with potential collisions occurring in bunches separated by 10 ns. ATHENA will digitize hit position, charge and timing signals originating from nearly 30 distinct sub-detectors using a variety of front end technologies including Silicon Photo Multipliers (SiPMs), Monolithic Active Pixel Sensors (MAPS), DC- and AC-coupled Low Gas Avalanche Detectors (DC-LGADs and AC-LGADs), Large Area Pico-Second Photon Detectors (LAPPDs), photomultiplier tubes (PMTs), and MPPGD technologies such as Micromegas and Gas Electron Multipliers (GEMs). The signals will be zero-suppressed, digitized and aggregated using front end boards containing a variety of ASICs and FPGAs, each of which will require power, cooling, configuration and clock signals. The primary function of the DAQ system will be to aggregate data and record all collision related hits. The system must also control, configure and monitor the acquisition of data and ensure data quality.

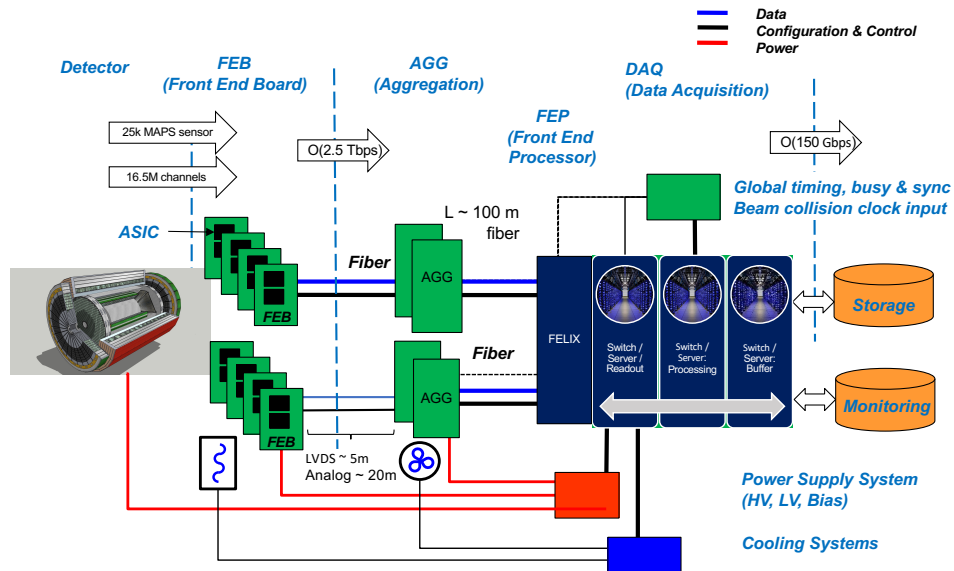


Figure 1.1: Overview of the ATHENA DAQ architecture.

The chosen architecture is illustrated in Fig. 1.1 and will be a streaming DAQ system following the scheme outlined in the Yellow Report. A global timing system is needed to synchronize the system with the bunch structure of the EIC. Front End Link eXchange (FELIX) boards are used as a basis to provide common interface between the Front End Boards (FEBs) and the commodity DAQ computers. These boards are capable of transferring data to the DAQ computers and of transmitting clock and configuration information to the FEBs. A farm of approximately 40 computers on a 100 Gbps Ethernet network is needed to read out the FELIX boards, reduce the noise and send the data to long term storage. An additional farm of 30 computers with 3000 CPU cores could do reconstruction of events for quality assurance and as a first pass of data analysis.

The ATHENA DAQ should write out all collisions provided by the collider to the detector at rates up to 500kHz. The global timing will be synchronised to the bunch timing with a resolution of

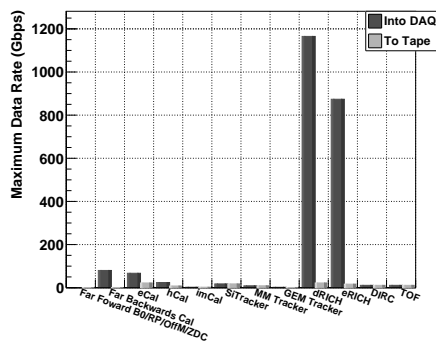


Figure 1.2: Maximum data volume by detector.

10 ns. The maximum data volume by detector is shown in Fig. 1.2. This illustrates that the digital data transmitted by the FEBs could have data volumes as high as 21 Tbps. This data volume will need to be reduced to a level of 100 Gbps for long term storage without losing detector hits that arise from beam collisions.

The biggest challenge to the goal of fully reading out the ATHENA detector with no deadtime will be the dark currents from the SiPM readout as high as 3 kHz per pixel. This dark current is indistinguishable from signals from single photons. We hope to reduce this by an order of magnitude in the FEBs by applying timing cuts relative bunch crossing time. It may be possible to further reduce this volume using machine learning techniques in the FPGAs of the FELIX boards. In the DAQ computers it will be possible to apply a software trigger to these detectors. Requiring a collision to be present will provide a data reduction of at least 200, allowing the ATHENA DAQ to readout all collision data to tape.

The largest potential risk of the system is unexpectedly high noise in any detector, or the inability to reduce the noise in the SiPM detectors with single photon thresholds. One factor mitigating this risk is that the architecture of the system does not eliminate the possibility of providing hardware trigger signals to specific detectors resulting in a hybrid triggered-streaming DAQ system. The potential avenues of data volume reduction at each stage will be the main R&D required. There will be significant development required to integrate each detector with the FELIX board.