AC-LGAD based - Timing Tracking Layer (TTL)

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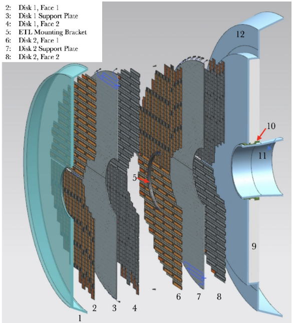
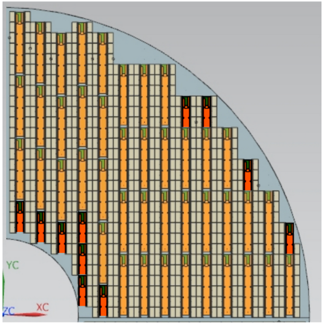
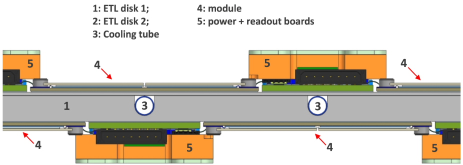
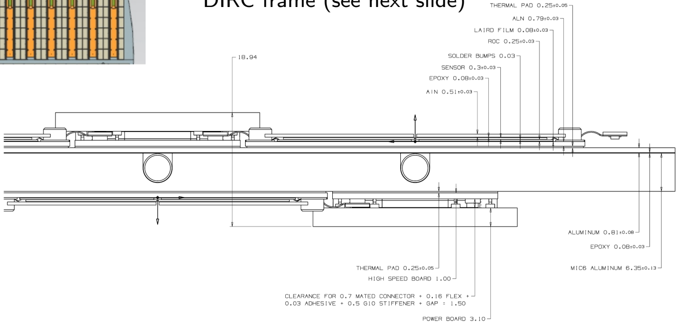
Basic design update principles





- Design based on the CMS forward upgrade [link]
- Basic elements: ladders of 3 or 6 LGAD sensors with service hybrid (for readout and power)
- Sensors mounted on aluminum plate (currently 6mm thick) and contains cooling
- Sensors on back side of plate shifted to cover service hybrid dead area (see bottom figure)
- Barrel layer to be mounted on inner or outer part of DIRC frame (see next slide)

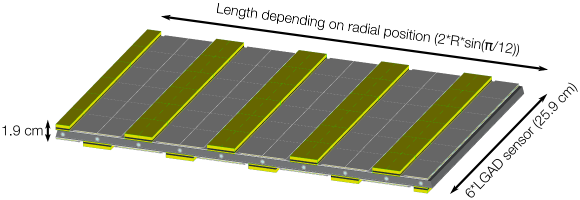


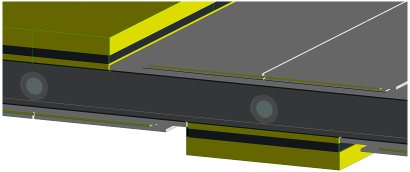


New Layers in Geant4

fun4all_eicdetectors/simulation/g4simulation/g4ttl

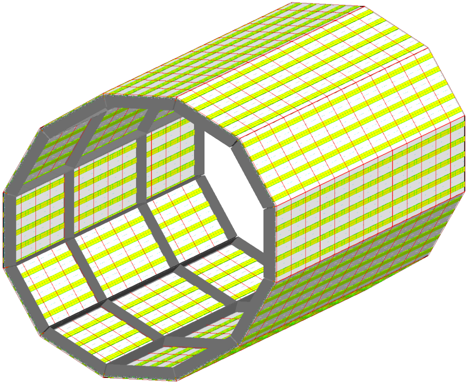
- LGAD sensors ($21 \times 42\text{mm}^2$) mounted on readout chips ($21 \times 21\text{mm}^2$) on top of Aluminum Nitride substrate for thermal conduction to aluminum plate
- Al plate in total 7.16mm thick and contains 5mm diam. cooling tubes
- Service hybrids (big yellow boxes) made of various materials, dominated by the power boards
- Sensors placed on both sides of plate for full coverage (total thickness $\sim$ 1.9 cm)
- Each barrel module is 6 LGAD sensors long and width depends on radial position

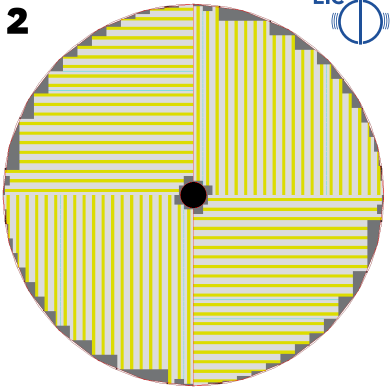


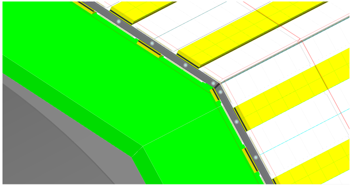


New Layers in Geant4 - 2

- Barrel made of 12 modules in azimuth and multiple modules along z-axis
  $\rightarrow$ implemented additional temporary support structure based on DIRC frame principles (support $\sim$7 cm high and 6mm thick)
- Forward layers mounted on identical 1/4 disk slices ($\rightarrow$ 4 modules) which are rotated by 90 degrees (see image)

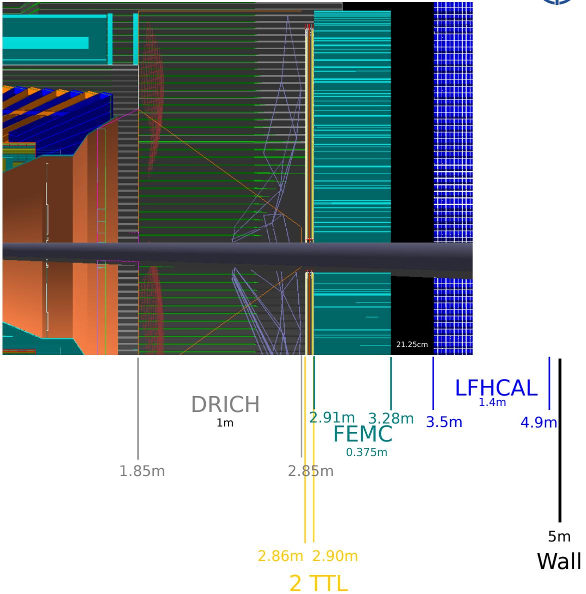






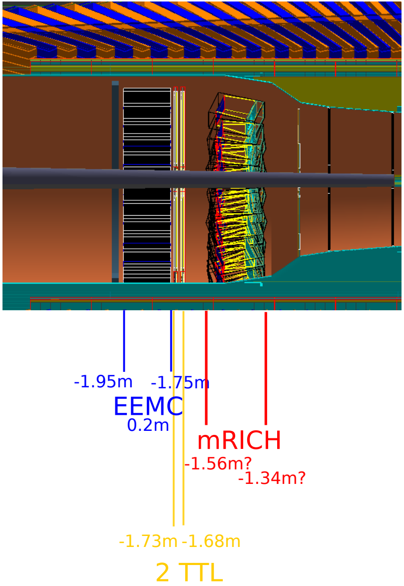
Current Positions: forward

- FEMC & LFHCAL activ depth 0.375 and 1.4m starting at 2.91m need at least $\approx$ 25cm for read-out
  $\rightarrow$ ideally not to be reduce, barely containing shower as is at high energies
- Current TTL in simulations 1.8cm deep $\Rightarrow$ 2 layer $\approx 4-5$cm
- DRICH starting at 1.85m forseen to be 1m deep, ideally wants 10cm more
  $\rightarrow$ seeing deteriorated performance with 1m
- DRICH can't move further in due to BECAL and electron coverage in calo's



Space is a commodity!

Current Positions: backward



- EEMC starts at -1.75m, optimized in junction with barrel ECal & services for maximum coverage for scattered electron
- mRICH ends at ≈ -1.56m, however they'd like to move further out to increase overage (currently 80%)
- TTL (2 layers) currently starts at -1.68m and is again 1.8cm per layer
- At most 19cm for alternative TOF+μRwell ideally full coverage
  → not as tight as in forward direction, BUT not spacious either

Space is a commodity!

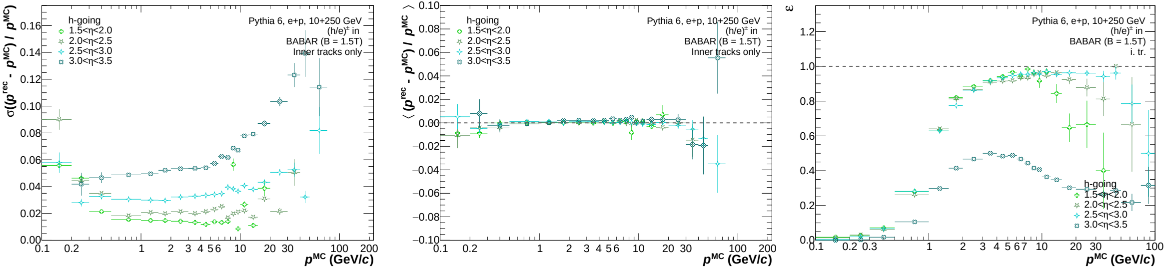
Current Cost estimate for AC-LGAD

- R&D (common for both end-caps & Roman Pods): $\sim$ **1 Mio** (accounted in eRD112), mainly labor
- Prototyping: $\sim$ **1.3 Mio**, mainly labor
- Final design: $\sim$ **1 Mio**, mainly labor
- Procurement:
  forward: **8.4 Mio** per layer ($\sim 9.5 m^2$)
  backward: **0.8 Mio** per layer ($\sim 1.15 m^2$)
- Assembly (2 forward, 2 backward layers): $\sim$ **1.8 Mio**, mainly labor

total 2 layers fwd/back: $\sim$ **20 Mio**
total 1 layers fwd/back: $\sim$ **11.7 Mio**

Performance

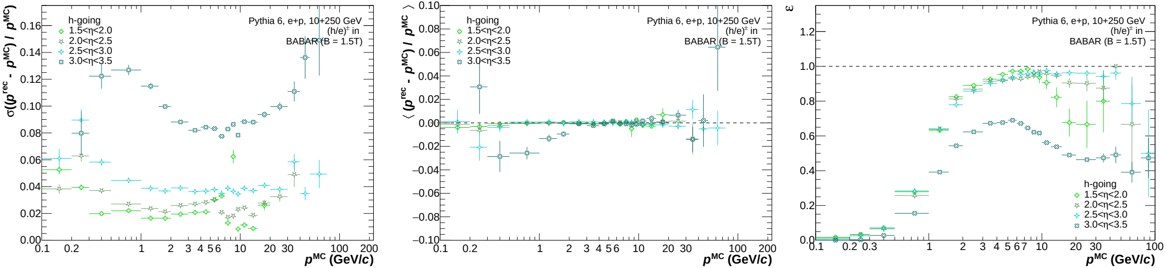
Tracking performance w/o TTL



- Very idealized tracking algorithm
  $\rightarrow$ relies on GEANT hits instead of reconstructed clusters
- Severe deterioration of tracking efficiency above $\eta > 2.5$
  no tracks beyond $\eta = 3.4$ for setup w/o TTL
- Momentum resolution deteriorates for $\eta > 2.5$

ECCE default w/o TTL

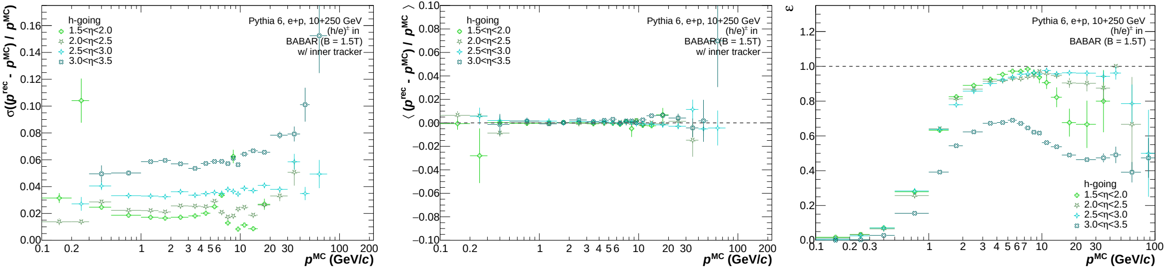
Tracking performance



- inclusion of TTL layers helps increase efficiency
- resolution seems to be deteriorated
  HOWEVER: not a fair comparison tracks with 2 layers in TTL + 1 inner tracker hit have much less resolution
- if track found resolution improves as expected

ECCE default 2 TTL layers fwd

Tracking performance



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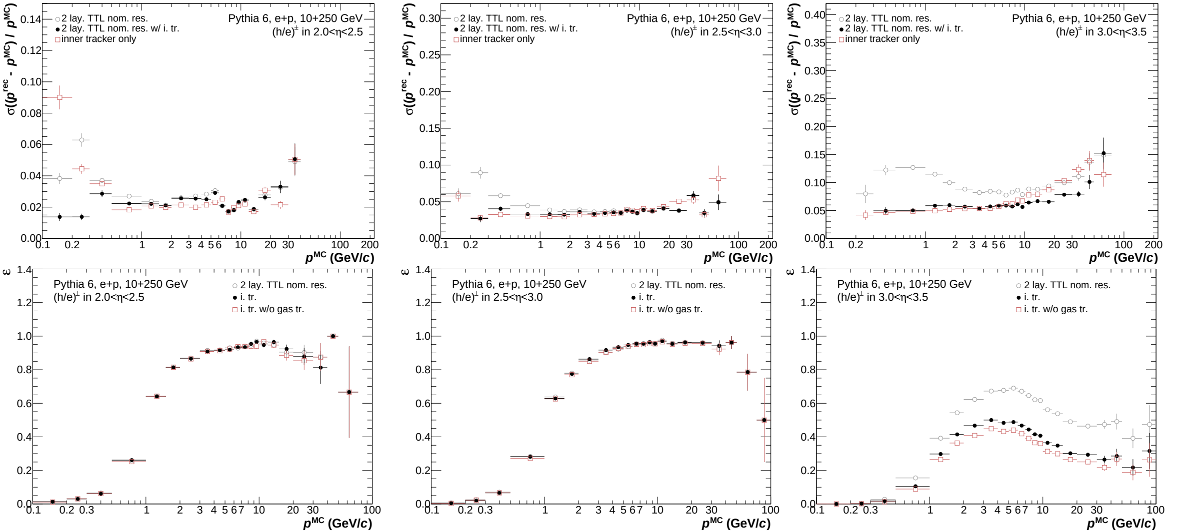
ECCE default 2 TTL layers fwd
track found in inner tracker too

Tracking performance: impact of 2 TTL

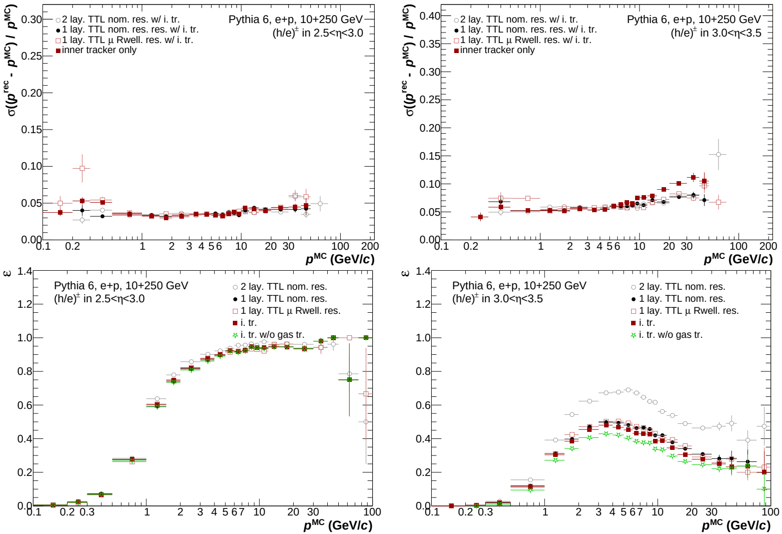


CAVEAT: This is all with close to ideal tracking! It will be worse in reality!

Tracking studies

- Only simulation for TTL available (centrally)
- Need to study impact of
  a) Reducing number of layer to 1
  b) Reducing number of layer to 1 asumming TOF will be mRPC & μRwell is installed upfront
- a) is simple for b) take 1 TTL layer with worse position resolution (55μm) as proxy

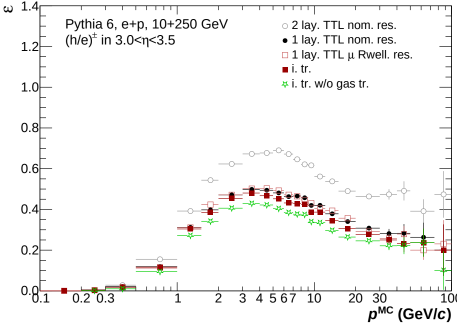
Tracking performance: impact of n TTL

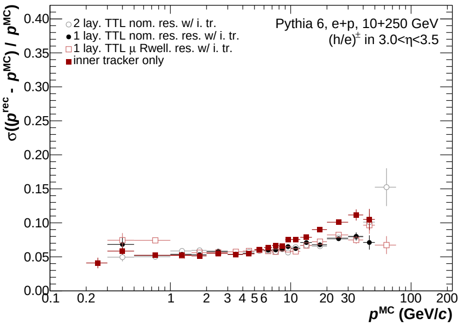


- inclusion of TTL layers helps increase efficiency by factor 2 for high η
- resolution between 1,2 TTL or μRwell at same position identical if inner track is reconstructed

CAVEAT: This is all with close to ideal tracking! It will be worse in reality!

Tracking performance: Why 2 layers?





- Advantage of 2 layers would be reduced fakes, due to posibility to build tracklets
  $\Rightarrow$ nearly impossible to show with existing simulation and tracking
  $\Rightarrow$ would also allow better position matching between clusters and tracks
- **maybe 1 layer to 1.7m and a 2nd to $\approx$ 0.6m best of both worlds**
  total cost: $\sim$ **11.7 Mio forward + 0.8 Mio backward**

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