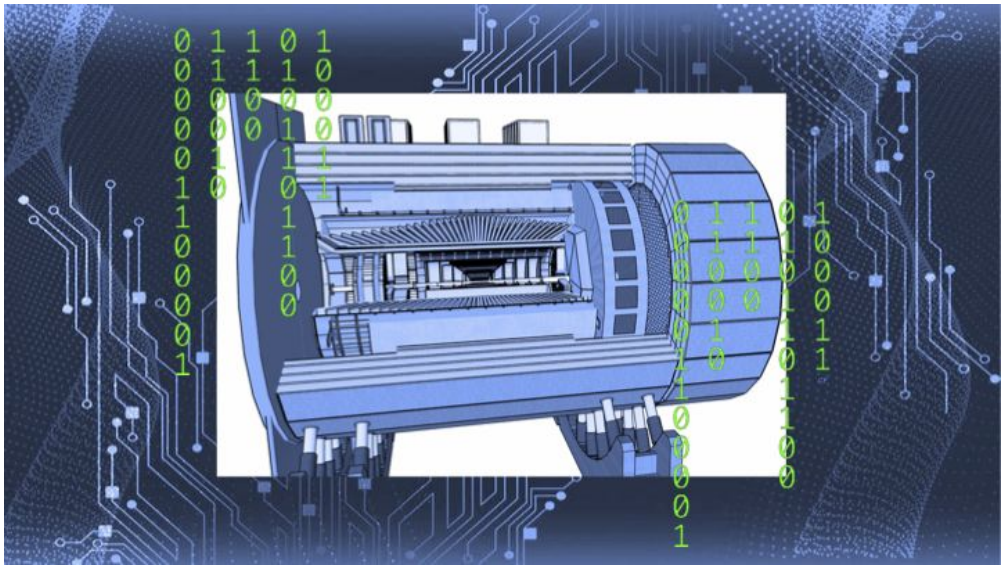
EIC Comprehensive Chromodynamics Experiment



Electronics, DAQ, and Computing

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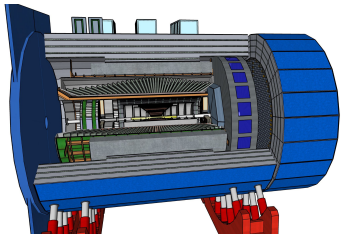
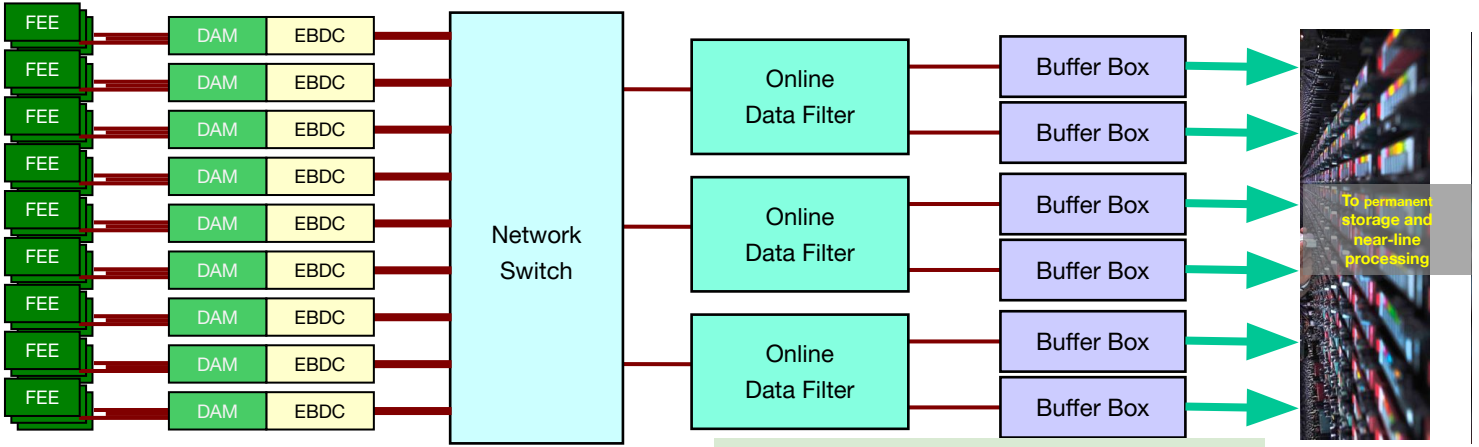
DAQ: Overview

- **ECCE proposal calls for a Streaming Data Acquisition System (SRO)**
  - Widely recommended by experts: EIC Computing Consortium, EIC Yellow Report
  - No need to wait for all signals from single crossing to read out data
  - Removes nearly all deadtime
  - Less restrictions for filter criteria and potentially less bias





FEE = Front End Electronics
DAM = Data Aggregation Module
EBDC = Event Buffer / Data Compressor

Front End Electronics

- **Requirement**: Digitize analog signals with appropriate dynamic range
- ★ ***Solution**: Mixture of ASICs and COTS modules that individually address specific needs of each detector*
  - *Nalu SoC, MAROC - PID detectors*
  - *AC-LGAD development (based on CMS eTROC) - TOF (high-res)*
  - *ATLAS ALTIROC - Far forward, Roman pots, etc.*

- **Requirement**: Does not require external triggering
- ★ ***Solution**: All FEE modules implement continuous sampling modes*

- **Requirement**: Preserve high resolution capability of calorimeters
- ★ ***Solution**: Implement common waveform digitizer design for all calorimetry*

- **Requirement**: Zero suppression + Feature extraction
- ★ ***Solution**: All FEE modules implement zero suppression. SAMPA, HDSoC, etc. have integrated DSPs for feature extraction. DAM boards also capable of feature extraction.*

- **Requirement**: Interface with DAM
- ★ ***Solution**: All FEE modules optical link compatible with FELIX*

See DAQ/Electronics ecce note for more details:
https://www.ecce-eic.org/ecce-internal-notes (PW: ECCEprop)

ASIC = Application Specific Integrated Circuit
COTS = Commercial Off The Shelf
DAM = Data Aggregation Module

PID Detector ASICs and Channel Counts

ASIC development done at community level
(not ECCE specific)

PID WBS Name	Detector	ASIC	Channels
Barrel PID	hpDIRC	High Density SoC	69,632
	TOF	eRD112 development	8,600,000
Electron Endcap	mRICH	High Density SoC	65,536
	TOF	eRD112 development	920,000
Hadron Endcap	dRICH	MAROC3	5,376
	TOF	eRD112 development	1,840,000
Far-Forward Detectors	Roman Pots	eRD112 development	524,288
	B0 Detector	eRD112 development	2.6M
	Off-Momentum Detectors	eRD112 development	1.8M
Far-Backward Detectors	Low-Q^2 Tagger	eRD112 development	4.6M
	Luminosity Monitor	eRD112 development	268,441

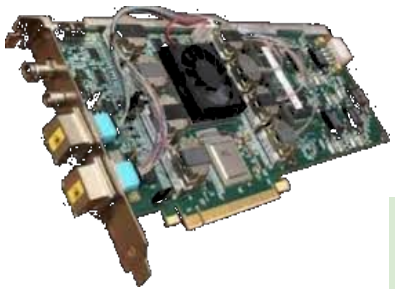
SoC= System on a Chip

eRD112 = project for targeted EIC detector R&D

DAM Boards

Detector system	DAM boards	Channel/Fiber Count
Barrel		
Si Tracker	4	100 fibers
uRWell	12	278,000 channels, 576 fibers
AC-LGAD TOF	30	1400 fibers
hpDIRC	5	200 fibers
BECAL	2	9,088 channels , 72 fibers
iHCAL + oHCAL	1	3,264 channels, 26 fibers
Forward		
AC-LGAD TOF	6	300 fibers
dRICH	5	220 fibers
FEMC	8	47,850 channels, 375 fibers
LFHCAL	10	58,590 channels, 460 fibers
Backwards		
mRICH	7	288 fibers
AC-LGAD TOF	3	150 fibers
EEMC	1	2878 channels, 24 fibers
Far-Forward		
B0 Detector, Roman Pots, Off-Momentum Detectors, ZDC	26	7.4M
Far-Backward		
Luminosity Monitor & Low-Q^2 Tagger	18	4.9M
Sum	**138**	

- Transition data to COTS Computing
- Built-in FPGA provides processing/Data aggregation



ATLAS FELIX board is an example of a DAM board

COTS = Commercial Off The Shelf
DAM = Data Aggregation Module

DAQ: Timing System

- Each beam crossing identified with unique 64-bit value
- Communicated to DAM boards which distribute to FEE
  - Data transferred at multiple of accelerator clock (e.g. x6)
    - 16bits per transfer *(16x6 = 96bits/crossing)*
  - Additional data embedded across transfers
    - "mode" bits can indicate different actions to FEE
  - Crossing number used to stamp all data from front end
    - Specifics of timing will be detector dependent
  - System modeled after working sPHENIX system

FEE = Front End Electronics
DAM = Data Aggregation Module

sPHENIX Prototype Timing Board

sPHENIX ZCU102 Timing module

Computing: Online to Offline Stream

FEE = Front End Electronics
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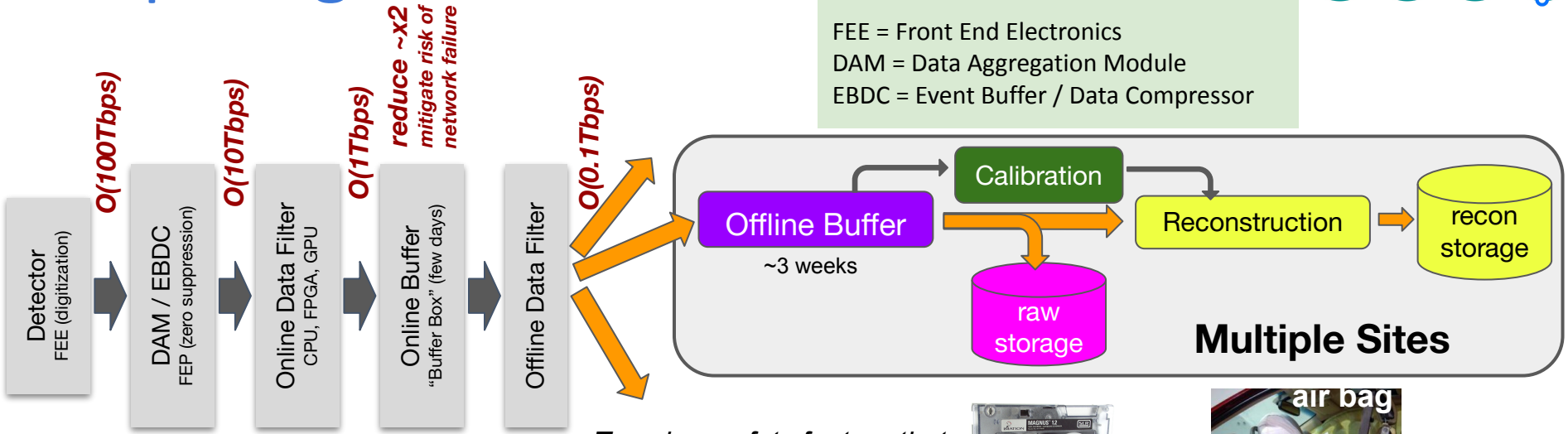
EBDC = Event Buffer / Data Compressor



Tape is a safety feature that you hope to never use!

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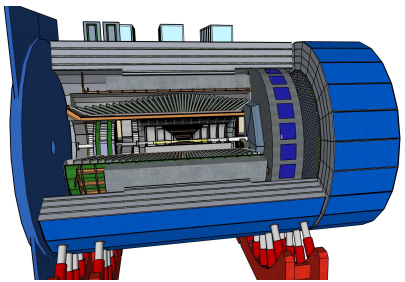
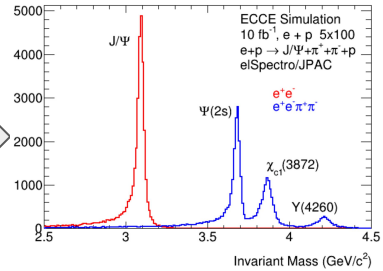
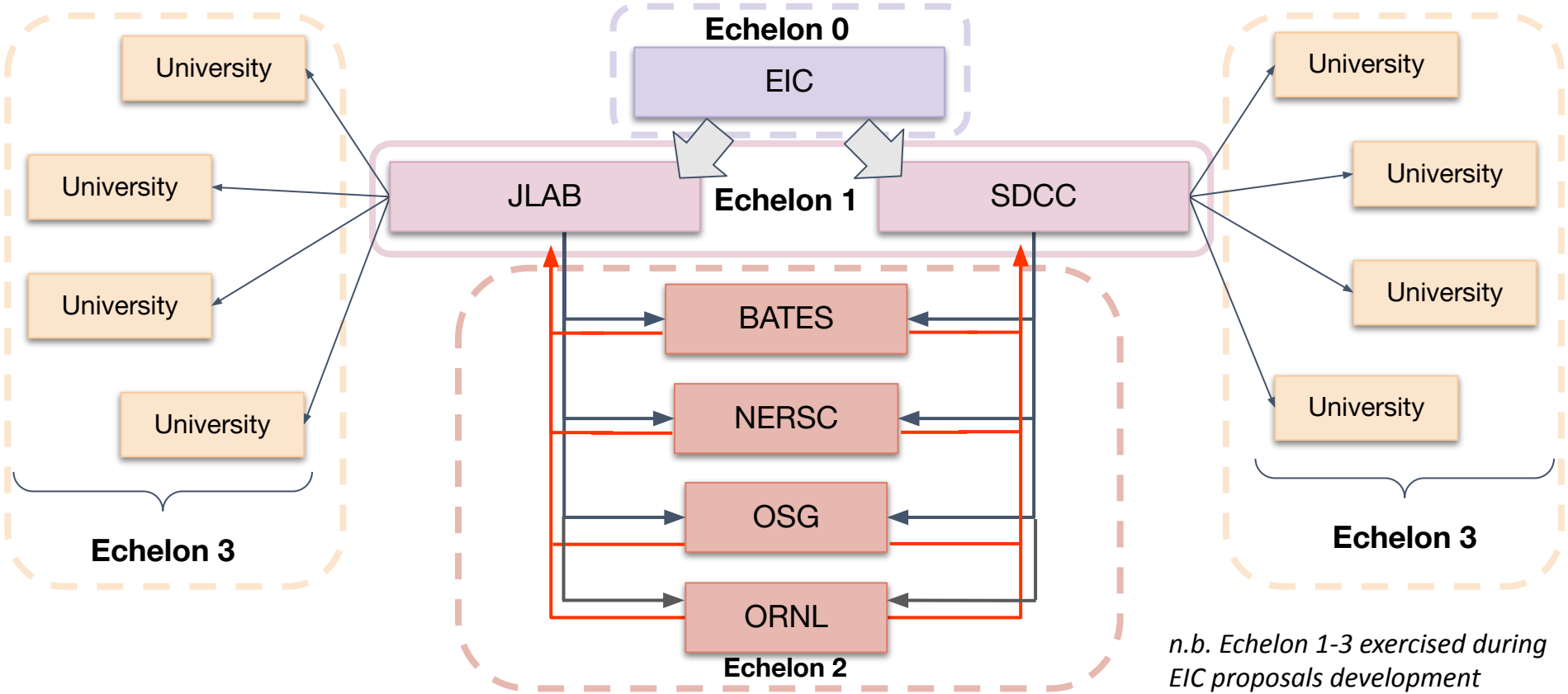


DAQ, BUFFERING, FILTERING, CALIBRATION, RECONSTRUCTION, ANALYSIS



Computing: Butterfly Model

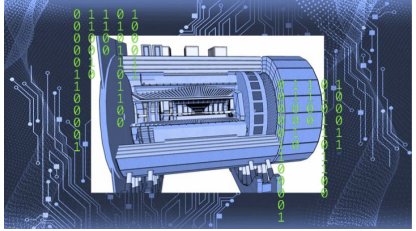


n.b. Echelon 1-3 exercised during EIC proposals development

Raw Data Requirements *(estimated)*

ECCE Runs	year-1	year-2	year-3
Luminosity	$10^{33}\text{cm}^{-2}\text{s}^{-1}$	$2 \times 10^{33}\text{cm}^{-2}\text{s}^{-1}$	$10^{34}\text{cm}^{-2}\text{s}^{-1}$
Weeks of Running	10	20	30
Operational efficiency	40%	50%	60%
Disk (temporary)	1.2PB	3.0PB	18.1PB
Disk (permanent)	0.4PB	2.4PB	20.6PB
Data Rate to Storage	6.7Gbps	16.7Gbps	100Gbps
Raw Data Storage (no duplicates)	4PB	20PB	181PB
Recon process time/core	5.4s/ev	5.4s/ev	5.4s/ev
Streaming-unpacked event size	33kB	33kB	33kB
Number of events produced	121 billion	605 billion	5,443 billion
Recon Storage	0.4PB	2PB	18PB
CPU-core hours (recon+calib)	191Mcore-hrs	953Mcore-hrs	8,573Mcore-hrs
2020-cores needed to process in 30 weeks	38k	189k	1,701k

Summary



- Fully Streaming DAQ system
  - Experiment-wide, improves performance, reduces risk, cost effective
- Candidate Front End Electronics identified for each detector system
  - Leverage community and commercial solutions as much as possible
- Multiple stages of data aggregation and reduction
  - heterogeneous hardware solutions (FPGA, CPU, GPU, …)
- Federated Computing Model to decentralize computing
- Latency (e.g. ~3weeks) between acquisition and fully calibrated/aligned/reconstructed data ready for physics analysis

See DAQ/Electronics and Computing Plan documents for more details: https://www.ecce-eic.org/ecce-internal-notes
(PW: ECCEprop)

Backups

Computing: Online to Offline Stream