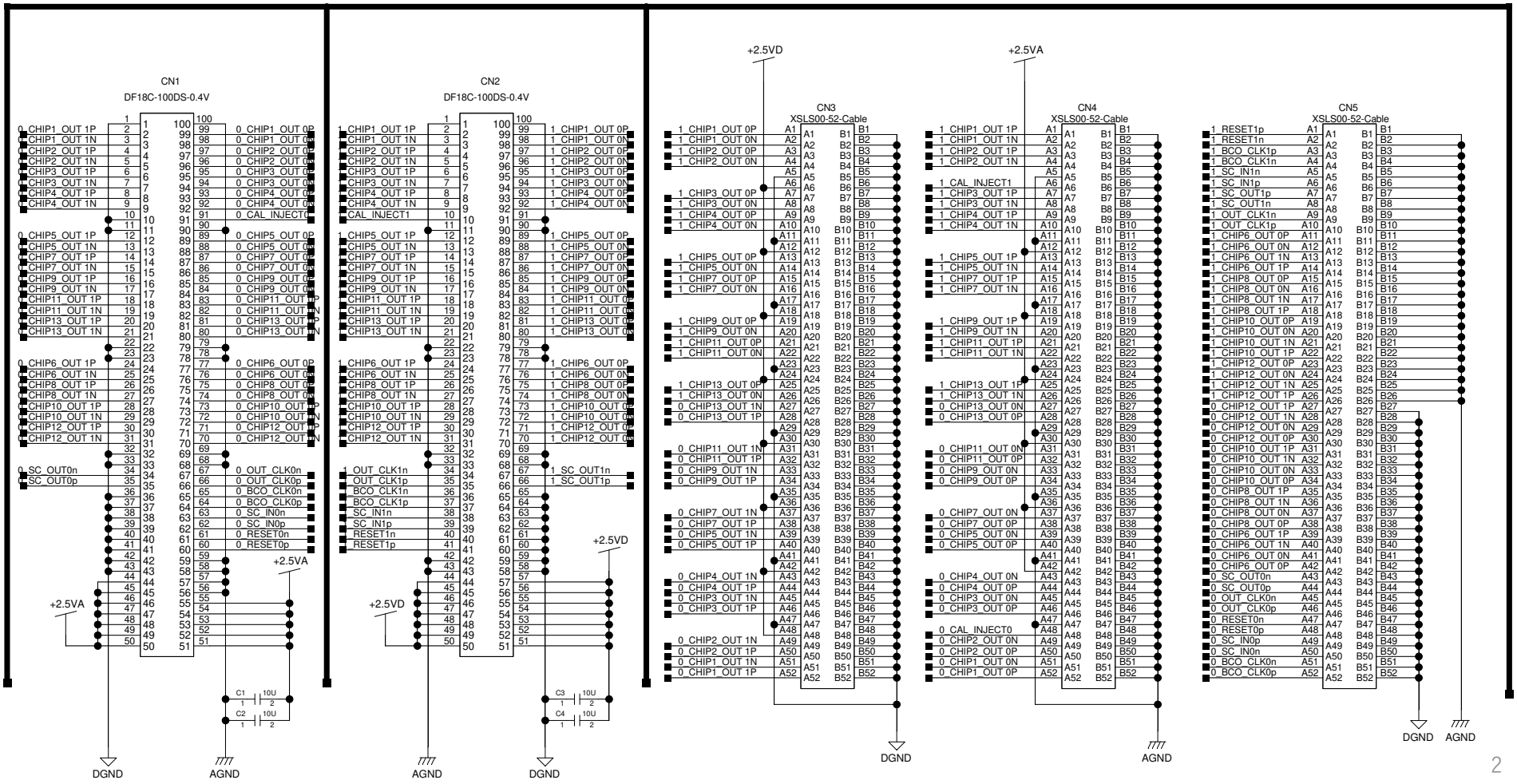
Conversion Cable Design

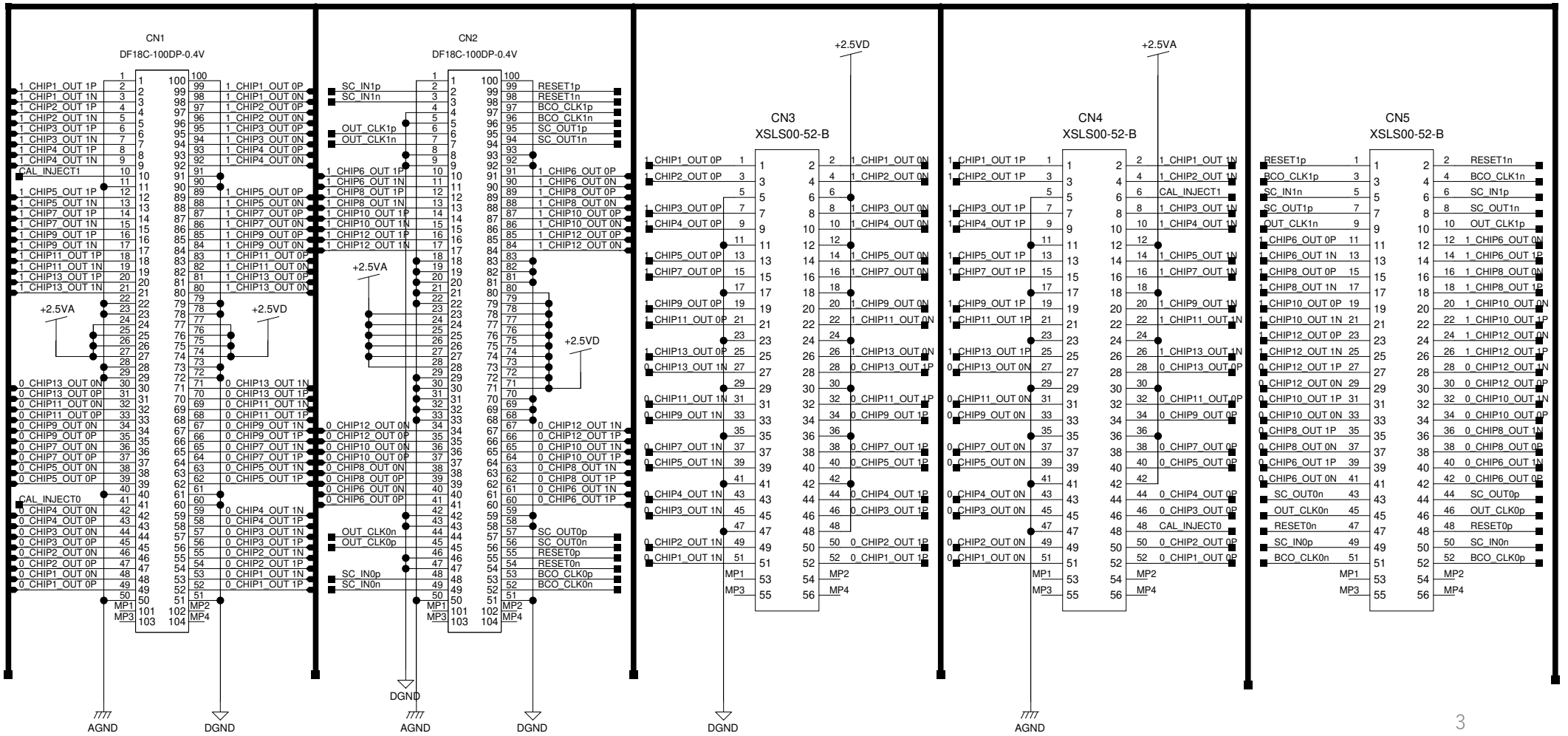
RIKEN/RBRC

Itaru Nakagawa

HDI Side


CN1
DF18C-100DS-0.4V
CN2
DF18C-100DS-0.4V
CN3
XSLS00-52-Cable
CN4
XSLS00-52-Cable
CN5
XSLS00-52-Cable
+2.5VD
+2.5VA
DGND
AGND
C1
C2
C3
C4
10U

ROC Side


CN1
DF18C-100DP-0.4V
CN2
DF18C-100DP-0.4V
CN3
XSLS00-52-B
CN4
XSLS00-52-B
CN5
XSLS00-52-B
+2.5VA
+2.5VD
AGND
DGND

HDI Side

- P/N pair of LVDS is in parallel configuration.

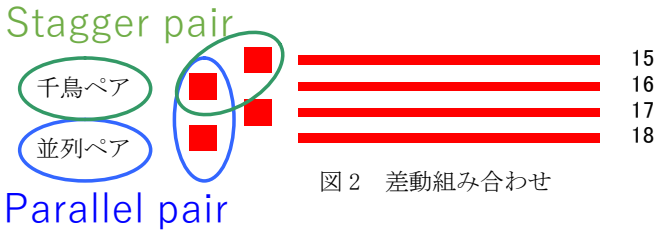
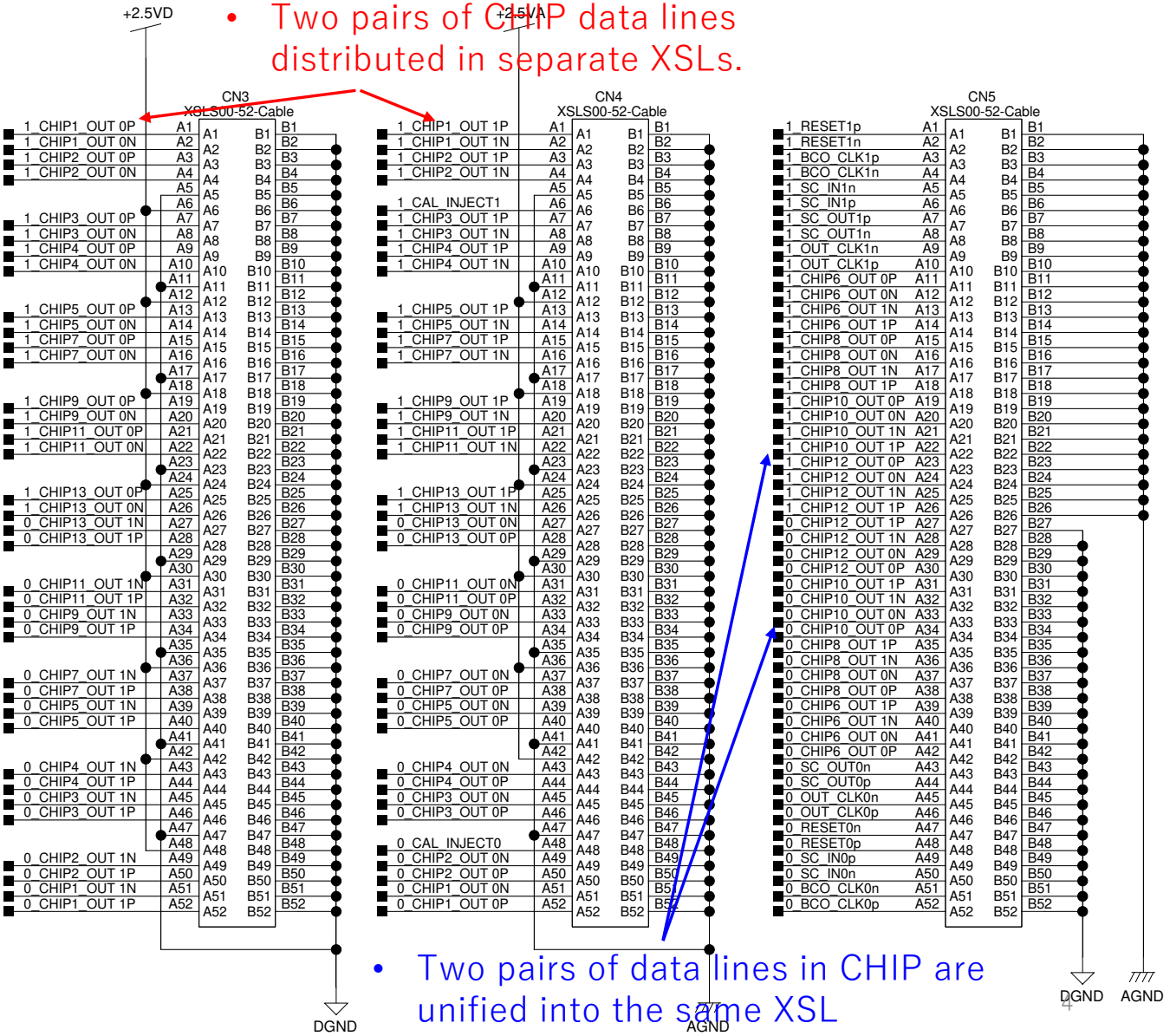


図 2　差動組み合わせ

Red：Good
Blue：Worrisome



- Two pairs of CHIP data lines distributed in separate XSLs.
- Two pairs of data lines in CHIP are unified into the same XSL

ROC Side

- The P/N pairs of LVDS are staggered pairs.
- Is it possible to secure the same length distribution line even with staggered pairs?

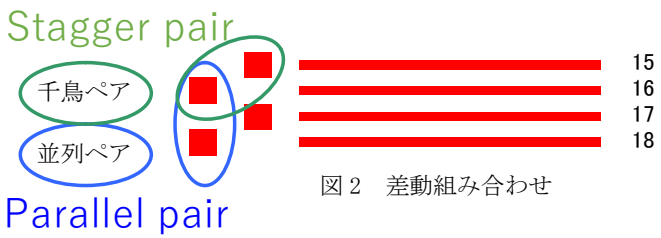
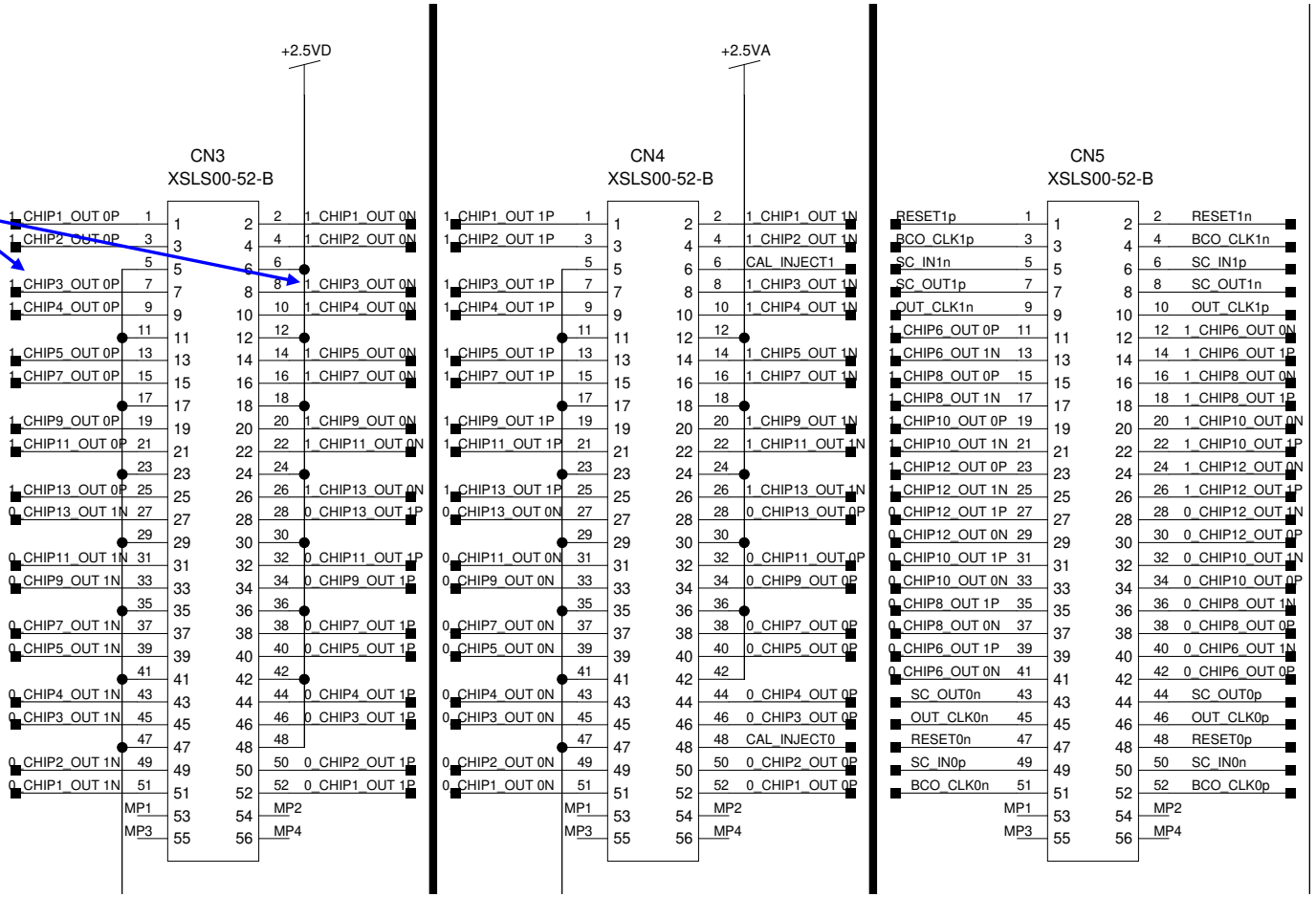


図２　差動組み合わせ



Staggered vs. Parallel Pairs

発 行
'21.08.16
ケル㈱

1/18
ES-0046
2008 年 5 月 9 日

ケル株式会社
第一技術部

承 認	照 査	作 成
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参考文献：KEL社の技術レポート
Reference : KEL co. technical report

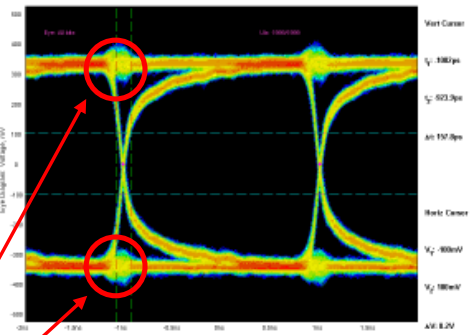
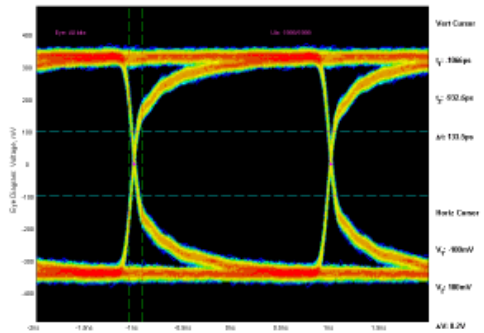
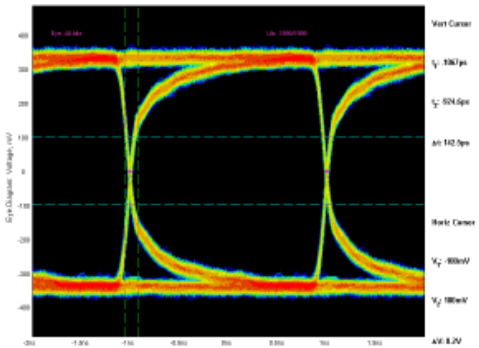
XSL 伝送特性(AWG46)

Staggered vs. Parallel Pairs

Our signal is 400Mbps which is comparable to KEL's following measurement, i.e. 500Mbps. I think the measurement is rather close to our usage environment.

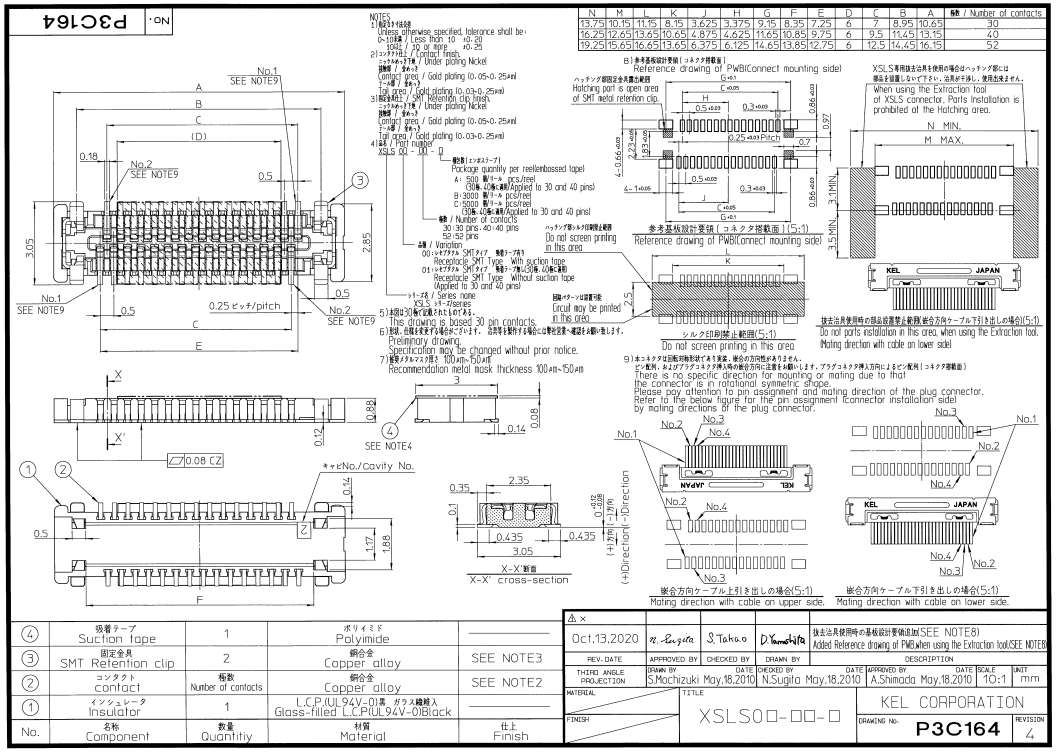
12/18
ES-0046

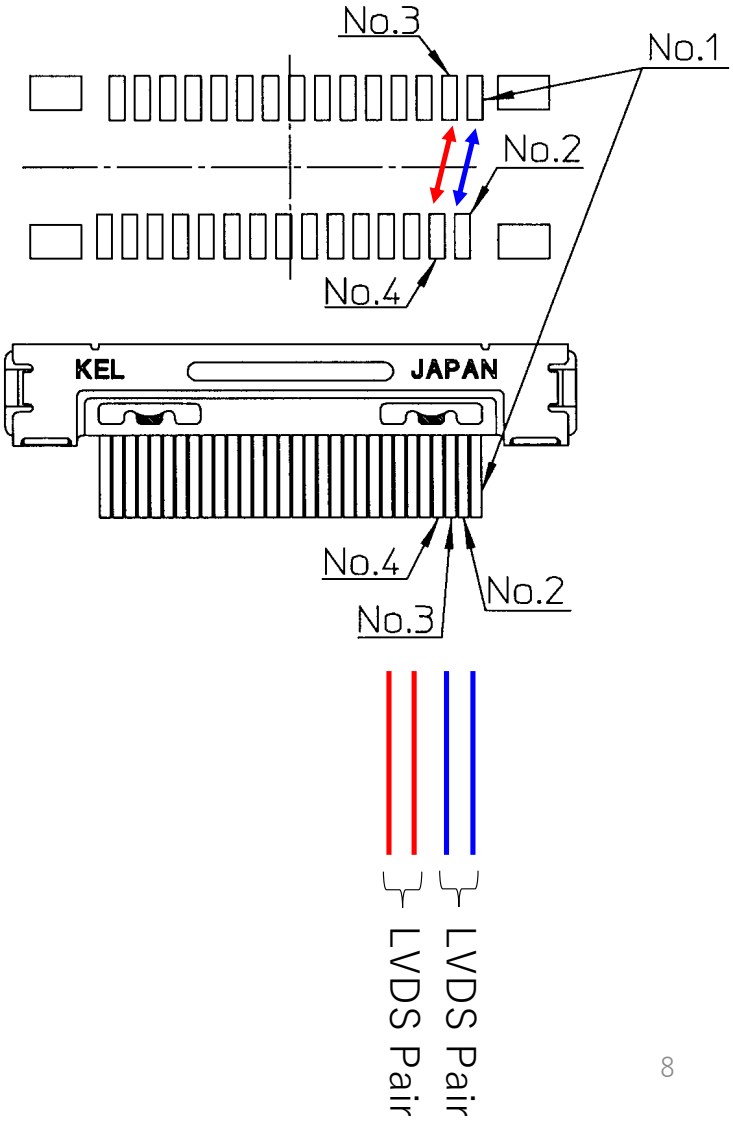
・±350mV

	千鳥ペア(18-19)	並列ペア(内側, 15-17)	並列ペア(外側, 16-18)
500Mbps			
	Jitter=7.9%（±100mV）	Jitter=6.7%（±100mV）	Jitter=7.1%（±100mV）

The staggered pair signal is rather distorted compared to parallel pair.

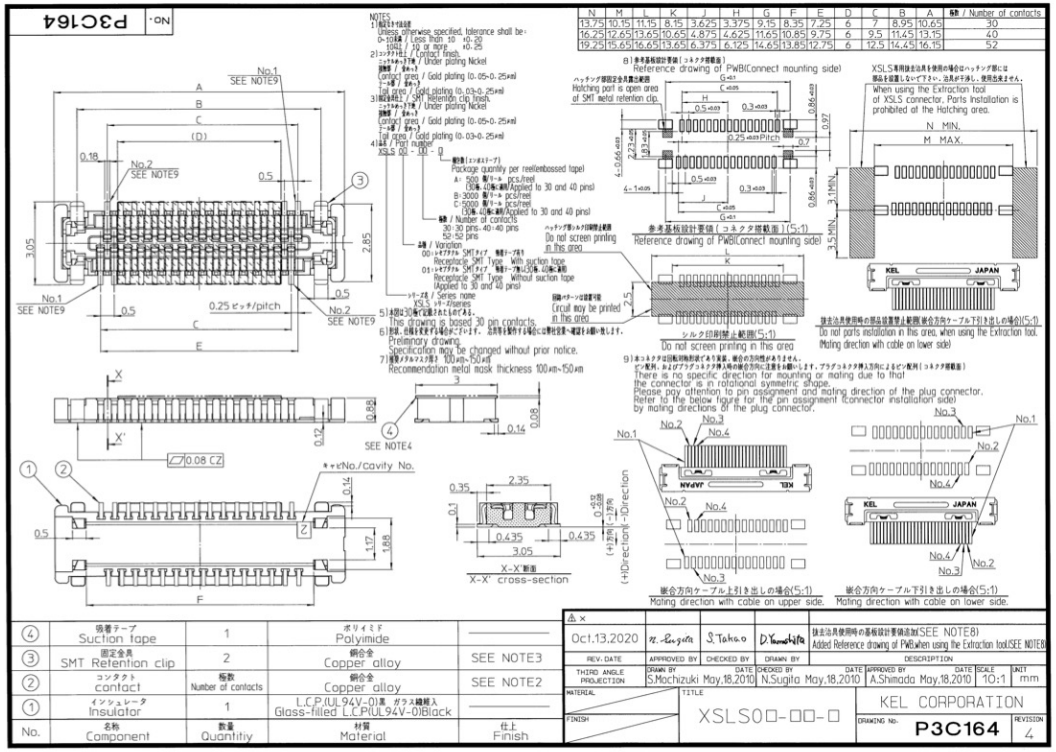
Solution?

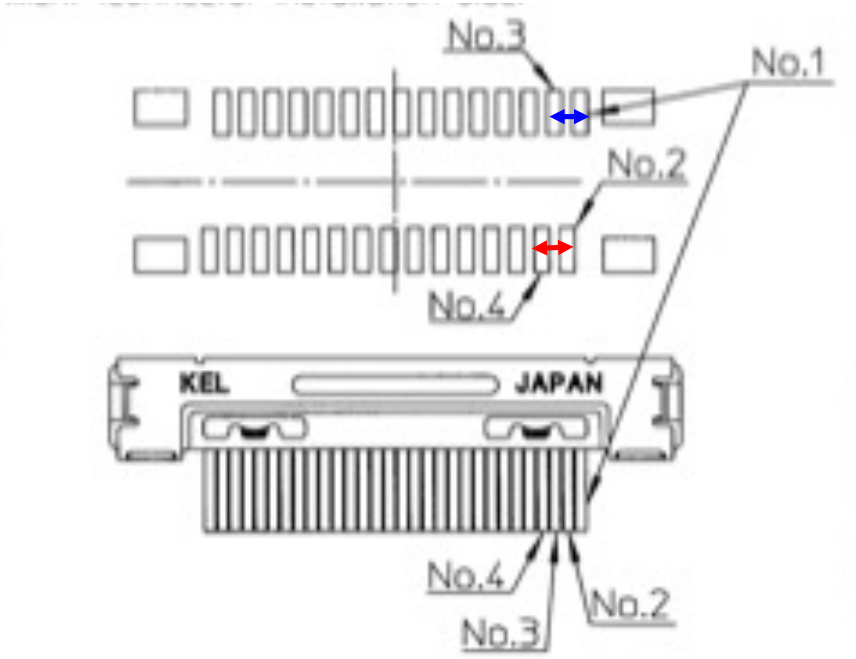


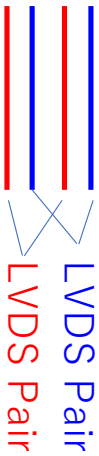


Since the LVDS pairs are running together right next to each other, they will end up with stagger combination at the pad end by design of the connector.

Solution?







Unless we twist between the adjacent LVDS pairs, the we cannot configure them as parallel pads layout, unfortunately.

Summary

- We'll let them proceed to fabricate the prototype as the present design.
- The design is posted on our wiki:

https://wiki.bnl.gov/sPHENIX/index.php/Conversion_Cable