UNIVERSITY OF BIRMINGHAM

Tracking and Vertexing based on Monolithic Active Pixel Sensors for the EIC

L. Gonella, University of Birmingham

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EIC detector tracking requirements

- Wide kinematic coverage.
- Good momentum resolution.
- High-precision primary vertex determination.
- Secondary vertex separation capability.

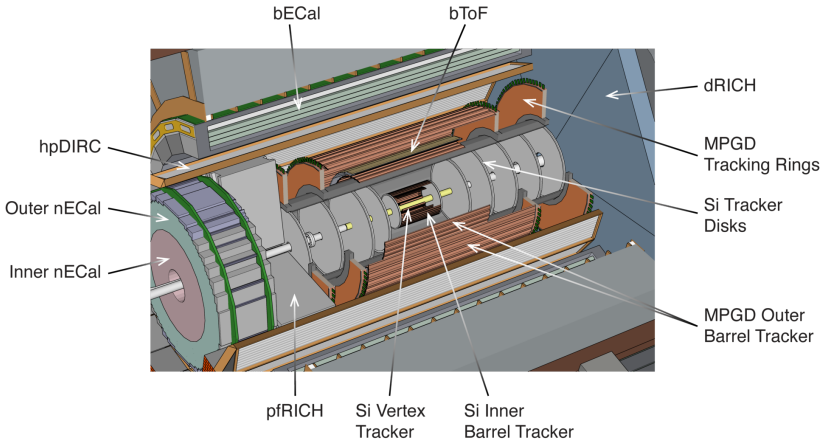
A well integrated, large acceptance vertex and tracking detector designed with high granularity and low material budget is needed to enable high precision measurements that are key to the EIC science programme.

EIC detector tracking concepts

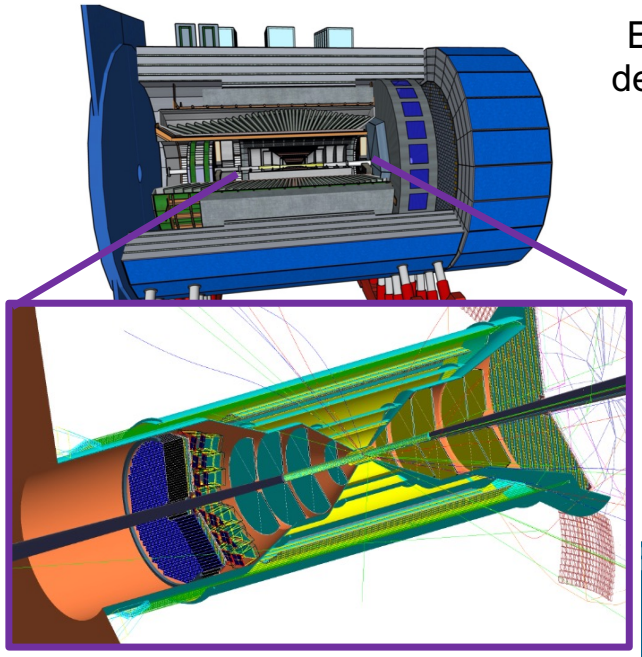
- The ATHENA, ECCE, CORE detector proposals are all equipped with a vertex and tracking detector as their innermost element.

- The tracking and vertexing systems under consideration are based on semiconductor detector technologies close to the interaction point.
  - 3 vertex layers, 2-3 intermediate layers, 4-6 silicon discs in the forward & backward regions.
  - In some case complemented by gaseous detectors at large radii.

ATHENA detector



ECCE detector



Silicon requirements for EIC

- Spatial resolution:
  - ≤ 5 μm for tracking layers & discs.
  - ~3 μm for vertex layers.
- Material budget:
  - ≤ 0.1% X_0 for vertex layers.
  - ≤ 0.8/0.3% X_0 for tracking layers/disk.
- Integration time: ≤ 2 μs.
- Power consumption: < 20 – 40 mW/cm^2.

Requirements driven technology choice:

Monolithic Active Pixel Sensors (MAPS).

MAPS for EIC

- MAPS are used in vertex detectors for STAR, ALICE, sPHENIX.
  - ALICE & sPHENIX use the ALPIDE chip developed for the ALICE ITS2 (180 nm CMOS imaging process).
  - ALPIDE doesn't meet requirements.

- New MAPS generation in 65 nm CMOS imaging process developed by ALICE ITS3 collaboration.
  - Sensor specifications meet or even exceed EIC requirements.

ALICE

Specifications

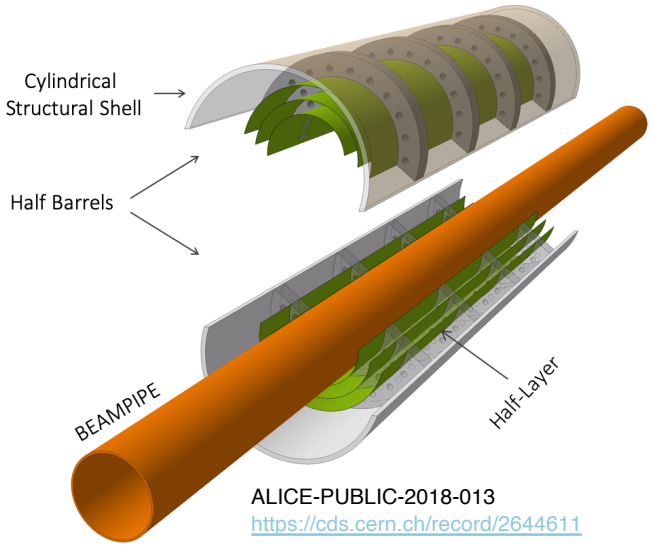
Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

M. Mager | ITS3 kickoff | 04.12.2019 |

ITS3 detector concept

- ITS3 vertex detector, 0.12 m^2.

- Innovative, truly cylindrical layout 0.05% X/X_0.
  - Wafer-scale (up to ~ 28 x 10 cm^2), thin sensor (20 - 40 µm), bent around beam pipe.
  - Air cooling (low power sensor, 50% reduction wrt ALPIDE)
  - Minimal support structure made of carbon foam rings and cylindrical structural shell.
  - No electrical services in active area.



ALICE-PUBLIC-2018-013
https://cds.cern.ch/record/2644611

The EIC can reuse the ITS3 sensor and detector concept for its vertex layers.

(Note: EIC has larger beam pipe radius)

From ITS3 to a 65 nm based EIC tracking system

- Dedicated EIC development for tracking layers and disks.
  - ITS3 wafer-scale sensor not suitable for staves & discs due cost/yield.
  - ITS3 0.012m^2, EIC ~6-8m^2.

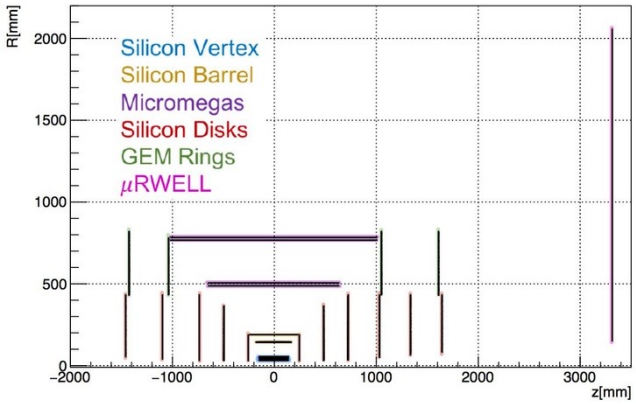
- Optimised ITS3 sensor size for low cost, large area coverage → EIC Large Area Sensor (LAS).
  - Same functionality and interfaces as ITS3 sensor, stitched but not wafer-scale.
  - Stitched sensor layout/size will need to be optimized to provide the coverage needed for each stave and disk.
  - Optimization will consider yield estimates from first engineering run.

- Staves derived from ITS2 structures; disks composed of overlapping staves or low mass CFC support discs.

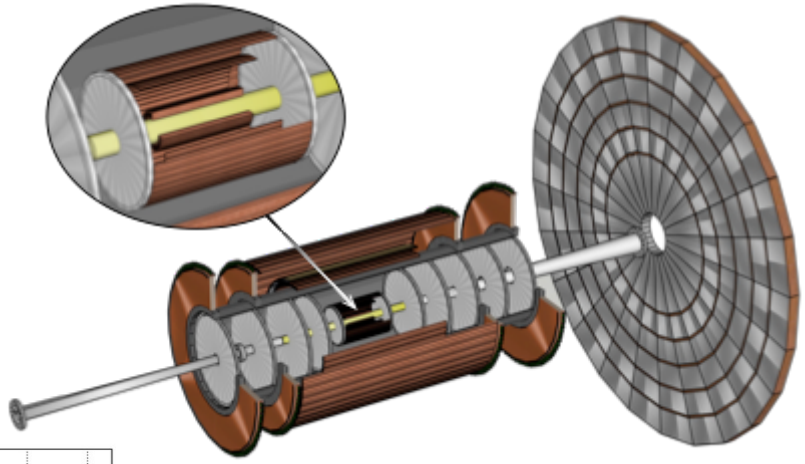
- Estimated material budget:
  - Baseline stave concept: 0.55% X/X_0
  - Baseline disk concept: 0.24% X/X_0

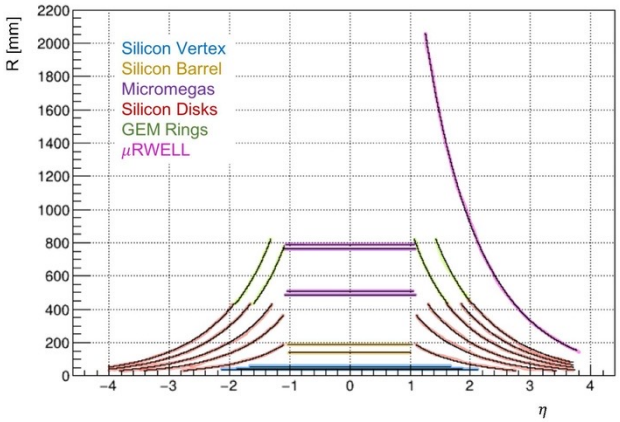
Example of EIC tracker: ATHENA hybrid tracker

- MAPS near the interaction point complemented by MPGDs at larger radii.
- Full coverage of the available space → tracking acceptance $-3.8 < \eta < 3.75$.
- Low material budget tracking with sufficient redundancy over a large lever arm.



Tracking material surfaces as a function of z





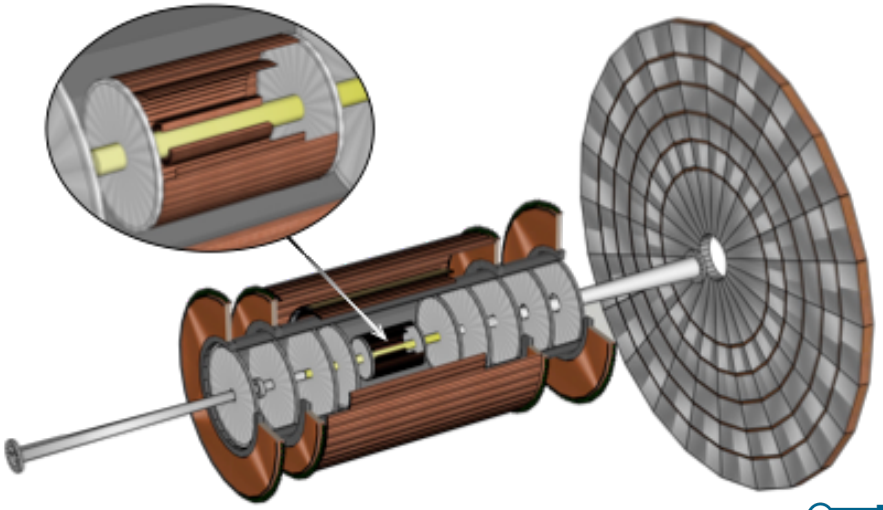
Tracking material surfaces as a function of pseudorapidity

ATHENA vertex layers

- 3 MAPS layers for vertexing (redundancy and low pT-threshold).
  - ITS3 sensor and detector concept, i.e. wafer-scale sensors, thin and bent around the beam pipe, 0.05% X/X0 per layer (ITS3 design).

- Radii from 1st eng CAD model based on possible stitched sensor size in phi.

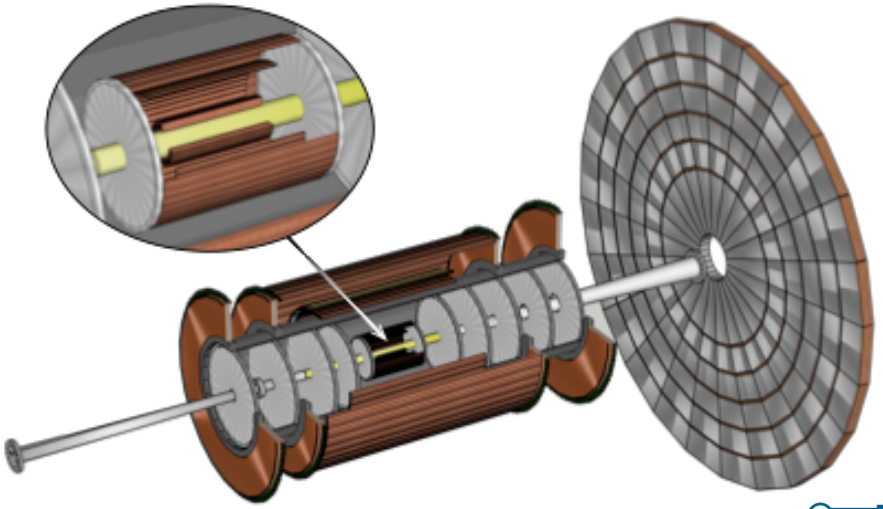
- Length = 28 cm: max length of a single sensor on wafer, allows for services on one side only; helps low material in negative direction.



ATHENA tracking layers and disks

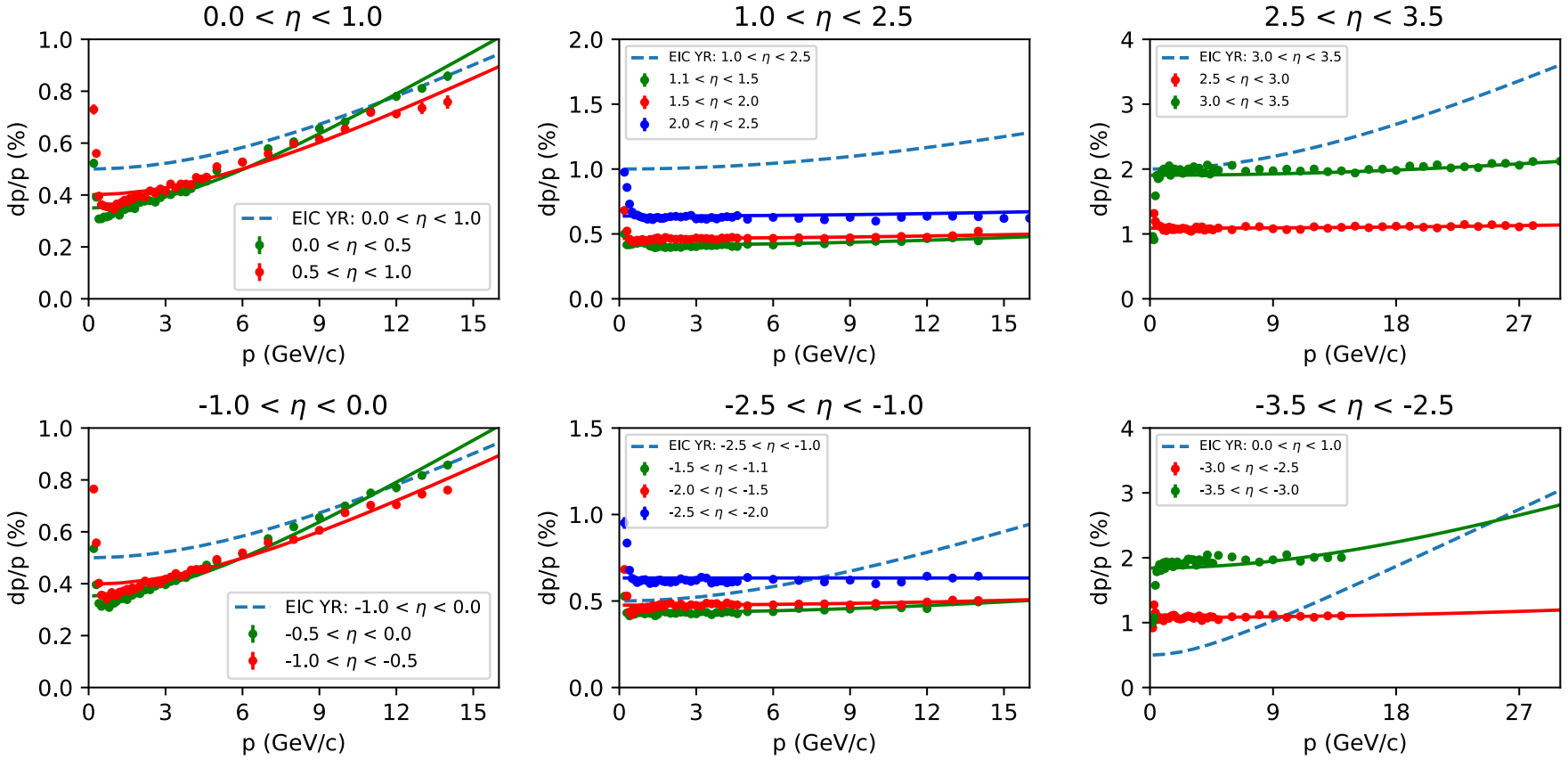
- 2 MAPS layers for sagitta measurements.
  - Stave structure with EIC LAS.
  - Conservative 0.55% X/X0 per layer, assumes water cooling, services running on the stave.

- 6 MAPS disks that extend until z = 165 cm for max lever arm.
  - Disk structure with with EIC LAS.
  - 0.24% X/X0 per disk.
  - 5 disks in the negative direction provide low material and enough of hits per track.



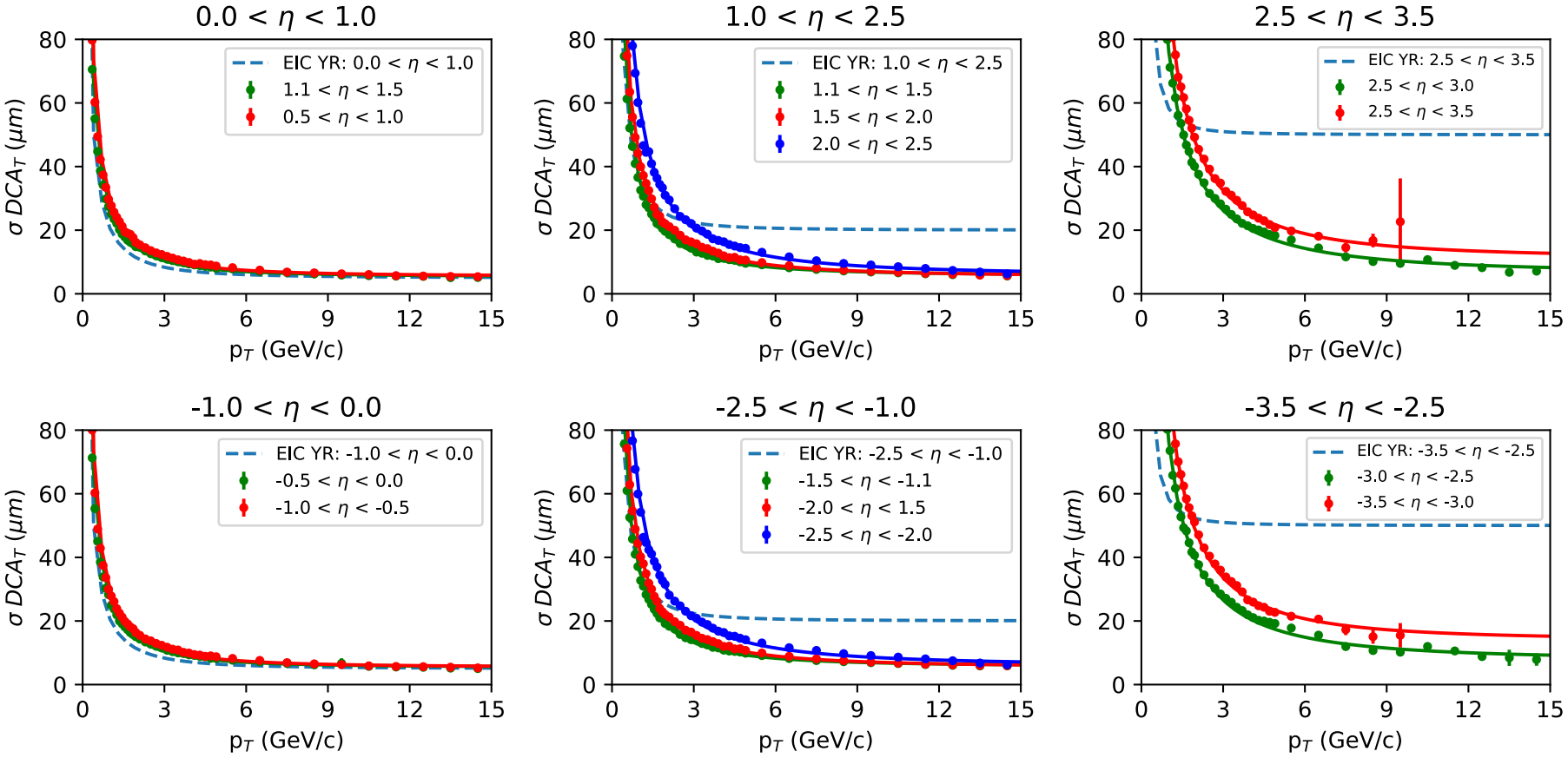
ATHENA SVT performance: dp/p

- Tracking performance meets or exceed the momentum resolution requirements stated in the Yellow Report, except for the most backward eta ranges.



ATHENA SVT performance: DCA_T

- Vertexing performance meet or exceed the DCA_T requirements stated in the Yellow Report, except for momenta below 2 GeV at very large eta ranges.



Even with state of the art Si (and MPGD technologies), the EIC physics requirements are challenging to meet.

Path to the EIC Silicon vertex and tracking detector

- Previous R&D efforts by LBNL & Birmingham in collaboration with RAL CMOS Sensor Design Group.
  - Beginning in 2015 & 2016, Efforts merged in 2020.

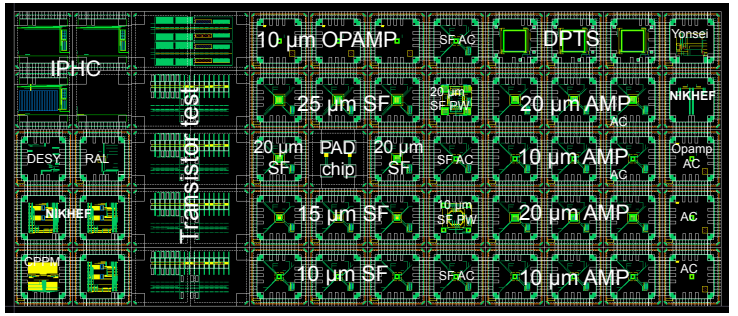
- Selected sensor technology, simulations for detector layout, performance plots.

- EIC Silicon Consortium formed in 2020 based on these efforts.
  - Larger group of participants, not based on one detector.

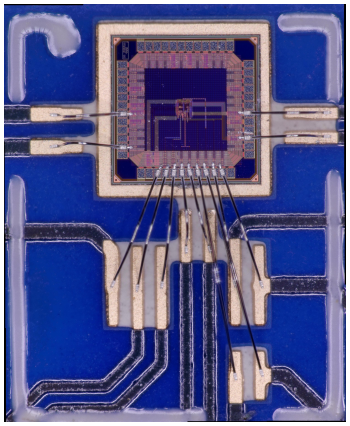
- Broader R&D effort starting.
  - EIC project funded eRD111/eRD104 + sensor development.

Sensor development

- Sensor design in collaboration with ITS3.



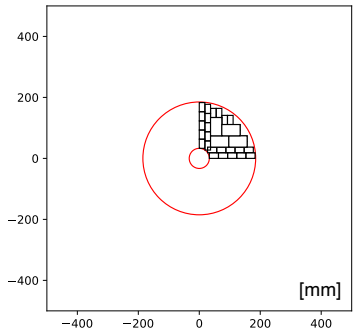
- First submission in 2021: MLR1
  - Multiple Layers per Reticule (MLR) submission to assess the suitability of the process for charged particles tracking.
  - Several small circuits submitted in a shared reticule to prototype as many structures as possible with the low cost.
  - EIC SC institutes contributed IP blocks for off-chip high speed data transmission.
  - Ongoing testing, no issue so far.

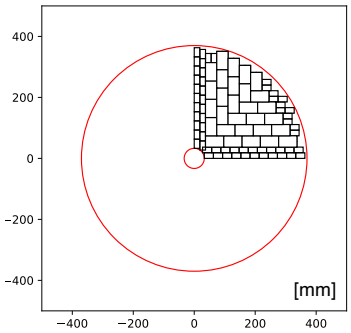


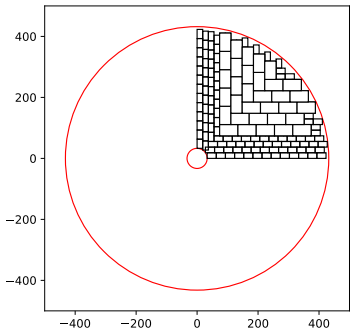
- ITS3 first engineering run: ER1, scheduled for May 2022.
  - First prototype of stitched wafer-scale sensor.
  - EIC SC institutes contributed further chips for off-chip and on-chip data transmission.

Sensor size vs. detector layout/coverage

- Conceptual studies have started to:
  - Understand achievable radii for vertex layers with ITS3 sensor width.
  - Size of the LAS for staves, tiling of disk
  - https://indico.bnl.gov/event/15486/contributions/62590/
  - https://indico.bnl.gov/event/15486/contributions/62591/







- This work is essential to:
  - Define LAS requirements to start design work (modification of stitching plan, possible modifications of the sensor peripheral circuits).
  - Progress work on all other detector aspects (stave & disks concepts, readout, mechanics and cooling).
  - Optimise detector layout (position of layers, routing of services, material budget, etc.).

eRD104: Service reduction

- Investigate methods to significantly reduce the services load for an EIC MAPS based tracking detector.

- Efforts are concentrated on the areas where the bulk of the detector services exists: powering distribution and the readout system.

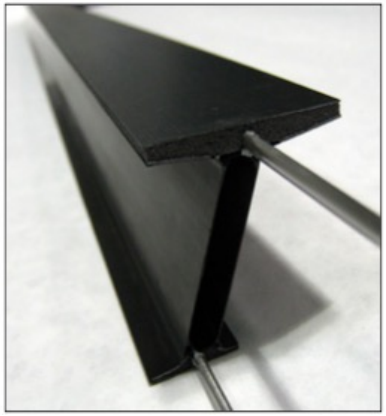
- Powering:
  - Radiation tolerant DC-DC converter, serial powering architectures with integrated regulators.
  - Preliminary work: https://www.eicug.org/web/sites/default/files/Powering-options-for-an-EIC-silicon-tracker.pdf

- Readout:
  - Data aggregation on detector using radiation tolerant FPGAs.

eRD111: Si-vertex (excl. sensor)

- Development of all aspects of the full tracking detector, beyond the sensor.
  - Forming modules from stitched sensors.
  - Stave/disc construction.
  - Mechanics and cooling.

- Electrically and mechanically integrated module concepts designed for automated loading on staves and discs; exploration of reliable, low-cost interconnection techniques; air cooling through carbon foam between face sheets of disc plates; etc.



Conclusion

- Strict tracking requirements necessary for physics goals at the EIC need a detector with high granularity & ultra low material budget.
- New generation 65 nm MAPS offer the best solution.
- R&D is carried out with the EIC SC to develop a full detector implementation.
- Sensor development is advancing well both in silicon and coupled with detector layout definition.
- eRD111 and eRD104 are designed to address challenges of designing a 65 nm based detector with low material solutions for supports, powering, cooling readout.

Backup