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Sensor Design Reports and EIC Large Area Ideas

31/01/21

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Sensor Design Reports

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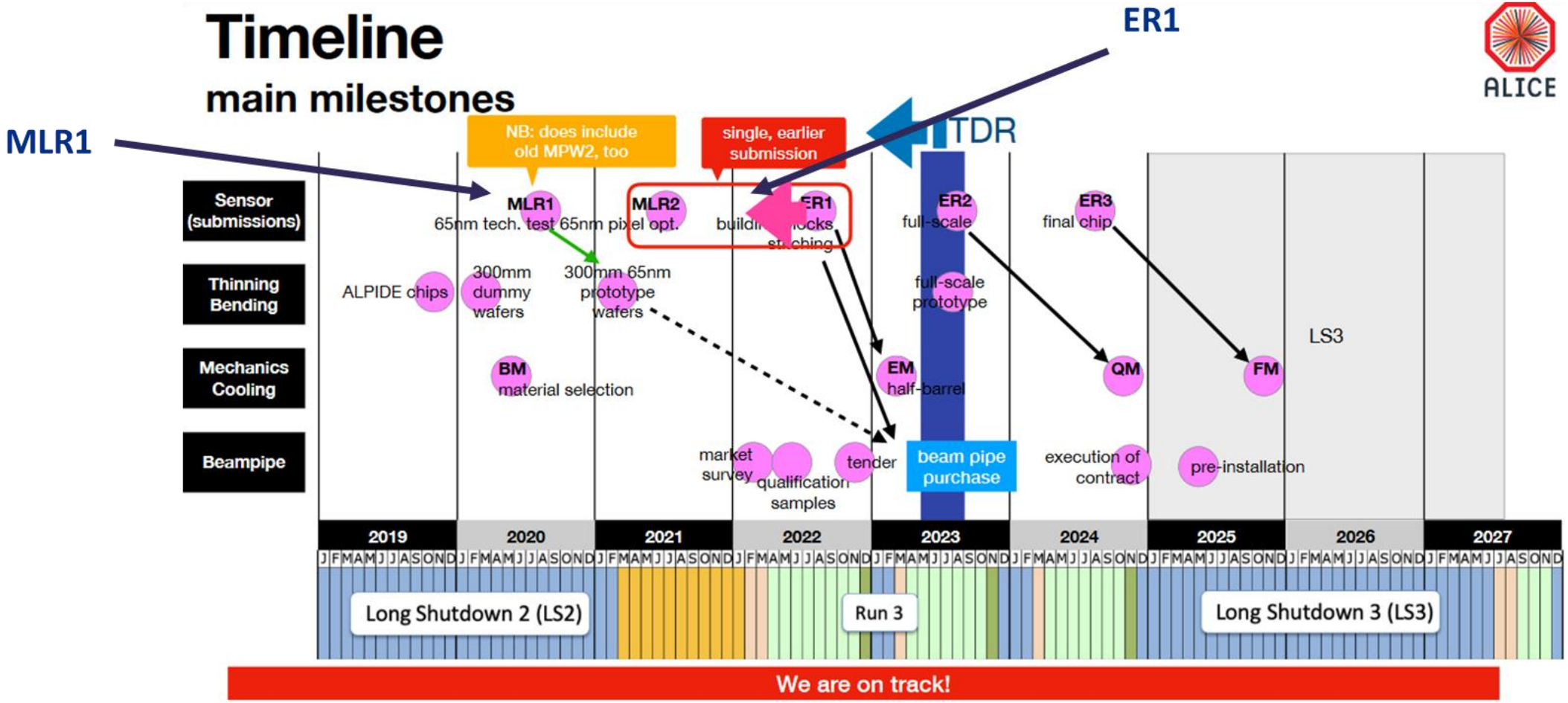
Timeline



MLR: multiple layer per reticle, **ER:** engineering run,
BM: breadboard module, **EM:** engineering module, **QM:** qualification module, **FM:** final module

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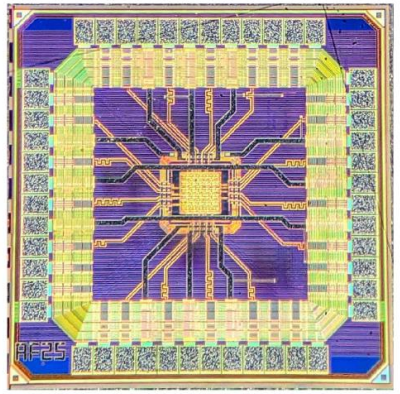
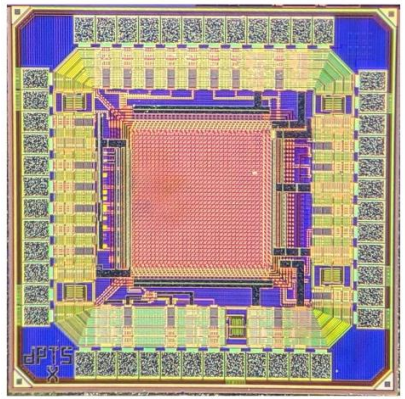
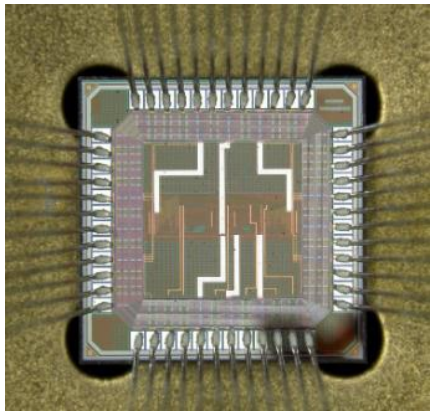
MLR1 Overview - Chips



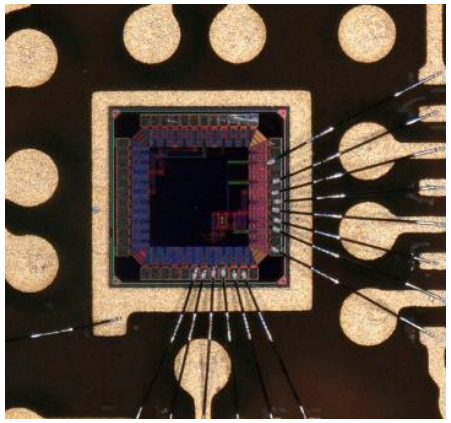
APTS (CERN)



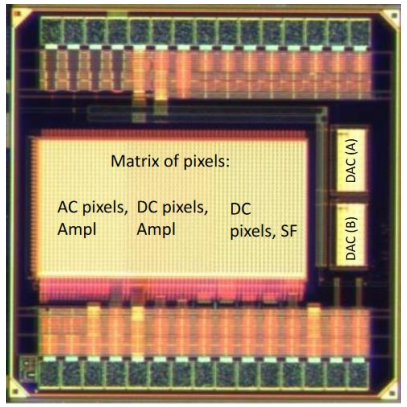
DPTS (CERN)



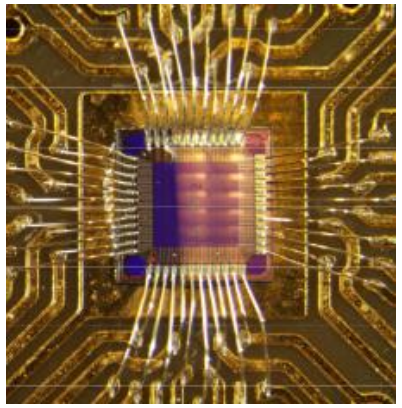
RO (CPPM)



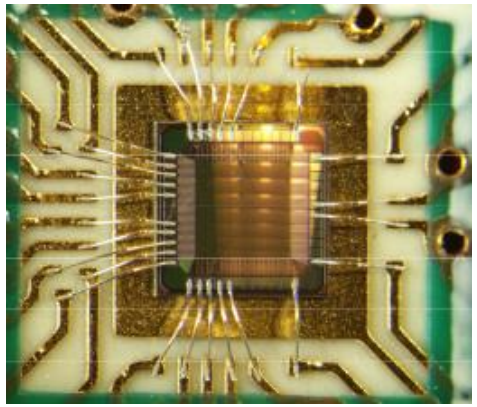
Pixels (DESY)



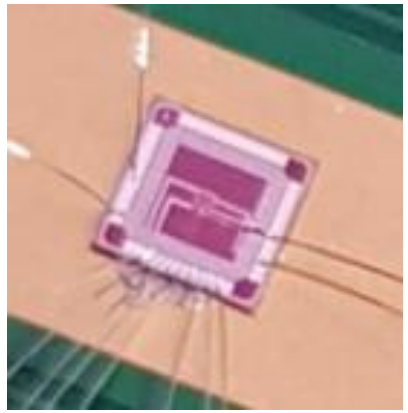
CE65 (IPHC)



Bandgap (NIKHEF)



VCO (NIKHEF)



CML (RAL)

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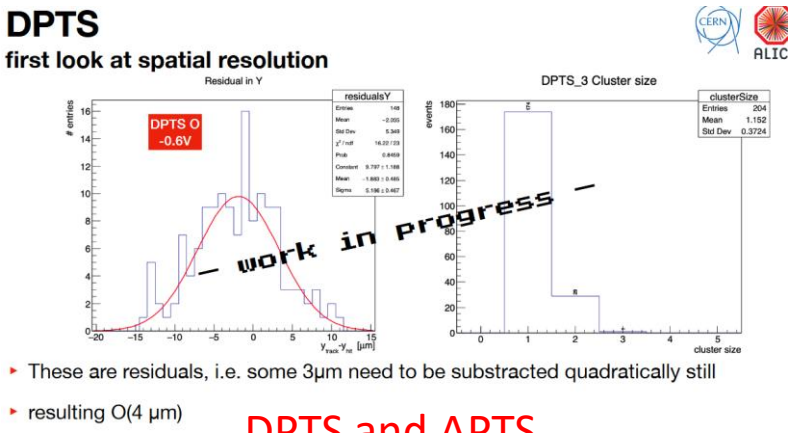
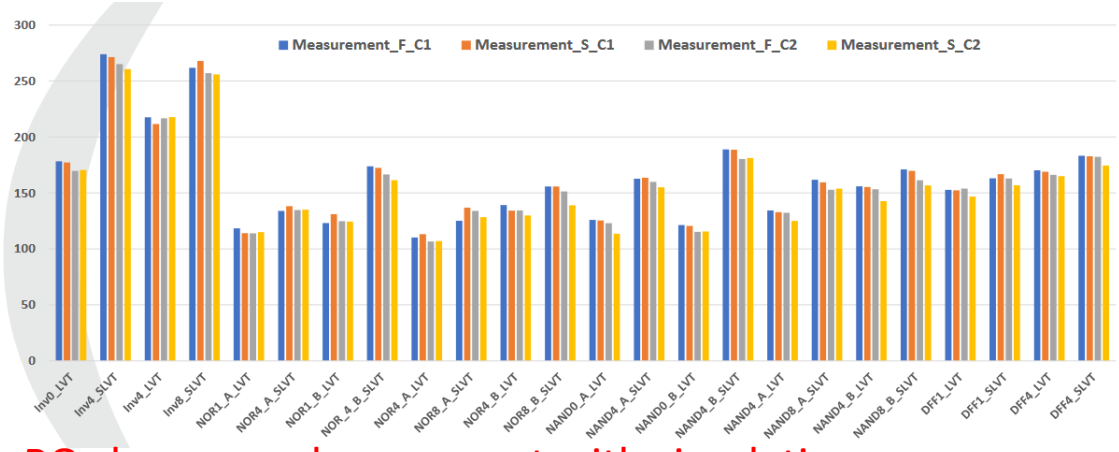
MLR1 Overview - Testing

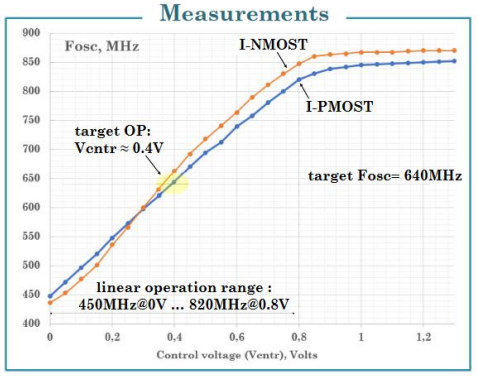


- These are residuals, i.e. some 3µm need to be substracted quadratically still
- resulting O(4 µm)

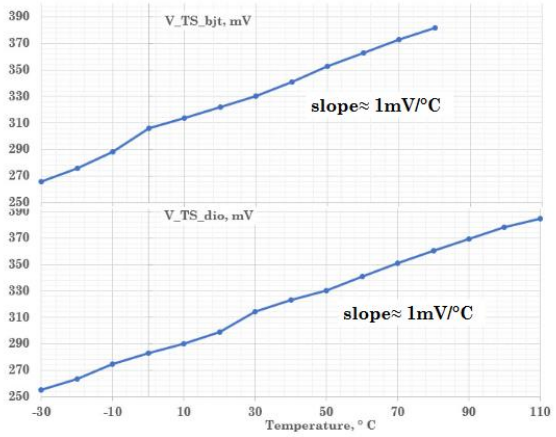
DPTS and APTS
both in beam test

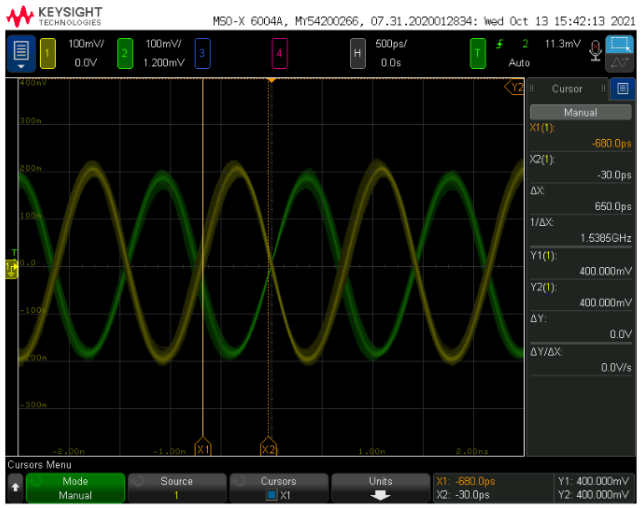


RO shows good agreement with simulation.
Irradiation planned.



Temperature sensor and
VCO fully functional





CML driver fully functional. More
advanced test system planned.

- Also many, many more. Transistor test structures, pixels, etc, etc…
- https://indico.cern.ch/event/1091910/

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ER1 Design Activity

- See most recent ITS3 WP2 plenary for more detail (https://indico.cern.ch/event/1117024/contributions/4691459/attachments/2380633/406)

Chips for ER1: still to be updated and mapped into floor-plan

Design	Purpose	Institute	# of test sites	Comments
MOSS	stitched sensor prototype develop stitching know-how, more conservative Focus on technology options, power distribution, signal routing, yield	INFN, IPHC, NIKHEF, CERN	-	1D stitching Matrix as simple as possible
MOST	Stitched sensor prototype, develop stitching know-how, more aggressive Study yield with high density layout parts and fine power segmentaton Low power and transmission of timing information over long distance	NIKHEF, IPHC, Heidelberg, CERN, INFN	-	Many parts in common with MOSS
H2M	Hybrid to Monolithic Investigate MAPS and architectures in non-stitched sensor	DESY and CERN	2	
CE65++	Pixel optimization vehicle Focus on optimizing pixels and front-end	IPHC	tbd	
SEU chips	Prototype with memories and flops Measure SEE cross-sections (SEL, SEU)	INFN Bari	2	
PLL NIKHEF	First step in high speed transmitter	NIKHEF	1	High speed transmission
PLL+buffer	First step in high speed transmitter	RAL	1	High speed transmission
Pixel test DESY	Pixel sensor and front end prototype	DESY	1	
Pixel test SLAC	Pixel matrix prototype	SLAC	1	
APTS	Analog pixel test structure	IPHC and CERN	tbd	
DPTS	Digital pixel test structure	CERN	tbd	
TTS1-5	Transistor test structures	CERN	10	
~~ADC prototype~~	~~Desired function~~	~~not covered~~		~~generated from DAC ?~~
~~Supply regulation~~	~~Desired function~~	~~not covered~~		~~Interest from several corners~~

To be refined

Based on measurements

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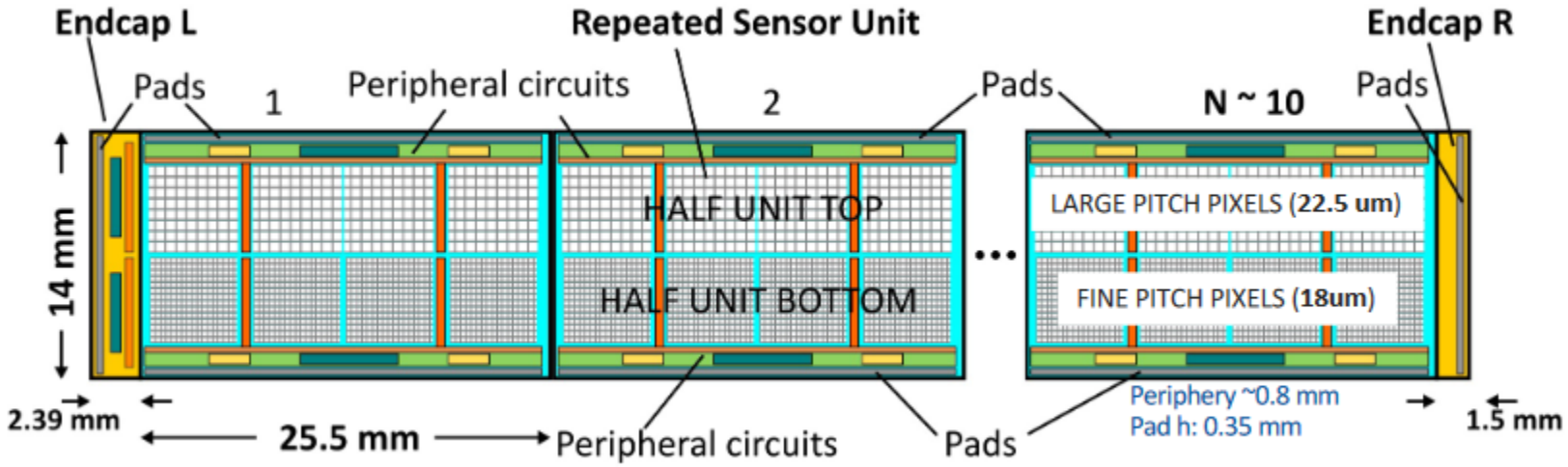
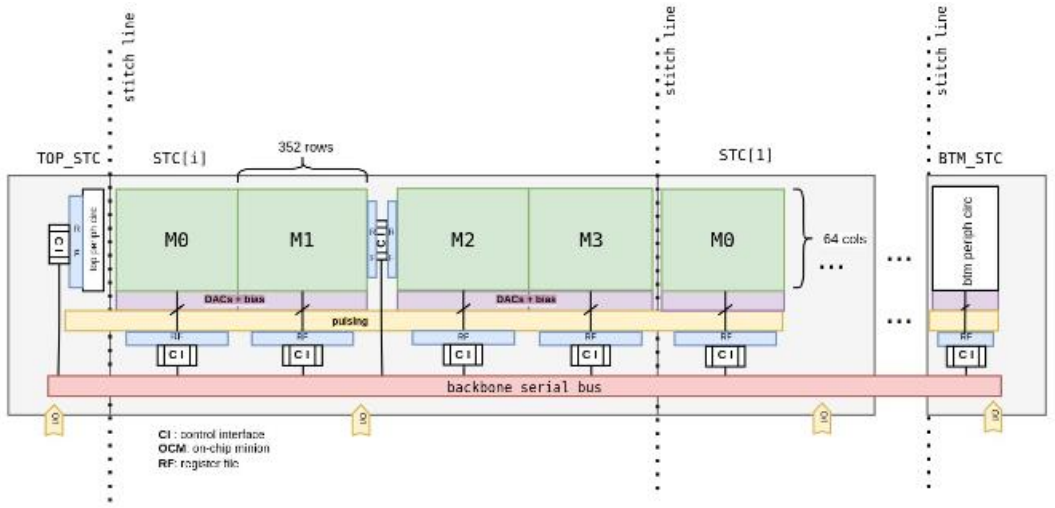
ER1 Design Activity – MOSS and MOST

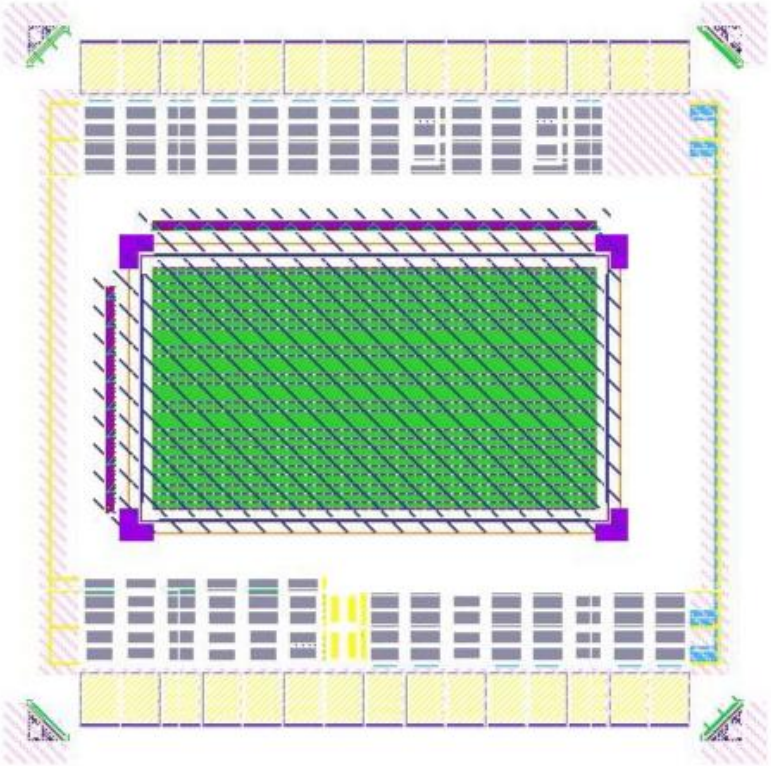


Primary Goals
Learn Stitching to make a particle detector
Interconnect power and signals on wafer scale design
Learn about yield and DFM
Study power, leakage, spread, noise, speed

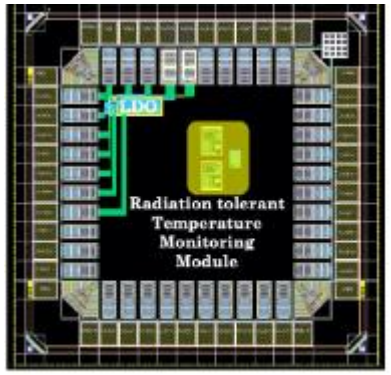
- Investigate **yield** when local density is preserved
  - Global power domains over full chip (Digital/Analog)
  - higher granularity in power gating in case of a defect of
    - analog (rows of 4 pixels)
    - digital (half columns)
  - PWELL tied to ground
    - reverse sensor biasing achieved by higher power supply
- Immediate transfer of hit data to the periphery (bottom endcap, 4 CML outputs)
  - event-driven asynchronous readout (no strobing) over long distance
    - serial binary address transmission for this implementation

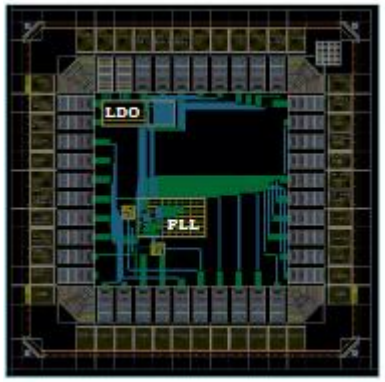


ER1 Design Activity – Other Chips

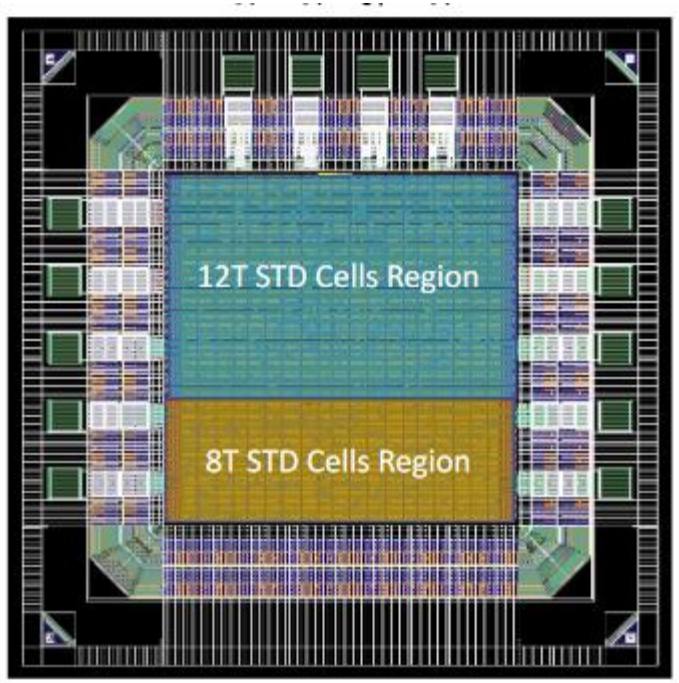


IPHC: CE65





NIKHEF: LDO, PLL for serialiser



INFN: SEU test chip

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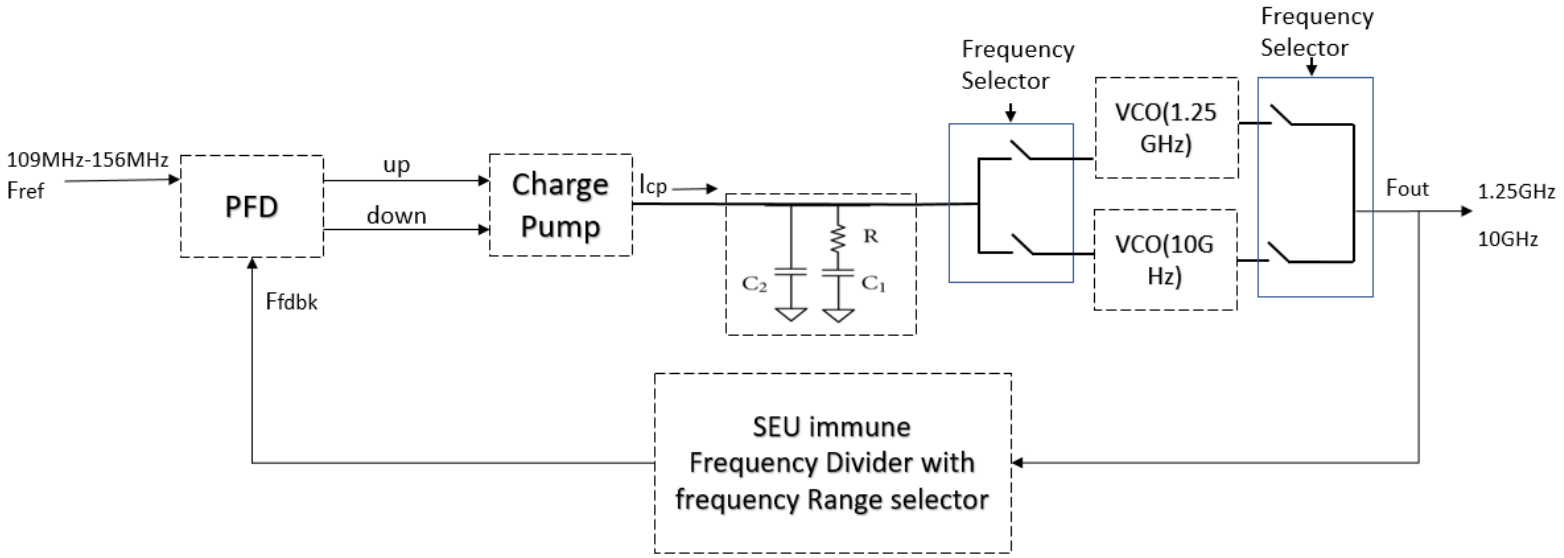
ER1 Design Activity – "EIC" Groups

RAL

- Design of PLL with dual frequency operation: 10GHz or 1.25GHz.
- Frequency selection switch
- Range of output frequencies are possible by varying the input reference frequency.



Specifications

- ❑ Supply Voltage : 1.2V
- ❑ Output Frequency : 7GHz-10GHz OR 500MHz-1.5GHz
- ❑ Input Reference clock : 109MHz-156MHz
- ❑ Jitter : <10%

LBNL/Brookhaven

- NDAs signed, PDK available
- Discussing best way to contribute
- Effort complicated by Continuing Resolution

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Large Area Sensor – First Thoughts

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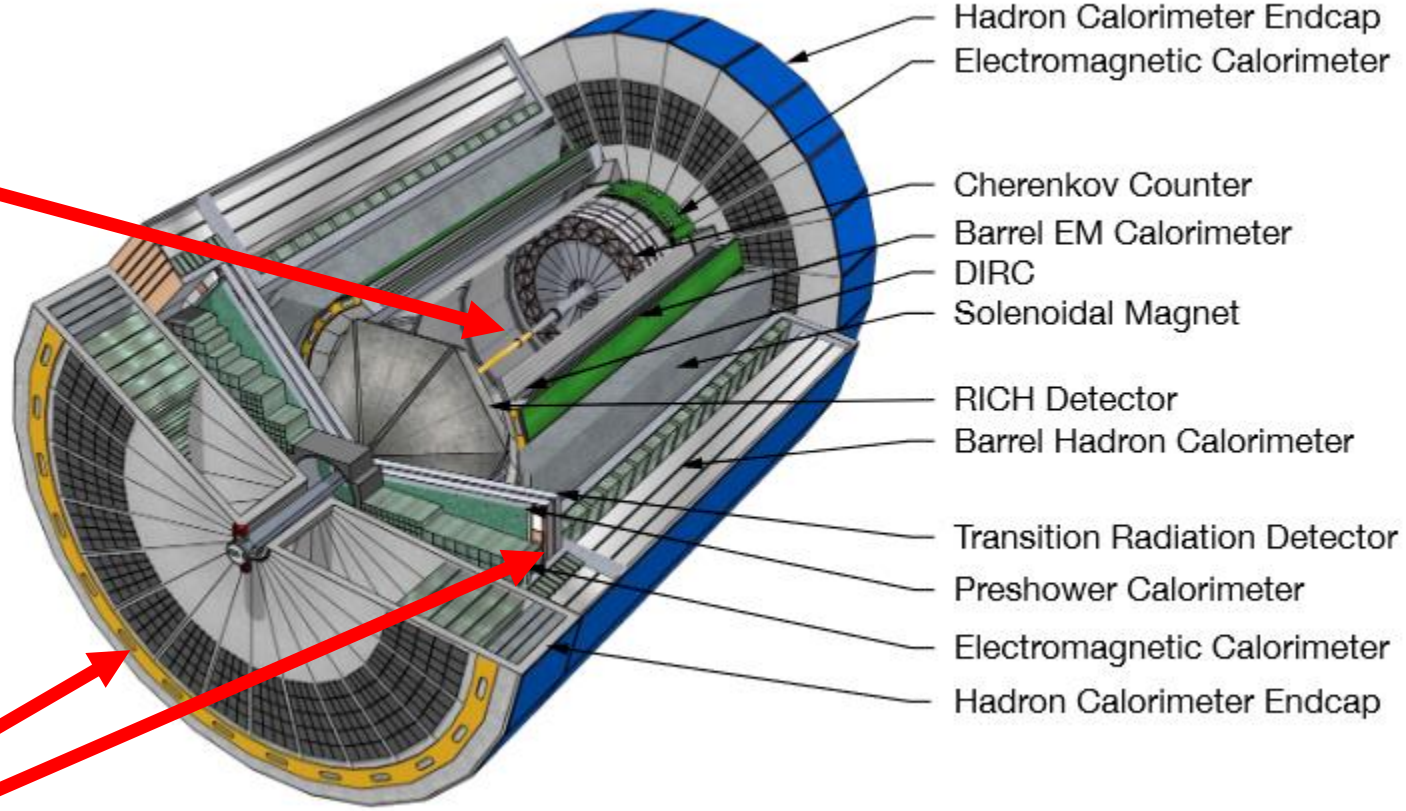
Introduction

- EIC will require 2 sensors:
  - Vertex chip: Likely to be identical to the ALICE ITS3 detector
  - Stave and disc chip: A large silicon area needs to be covered and the yield of the wafer-scale chip is likely to be too low for this. Therefore a chip functionally similar to the vertex device, but with a different layout, will be needed.



EIC Yellow Report Summary - http://www.eicug.org/web/sites/default/files/EIC_YR_Summary_v1.0.pdf

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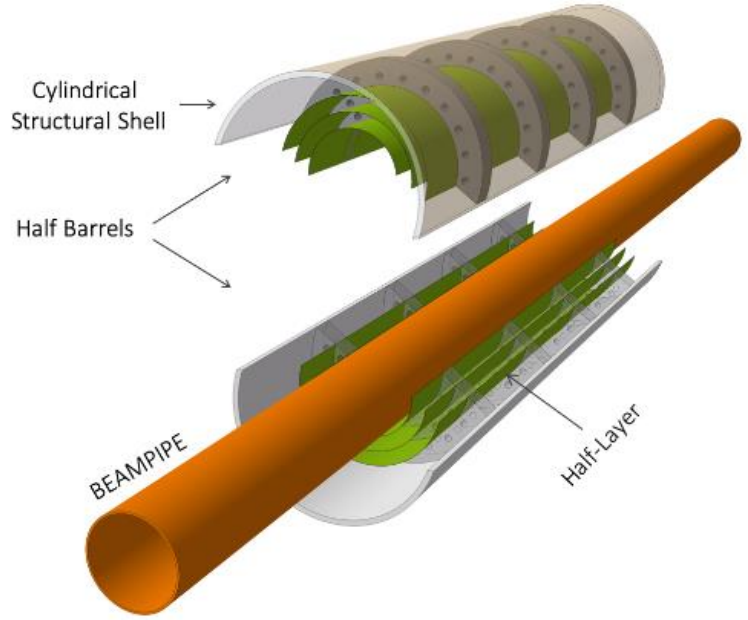
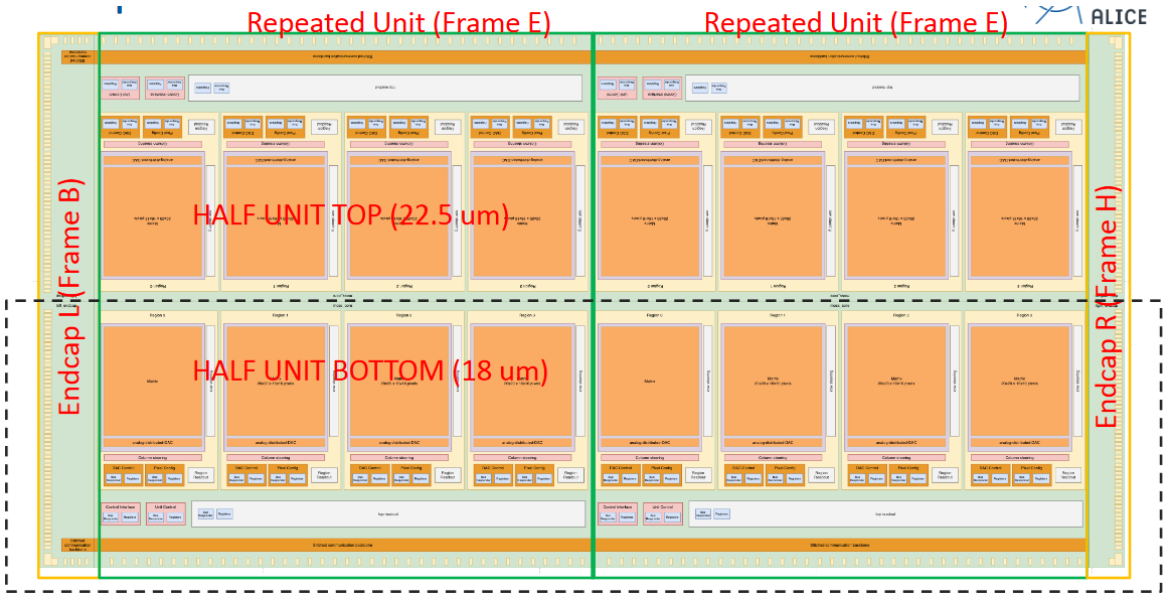
- Goal of this presentation is to discuss technical and organisational paths towards this

Vertex Chip

- “Top-level” idea for the vertex chip is fairly simple (even if technically complex!)
- ITS3 chip likely to be suitable. Ideal would be to use this. Development already underway, several EIC groups engaged in working with ITS3.
- Different barrel arrangement may be needed.
- **Remaining issues to resolve:**
  - Agreement for the supply of this device
  - Agreement on required EIC financial contribution to ALICE
  - Mechanical arrangement





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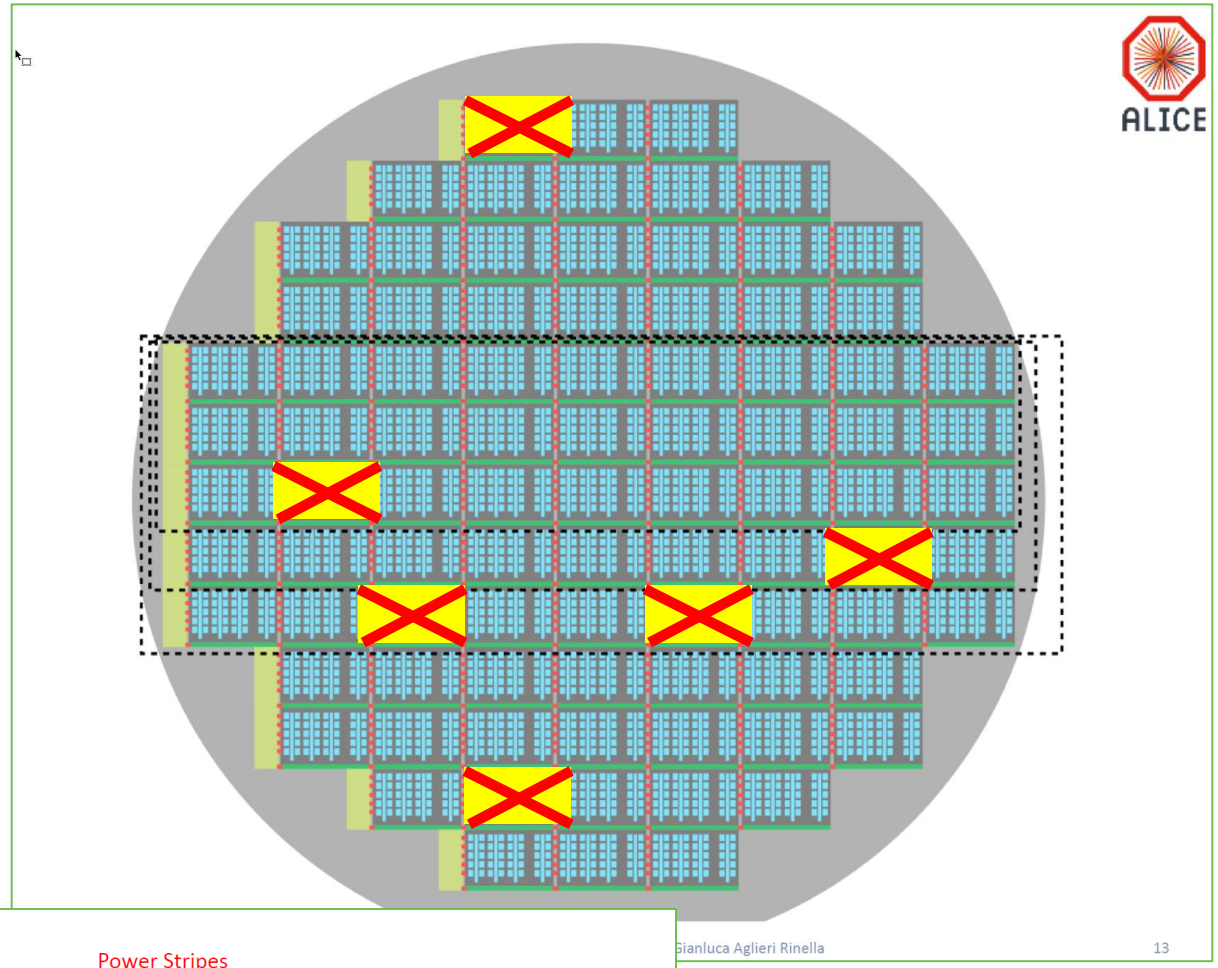
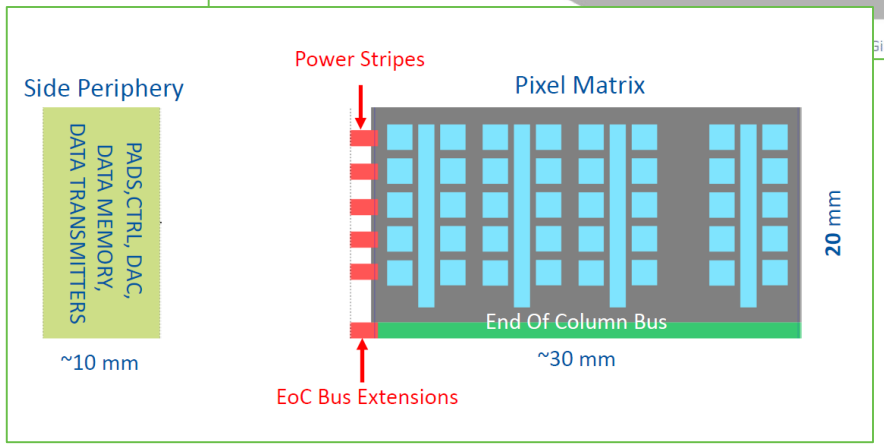
Stave/Disc Chip

- “Top-level” plan is more complex than for the vertex chip.
- 3 main issues are:
  - How to achieve the required yield?
  - What technical configuration do we want for this chip?
  - What design path will we follow?
- Several options in following slides. And also must not forget the option that yield is good and wafer scale chip could be used for both!





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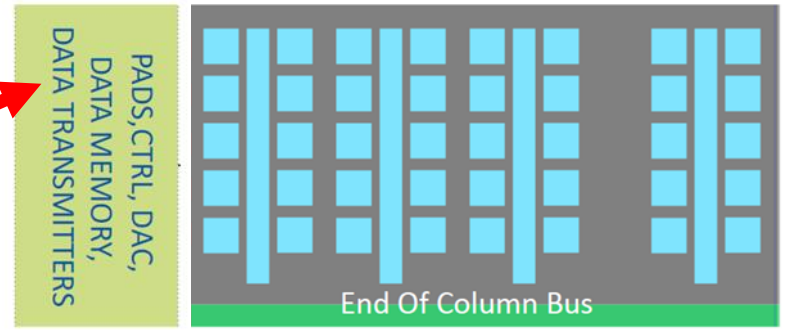
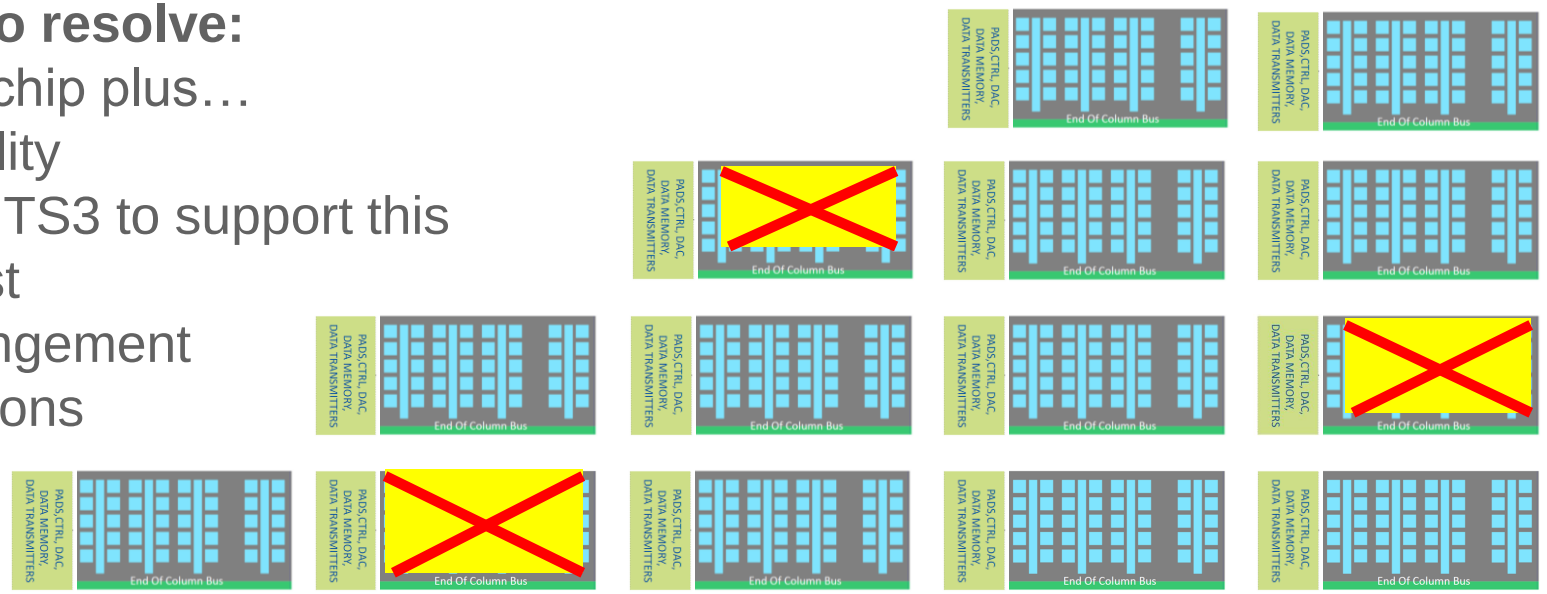
Stave/Disc Chip - Option A

- Simplest option is to just adjust the stitching plan for our requirements
- Result would be small chips like this
- This leaves a dead area and construction would have to be something like this



- **Remaining issues to resolve:**
  - Same as vertex chip plus…
  - Technical feasibility
  - Agreement with ITS3 to support this
  - Timeline and cost
  - Mechanical arrangement
  - Physics Implications



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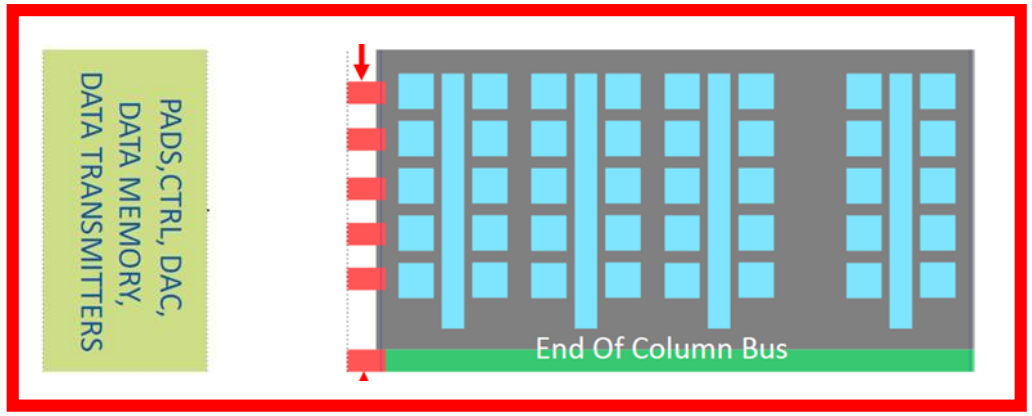
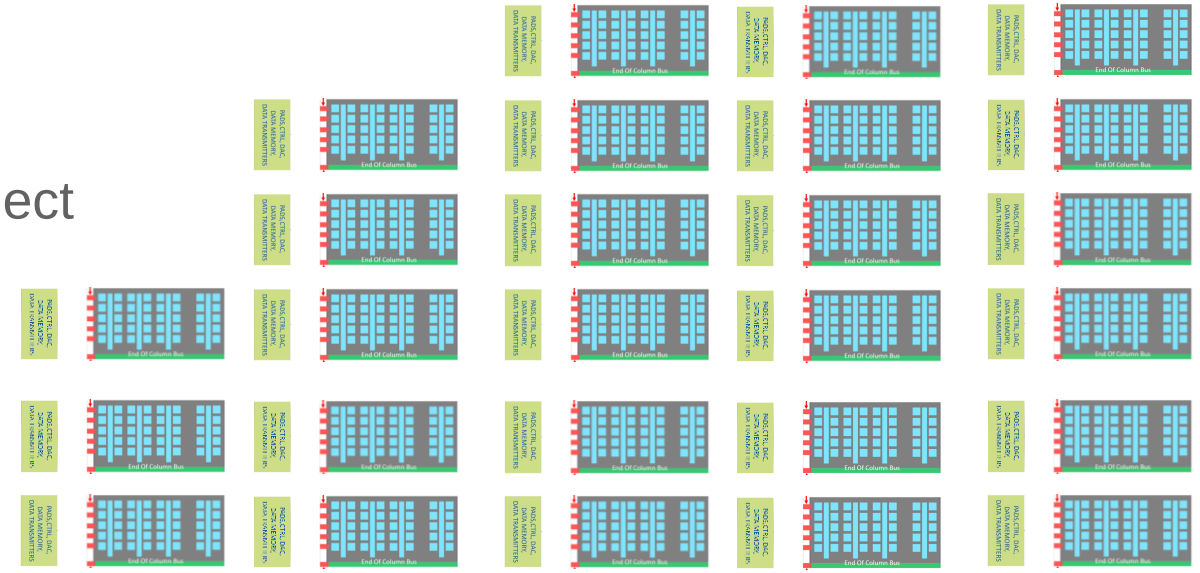
Stave/Disc Chip - Option B

- Adjust design to produce a separate “periphery” and “pixel” block
- Pixel blocks could transmit data through from others to reach periphery blocks. All could be wire bonded together.
- Reticle and wafer would look like this
- Idea would then be to assemble wire-bonded staves like this with limited dead area
- Yield could be improved by wafer probing to select only good pixel blocks for staves





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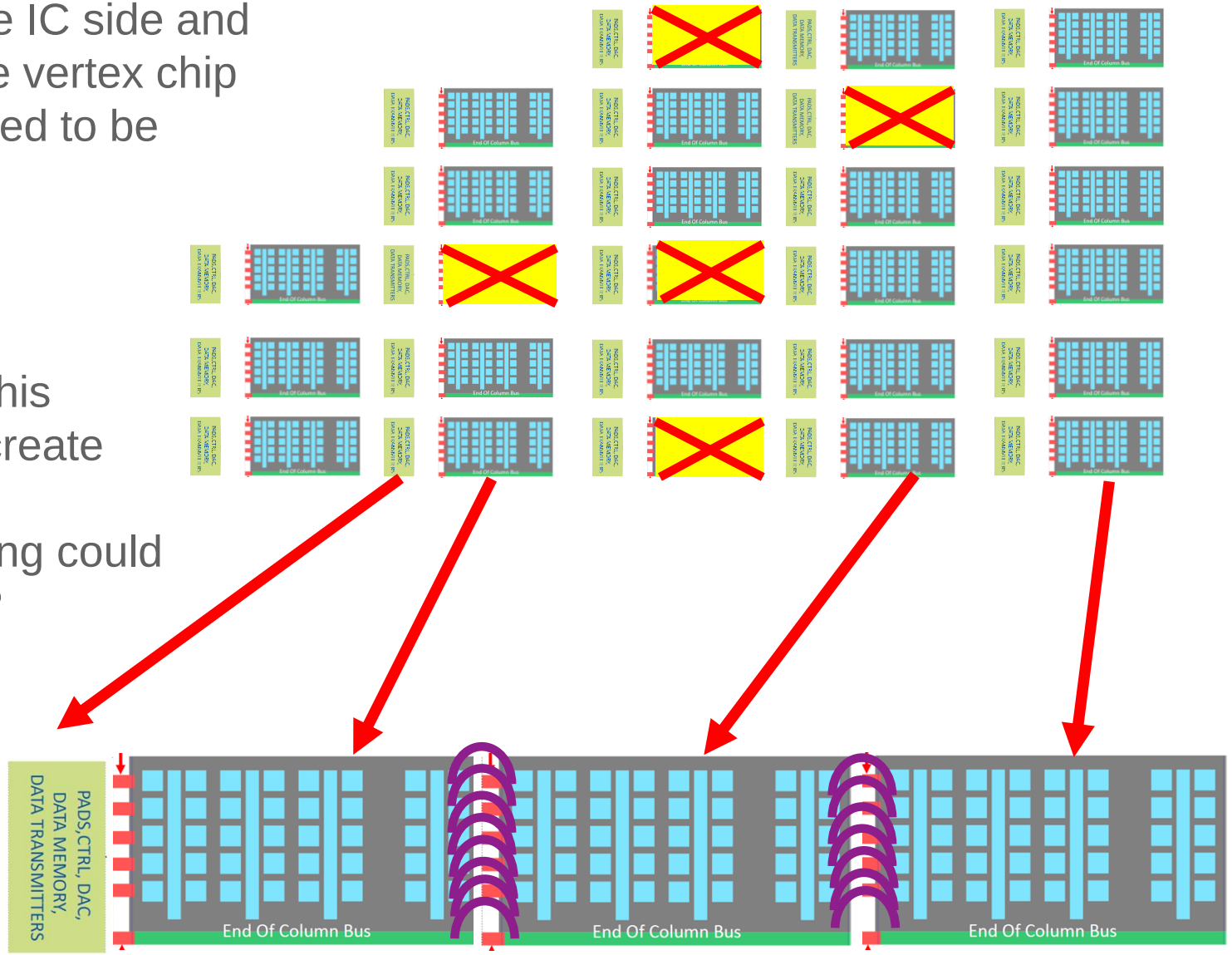
Stave/Disc Chip - Option B

- This would require design work on the IC side and access to the design databases of the vertex chip
- Wire bond pads and drivers would need to be added in the pixel blocks

- **Remaining issues to resolve:**

  - Agreement with ITS3 to support this
  - Define blocks we would have to create
  - Determine foundry access
  - Mechanical arrangement. How long could staves be? Still some dead area?
  - Physics Implications
  - Timeline
  - Cost



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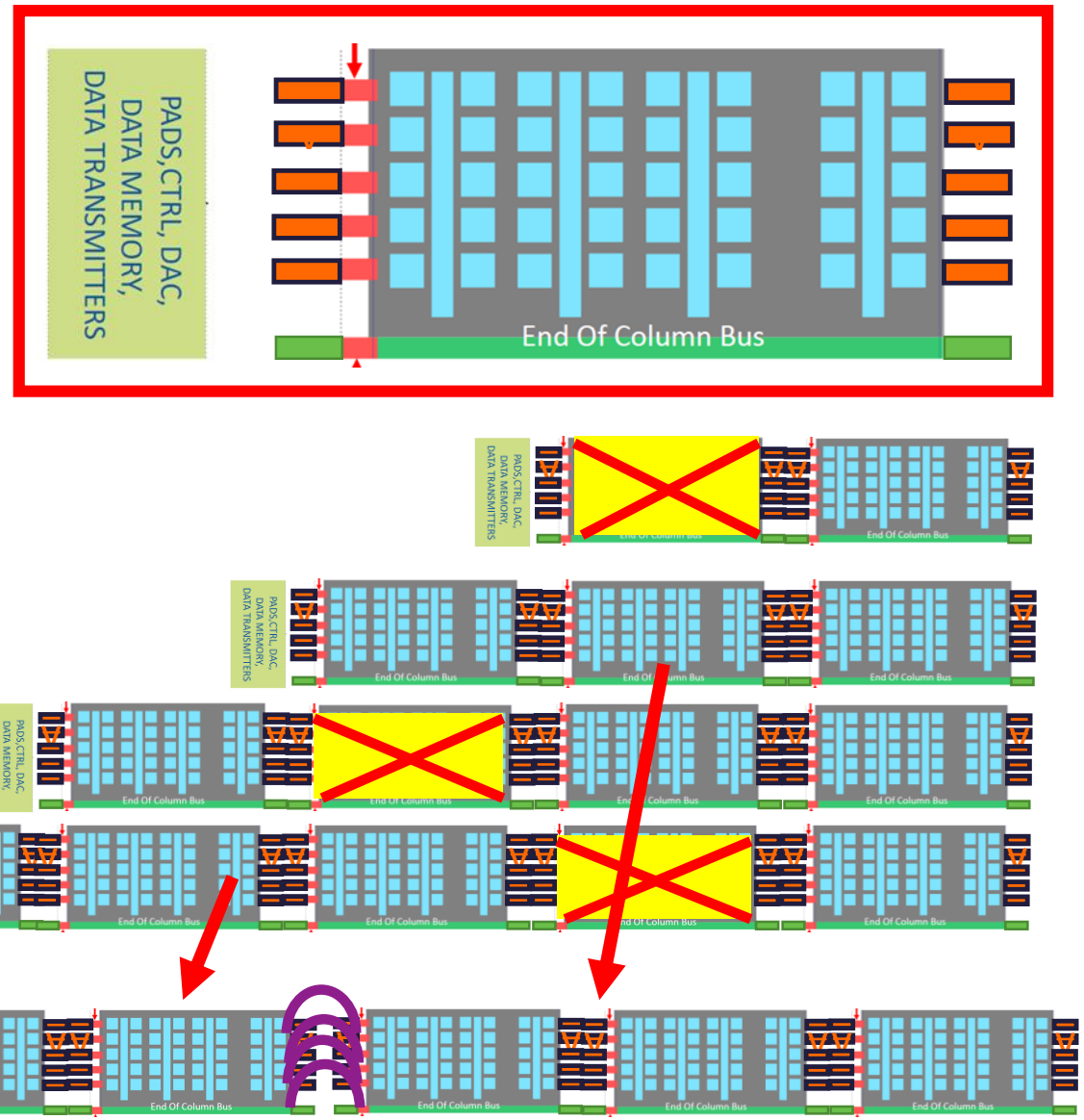
Stave/Disc Chip - Option C

- Similar to option B, but make the connections on the wafer between “pixel” stitching blocks
- Makes greater use of the stitching technology and reduces wire bonding
- Probing and dicing is more complex
- Would still need to add bond pads for those chips that need them, and for probing

- **Remaining issues to resolve:**
  - Same as option B
  - How to detect power-ground shorts?
  - More complex dicing needed



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Stave/Disc Chip - Option D

- Do not base stave/disc device on vertex chip. Produce a completely separate design.
- Requires no ITS3 data, but vastly increased design effort and silicon cost.

- **Remaining issues to resolve:**

  - Define specification
  - Determine foundry access for production
  - Mechanical arrangement. How long could staves be? Still some dead area?
  - Timeline, cost and physics implications

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Questions?

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