Getting involved in the ITS3 MLR1 testing campaign

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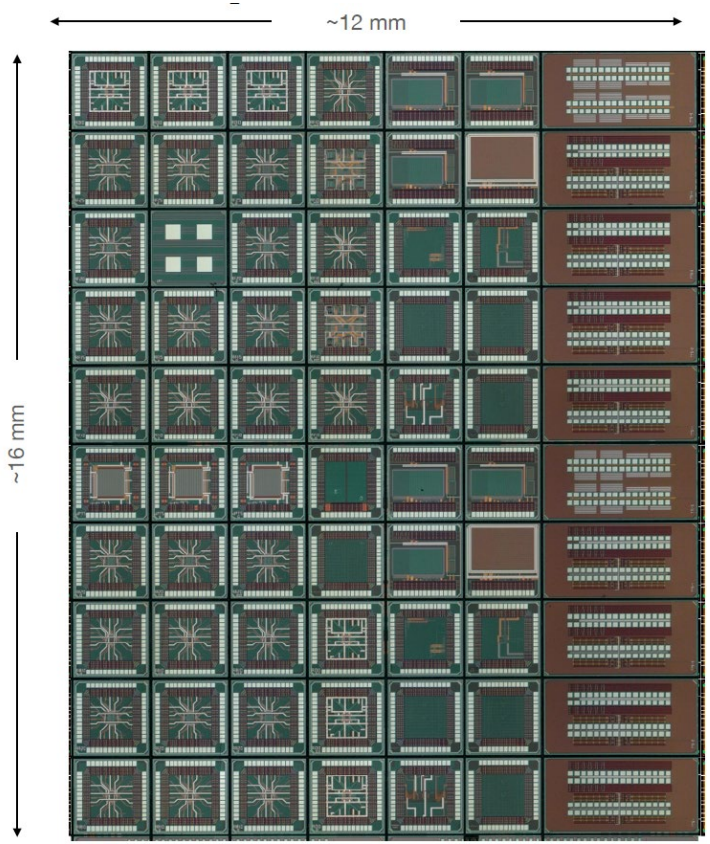
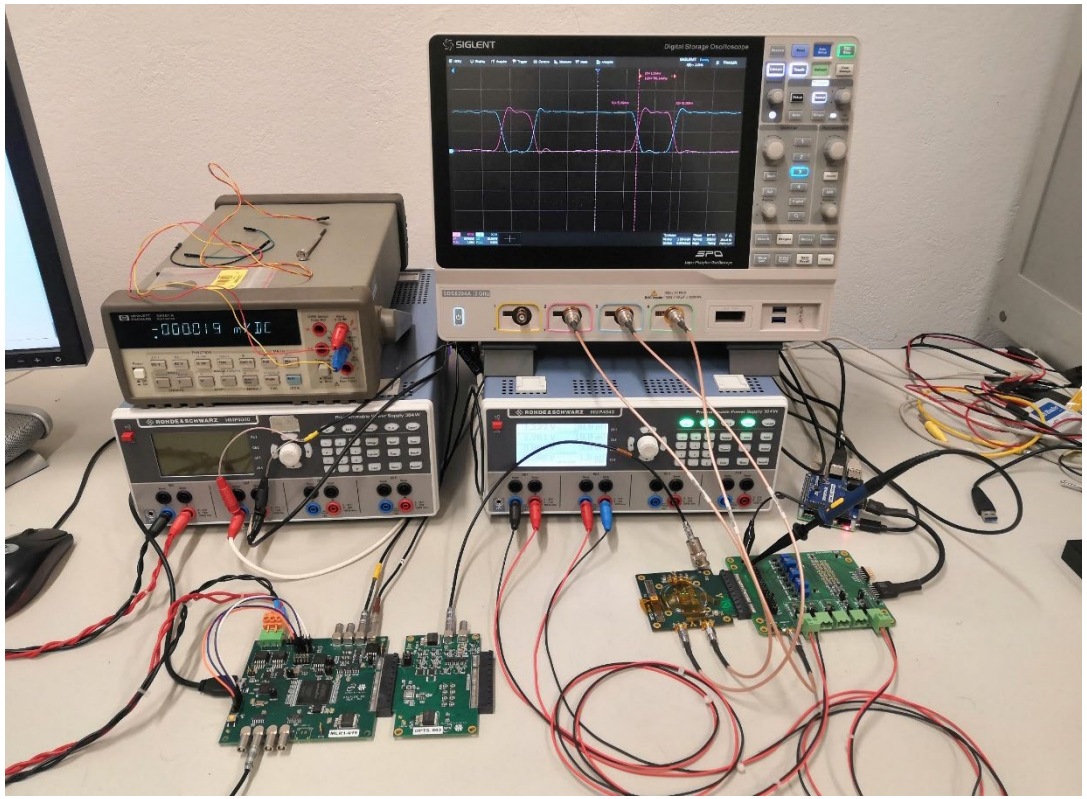
Università di Trieste and INFN Sezione di Trieste

EIC Silicon Consortium meeting – Jan 27th 2022





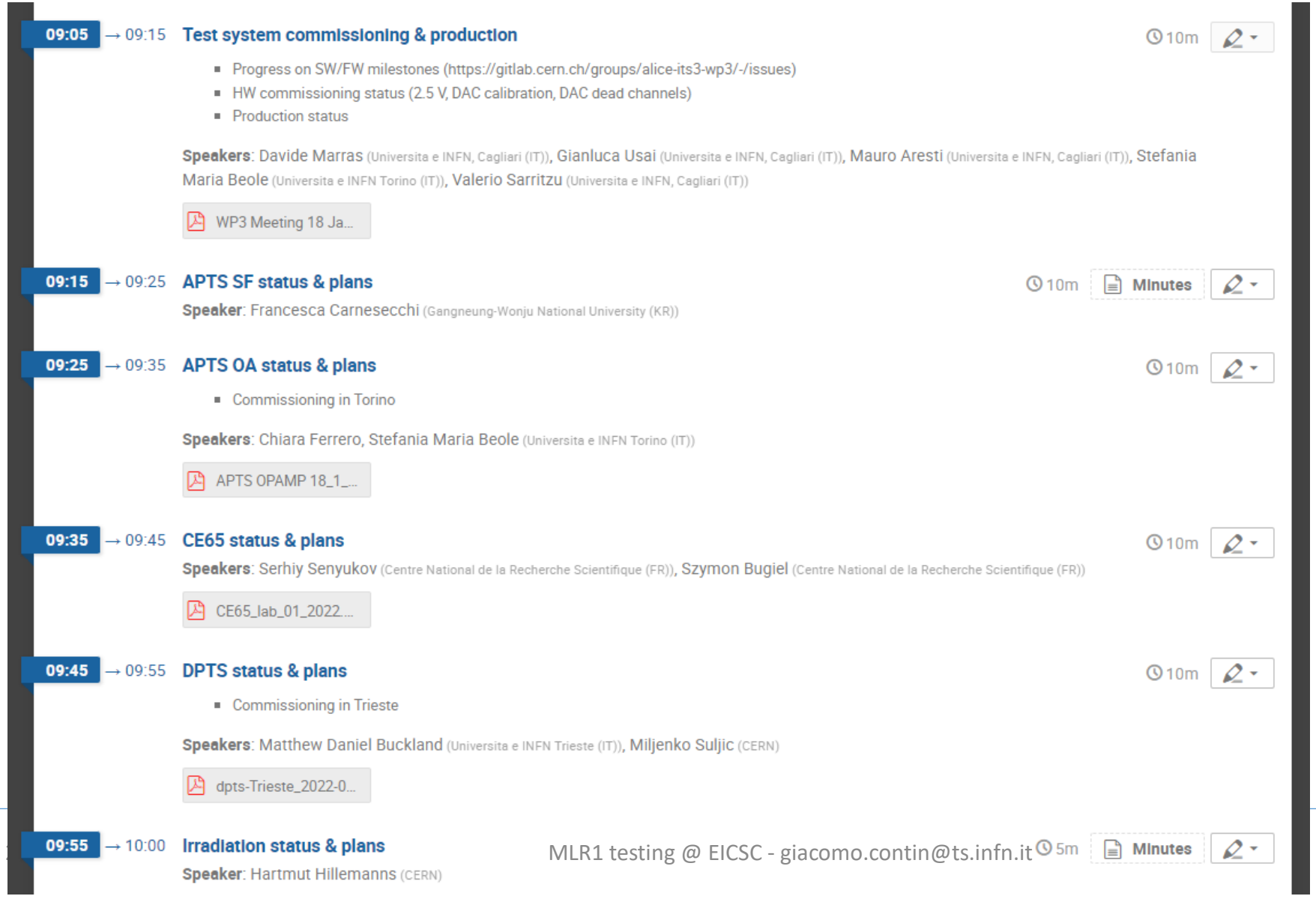
How to get involved in the ITS3 MLR1 testing

- Requirements to get involved in the MLR1 and future ITS3 chips:
  - A longer commitment to ITS3 beyond the testing phase is preferable
  - Training is not possible upon request, joining in person an experienced group is preferable
  - Local supervision at the Institute: students/unexperienced researchers have to be locally supervised, since no supervision from the ITS3 team is available
  - Constant support from CERN team / experienced teams is not guaranteed
  - … please let us know if these requirement sound reasonable for your participation

From previous presentations

- Suggested path to actively join the activities:
  1. Inform/negotiate with Alex Kluge and Magnus Mager at the institutional level
  2. Inform Miko Suljic and Sergey Senhiukov at the technical level
     - Join ITS3 WP3 e-group to access https://twiki.cern.ch/twiki/bin/viewauth/ALICE/ITS3WP3 (requires ALICE membership)
     - Express interest / request test system or access to data
  3. Start learning independently from points 1) and 2) outcome
     - See how in the next slides

MLR1 testing /1 : test system and chip testing



09:05 → 09:15 **Test system commissioning & production** 10m

- Progress on SW/FW milestones (https://gitlab.cern.ch/groups/alice-its3-wp3/-/issues)
- HW commissioning status (2.5 V, DAC calibration, DAC dead channels)
- Production status

Speakers: Davide Marras (Universita e INFN, Cagliari (IT)), Gianluca Usai (Universita e INFN, Cagliari (IT)), Mauro Aresti (Universita e INFN, Cagliari (IT)), Stefania Maria Beole (Universita e INFN Torino (IT)), Valerio Sarritzu (Universita e INFN, Cagliari (IT))

WP3 Meeting 18 Ja...

09:15 → 09:25 **APTS SF status & plans** 10m Minutes

Speaker: Francesca Carnesecchi (Gangneung-Wonju National University (KR))

09:25 → 09:35 **APTS OA status & plans** 10m

- Commissioning in Torino

Speakers: Chiara Ferrero, Stefania Maria Beole (Universita e INFN Torino (IT))

APTS OPAMP 18_1_...

09:35 → 09:45 **CE65 status & plans** 10m

Speakers: Serhiy Senyukov (Centre National de la Recherche Scientifique (FR)), Szymon Bugiel (Centre National de la Recherche Scientifique (FR))

CE65_lab_01_2022....

09:45 → 09:55 **DPTS status & plans** 10m

- Commissioning in Trieste

Speakers: Matthew Daniel Buckland (Universita e INFN Trieste (IT)), Miljenko Suljic (CERN)

dpts-Trieste_2022-0...

09:55 → 10:00 **Irradiation status & plans** 5m Minutes

Speaker: Hartmut Hillemanns (CERN)

<u>Active groups:</u>

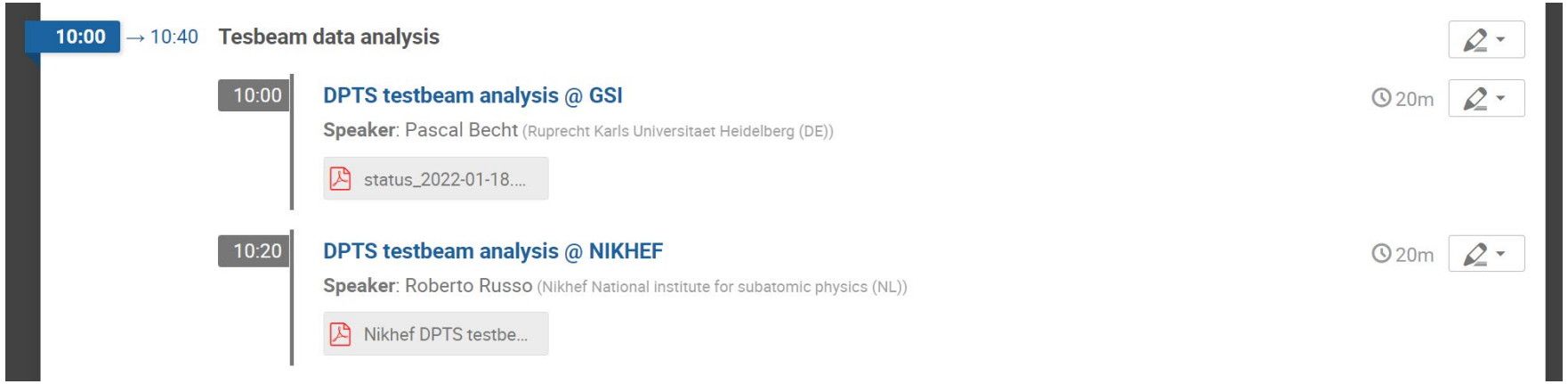
Test system design/production

- Cagliari
- Torino
- Strasbourg IPHC
- Trieste
- CERN

Chip tests:

- CERN
- Torino
- Strasbourg IPHC
- Trieste

MLR1 testing /2 : beam test data analysis



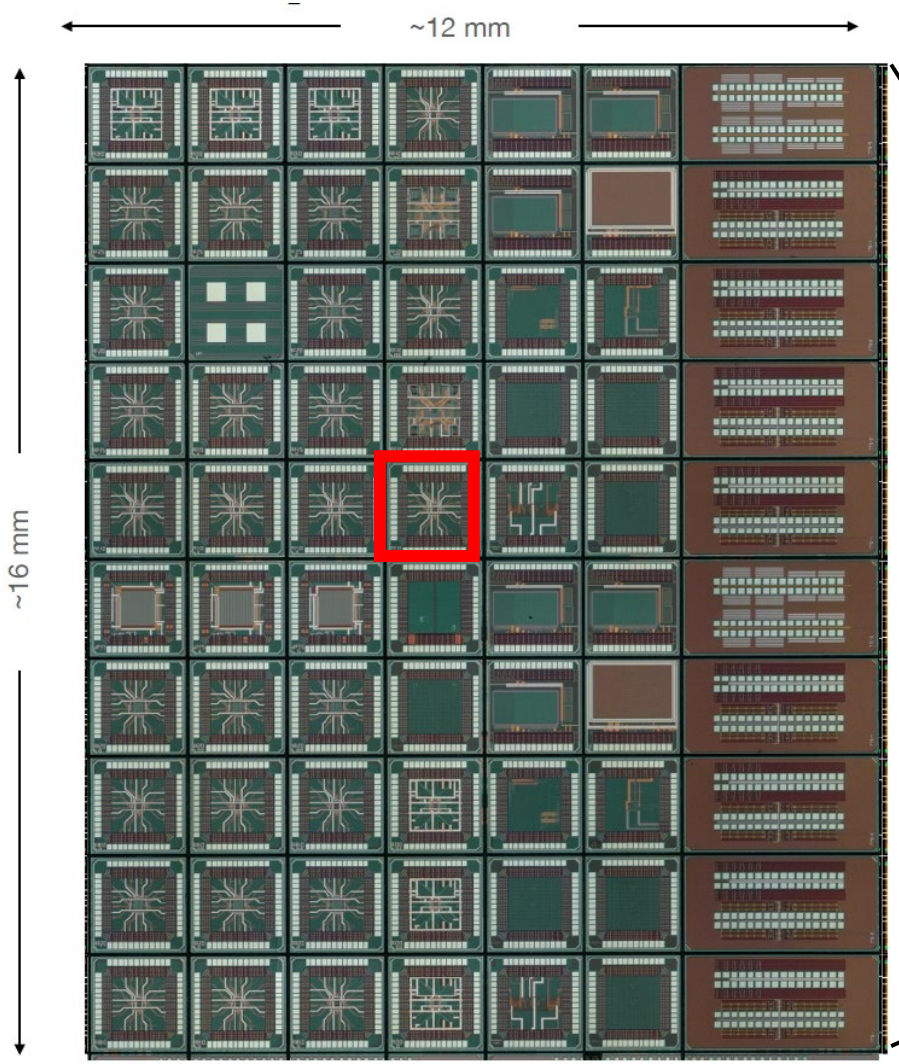
Data available from:

- DESY September 2021 - MLR1, Carbon foam, W-ALPIDE
- NPI September 2021 - DPTS SEU cross-section
- NPI October 2021 - DPTS irradiation & SEU cross-section
- PS October 2021 - MLR1
- SPS November 2021 - MLR1
- DESY December 2021 - MLR1
- NPI December 2021 - DPTS irradiation & SEU cross-section

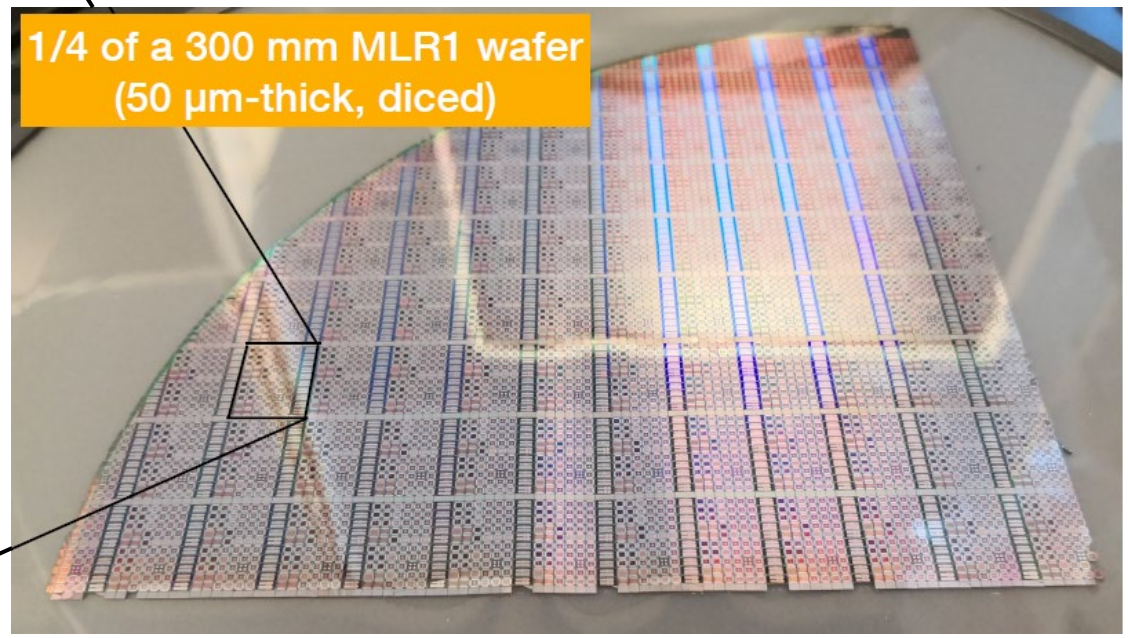
Active groups in beam test data analysis:

- GSI
- NIKHEF
  - Both these groups joined ITS3 recently

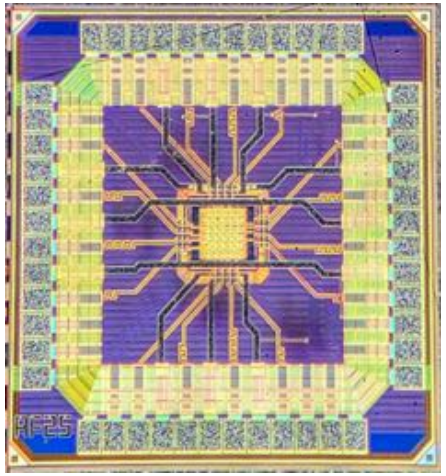
MLR1 reticle: 60 chips (+ 10 transistor test structures)



- Pixel test structures
- Pixel matrices
- Radiation test structures
- Analogue building blocks

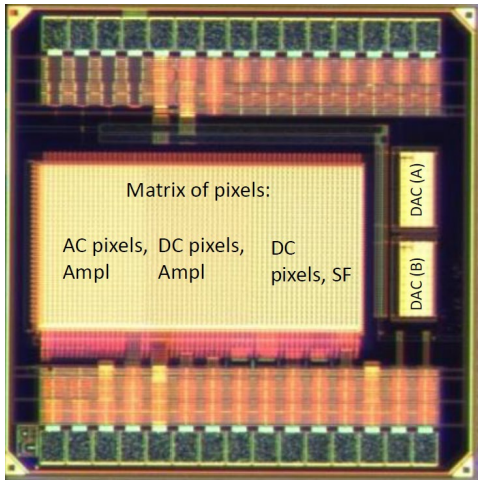


APTS, CE65, DPTS



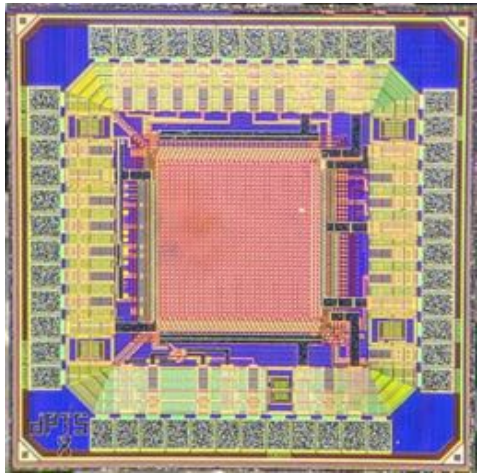
APTS

- Most “simple” chip
- 4x4 pixel matrix
- 10, 15, 20, 25 µm pitches
- Different pixel and amplifier architectures
- Direct analogue readout of all 16 pixels



CE65

- “Large” area chip with analogue rolling shutter readout
- 64x32 pixel matrix
- 15 µm pitch
- 3 pixel architectures
- 2 currents DACs on same die



DPTS

- Most “complicated” chip
- 32x32 pixel matrix
- 15 µm pitch
- Asynchronous digital readout

Chip variant phase space

APTS

#	Pitch (um)	Buffer	Coupling	Process
1	10	SF	DC	std
2	10	SF	DC	mod
3	10	SF	DC	gap
4	15	SF	DC	std
5	15	SF	DC	mod
6	15	SF	DC	gap
7	20	SF	DC	std
8	20	SF	DC	mod
9	20	SF	DC	gap
10	25	SF	DC	std
11	25	SF	DC	mod
12	25	SF	DC	gap
13	10	SF	AC	std
14	10	SF	AC	mod
15	10	SF	AC	gap
16	20	SF	AC	std
17	20	SF	AC	mod
18	20	SF	AC	gap

#	Pitch (um)	Buffer	Coupling	Process
19	10	SF+amp	DC	std
20	10	SF+amp	DC	mod
21	10	SF+amp	DC	gap
22	20	SF+amp	DC	std
23	20	SF+amp	DC	mod
24	20	SF+amp	DC	gap
25	10	SF+amp	AC	std
26	10	SF+amp	AC	mod
27	10	SF+amp	AC	gap
28	20	SF+amp	AC	std
29	20	SF+amp	AC	mod
30	20	SF+amp	AC	gap
31	10	OPAMP	DC	std
32	10	OPAMP	DC	mod
33	10	OPAMP	DC	gap
34	10	OPAMP	AC	std
35	10	OPAMP	AC	mod
36	10	OPAMP	AC	gap
37	10	SF mux	DC	gap
38	20	SF mux	DC	gap

CE65

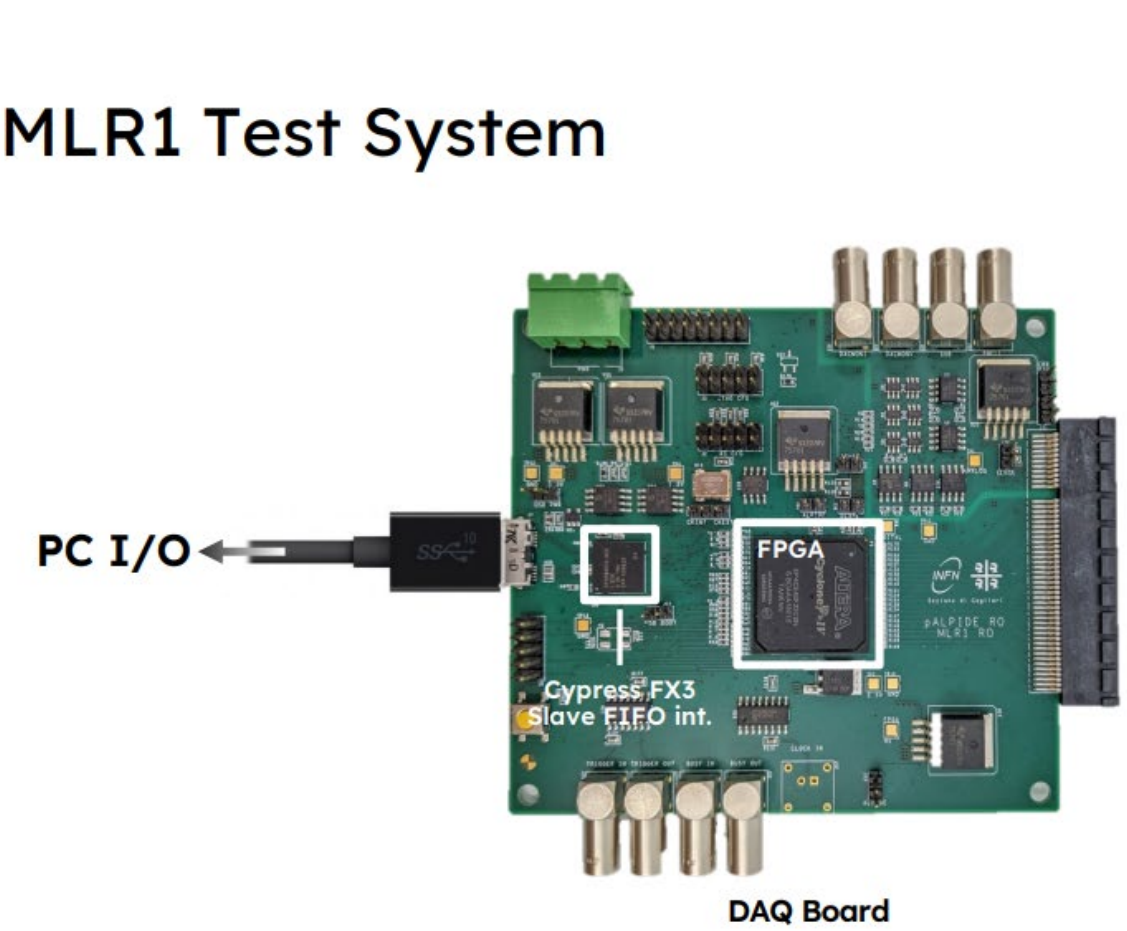
#	Pitch (um)	Buffer [coupling]	Process
A	15	Amp [AC], Amp [DC], SF [DC]	std
B	15	Amp [AC], Amp [DC], SF [DC]	gap
C	15	Amp [AC], Amp [DC], SF [DC]	Mod
D	25	Amp [AC], Amp [DC], SF [DC]	std

DPTS

#	Pitch (um)	Variant
1	15	Base
2	15	Column cross connect
3	15	column cross connect, shorted DVSS AVSS

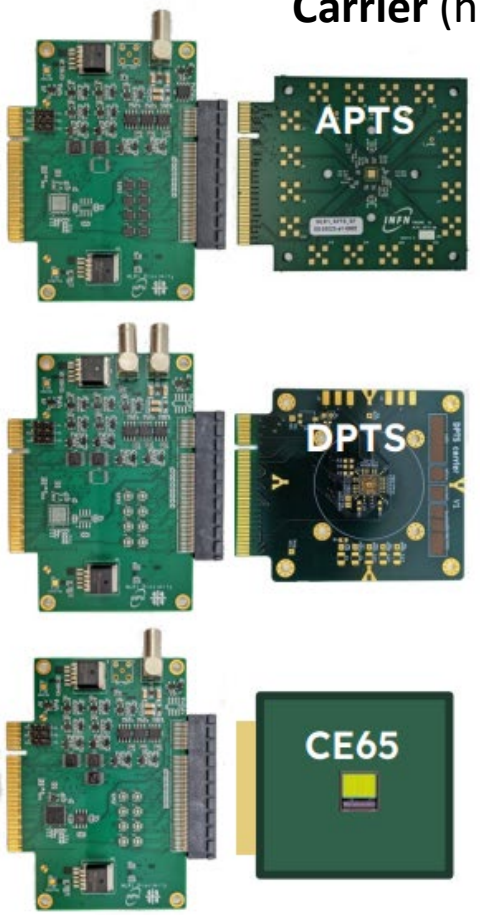
× 4 splits

Common test system: DAQ + Proximity + Carrier

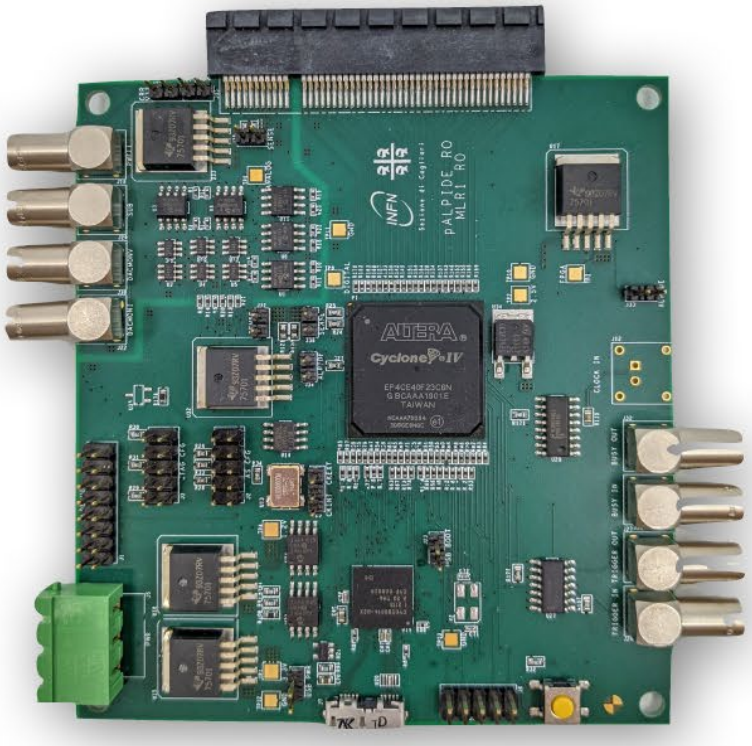


Proximity

Carrier (hosting the chip)



MLR1 DAQ board



DPTS Proximity Card

APTS SF Proximity Card

CE65 Proximity Card

APTS OA Proximity Card

20 DAQ + 20 Proximity cards delivered 17.08.

Commissioning ongoing at INFN Cagliari (FW/SW/all variants), CERN (APTS/DPTS), IPHC (CE65)

Test system availability

Second Batch Production Status

Hardware	APTS-OA	APTS-SF	CE65	DPTS
DAQ Boards	30x, PCBs at FEDD for mounting			
Proximity Cards	No 2nd batch	20x PCBs at FEDD for mounting Due 2nd half of Feb	5x PCBs ready to be sent to FEDD	5x PCBs ready to be sent to FEDD
Carrier Cards	60x PCBs due 1st week of Feb (CIRLY)	250x Due 11 Feb	No 2nd batch	No 2nd batch

- After 'second batch' production:
  - Boards will be just enough for groups currently involved + spares
  - In the first phase, only ITS3 groups will access the boards
    - Trieste, Liverpool, Daresbury, probably LBL, will be able to obtain some
  - If spares stay available / when a new production is completed:
    - Distribution to other EIC SC groups
    - Decision to be taken at the ITS3 project level

In the meantime… how to join testing campaign

- Agree on a training period with a group already working on one of the chip

- Join the experienced group for a few weeks to work with them
  - Tests are still in the development/debugging phase → very convenient for learning!
  - Trainee is preferably an experienced postdoc/researcher
  - Trainee can also be a student, provided that there is an experienced supervisor at the home institute

- In the meantime, procure the necessary equipment for testing at the home institute:
  - PC / Raspberry Pi
  - ITS3 test system (subject to availability – see previous slide)
  - Electronics laboratory capabilities
  - Radioactive sources / laser system
  - Oscilloscope with BW>1GHz (only for some tests)
  - Wire bonding facility (optional)

- *Alternative option: temporar relocate member(s) at host institute*

MLR1 Task List: APTS SourceFollower

APTS SF characterisation	Lab measurements		-	-	Sensor characterisation in the laboratory.
		Software	?	?	Develop software for signal extraction and clusterisation.
		Noise	?	?	Study the noise of the test system, sensor, RTS.
		Calibrate	?	?	Calibrate conversion and pulsing capacitances (55-Fe).
		Charge collection	?	?	Study the response to 55-Fe X-rays. X different variants X different biases.
		Temperature dependence	?	?	Characterise sensor response as function of temperature.
		Separating PWELL and SUB	?	?	Study the behaviour with separate PWELL and SUB.
	Testbeam analysis		-	-	Analyse the testbeam data.
		EUDAQ converter	Mauro	Nov 2021	Write, test and verify APTS converter.
		Charge collection	?	?	Study charge collection MPV and charge sharing. X different variants X different biases.
		Efficiency	?	?	Efficiency vs biasing parameters / threshold for multiple chips.
		Spatial resolution	?	?	Spatial resolution vs biasing parameters / threshold for multiple chips.

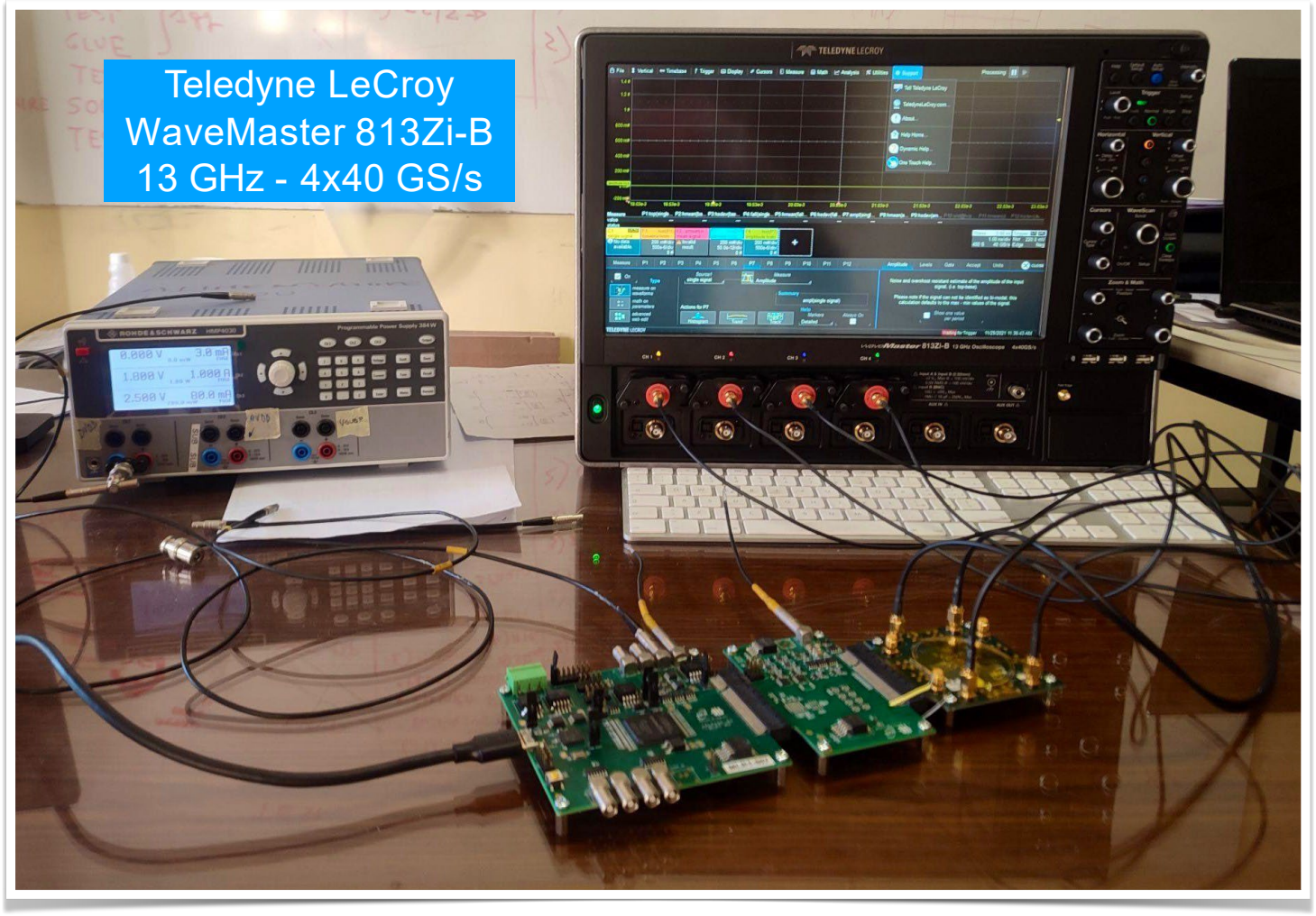
MLR1 Task List: APTS OpAmp

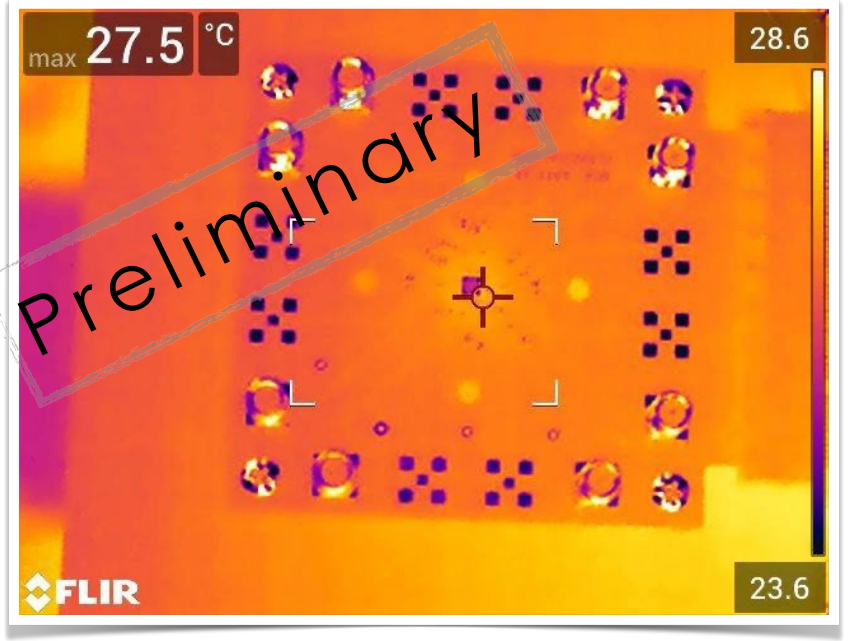
APTS OA characterisation	Lab measurements		-	-	Sensor characterisation in the laboratory.
		Software	?	?	Develop software for signal extraction and clusterisation.
		Noise	?	?	Study the noise of the test system, sensor, RTS.
		Pulsing	?	?	Study response to pulsing.
		Calibrate	?	?	Calibrate conversion and pulsing capacitances (55-Fe).
		Charge collection	?	?	Study the response to 55-Fe X-rays. X different variants X different biases.
		Laser response	?	?	Characterise all aspects of the sensor response to laser beam.
	Testbeam analysis		-	-	Analyse the testbeam data.
		EUDAQ SW	?	?	Write, test and verify Producer and Converter.
		Efficiency	?	?	Efficiency vs biasing parameters / threshold for multiple chips.
		Time resolution	?	?	Study time response to MIP beam.

MLR1 Task List: DPTS

DPTS characterisation	Commission DAQ board based test system		Trieste	2021	Commission the MLR1 DAQ board + DPTS Proximity for use with DPTS.
	Lab measurements		-	-	Sensor characterisation in the laboratory.
		Response vs front-end bias	?	?	Threshold, noise, Fake Hit Rate, TOT, Rise time... as a function of all biasing parameters. Subset of pixels, multiple chips (variants, irradiation...).
		Noise	?	?	Understand noise sources and behaviour.
		Dead pixels	?	?	Study pixels unresponsive to pulsing and external stimuli.
		55-Fe	?	?	Study the response to 55-Fe X-rays and try to use it to calibrate the pulsing capacitance/threshold.
		Temperature dependence	?	?	Characterise sensor response as function of temperature.
		Separating PWELL and SUB	?	?	Study the behaviour with separate PWELL and SUB.
		Monitor pixel output	?	?	Characterise AOUT pulse as function biasing parameters.
		Laser response	?	?	Characterise all aspects of the sensor response to laser beam.
	Testbeam analysis		-	-	Analyse the testbeam data.
		Efficiency	?	?	Efficiency vs biasing parameters / threshold for multiple chips.
		Spatial resolution	?	?	Spatial resolution vs biasing parameters / threshold for multiple chips.
		Time resolution	?	?	Study time response to MIP beam.

APTS OA: commissioning started in Torino





10 AO10 sensors in Torino:

- 4x from split 1
- 6x from split 4

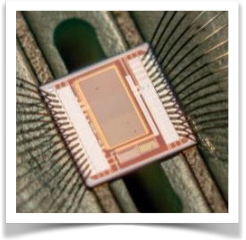
Other flavours to be bonded

APTS OA: first response

Single and mean signals from pixels 3, 4, 11 & 12 at Vsub = Vpwell = 0V, VH = 1200 mV, others nominal

Measure	P1:fall(F5)	P2:base(F5)	P3:top(F5)	P4:fall(F6)	P5:base(F6)	P6:top(F6)	P7:fall(F7)	P8:base(F7)	P9:top(F7)	P10:fall(F8)	P11:base(F8)	P12:top(F8)
value	882 ps	173.622 mV	229.213 mV	783 ps	185.938 mV	241.269 mV	908 ps	179.918 mV	235.521 mV	837 ps	169.496 mV	225.847 mV
status	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

CE65: ^{55}Fe lab characterisation

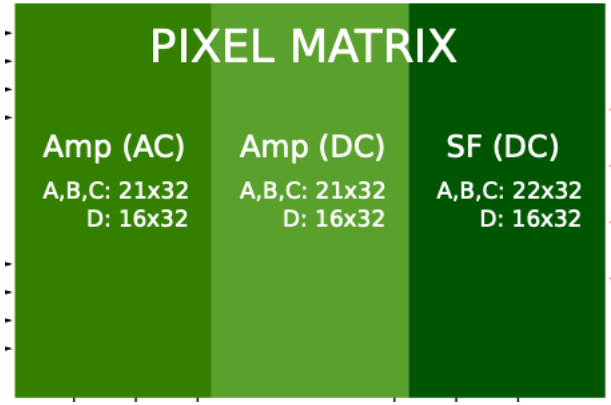


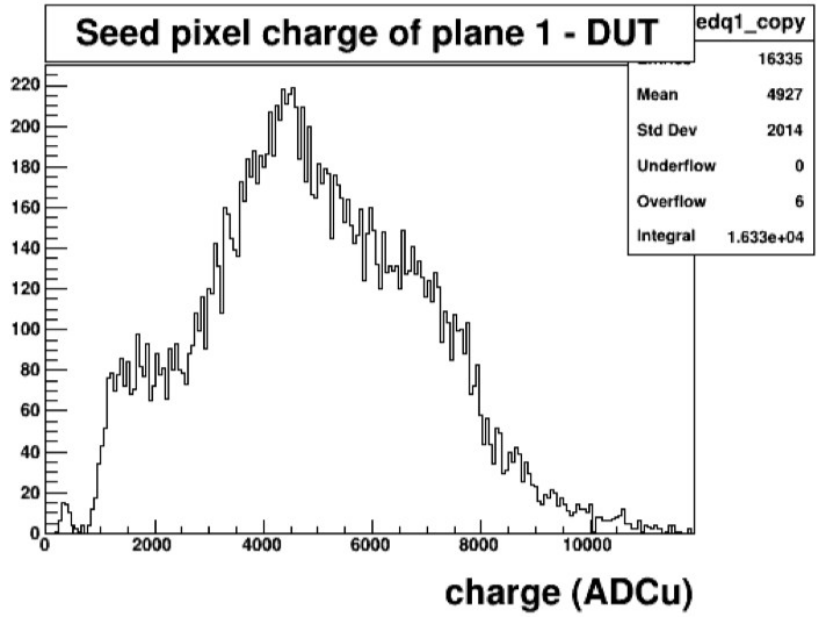
SPLIT	A	B	C	D
1				
4				

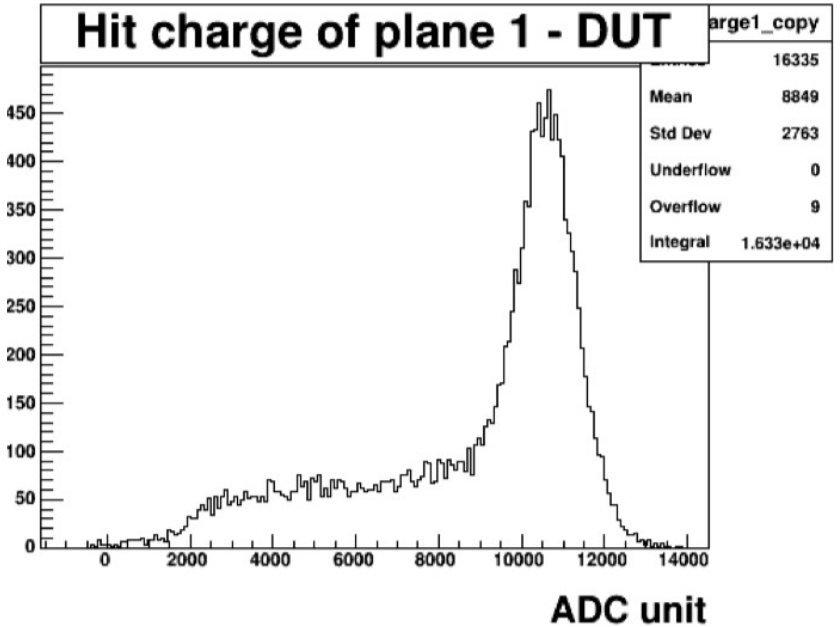
- operational
- no signs of life
- not tested

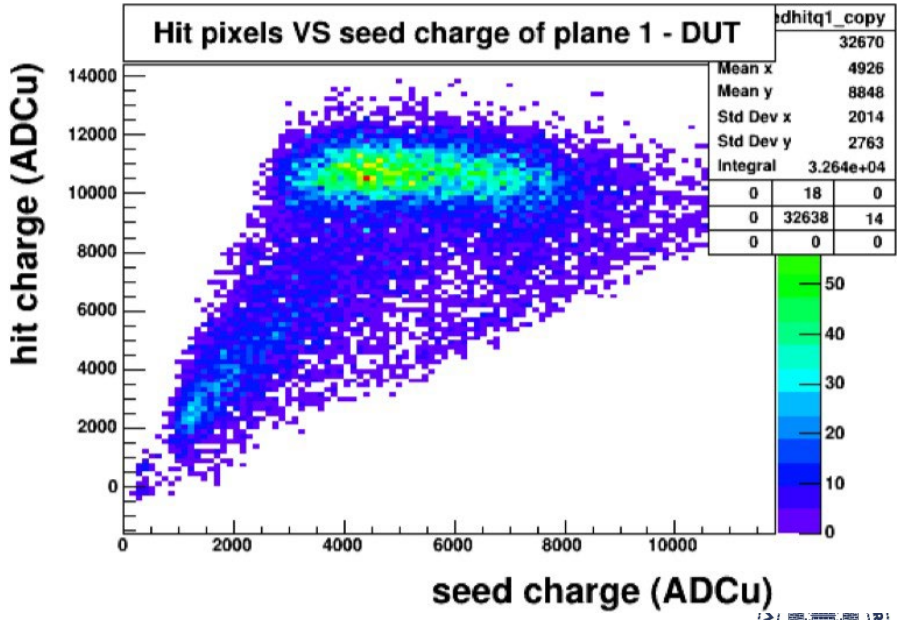
CE65 Variants:

- **A:** pitch = 15 um
  diode – simple n well
- **B:** pitch = 15 um
  diode – deep n with gaps
- **C:** pitch = 15 um
  diode – blanket deep n
- **D:** pitch = 25 um
  diode – simple n well

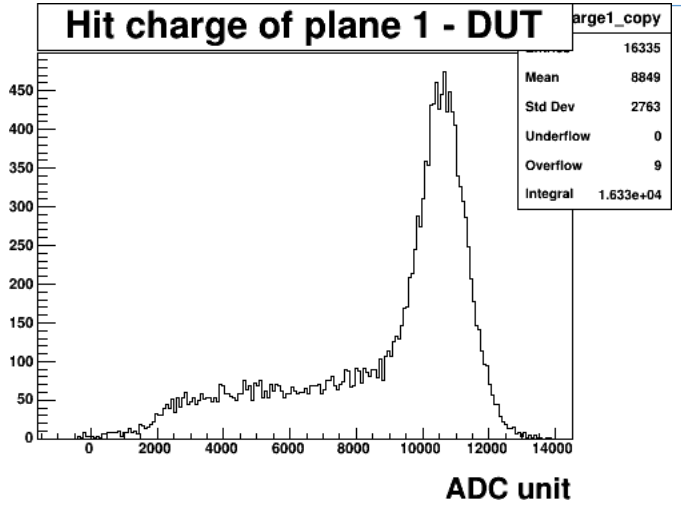




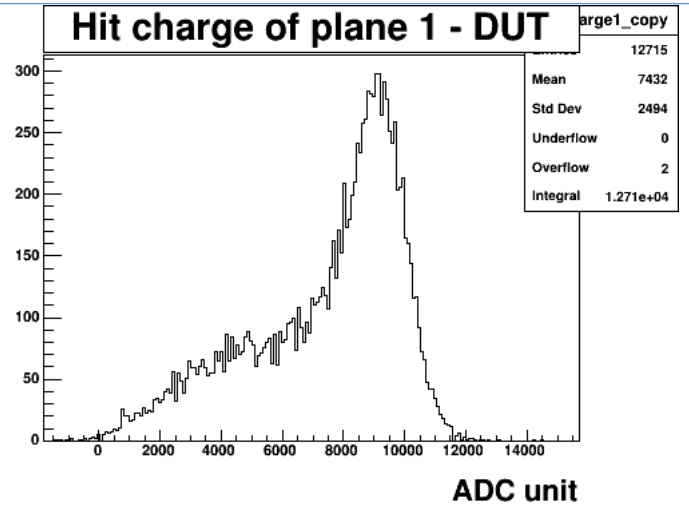




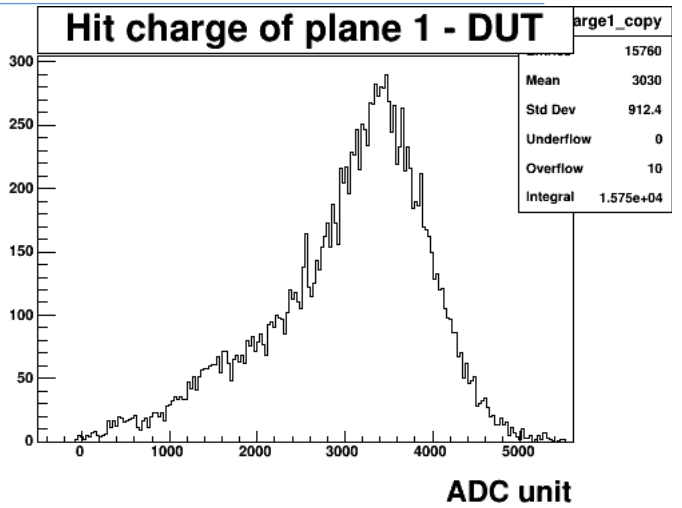
CE65: Vbb influence, variant A, DC amp, split 4



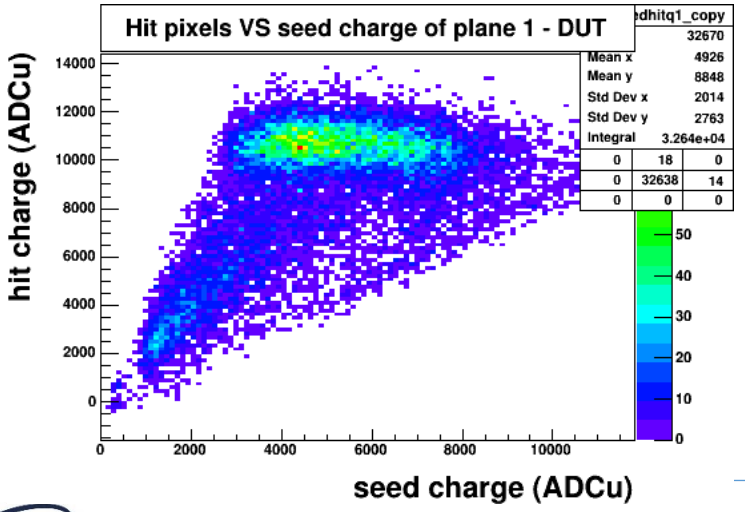
Vbb = 0 V

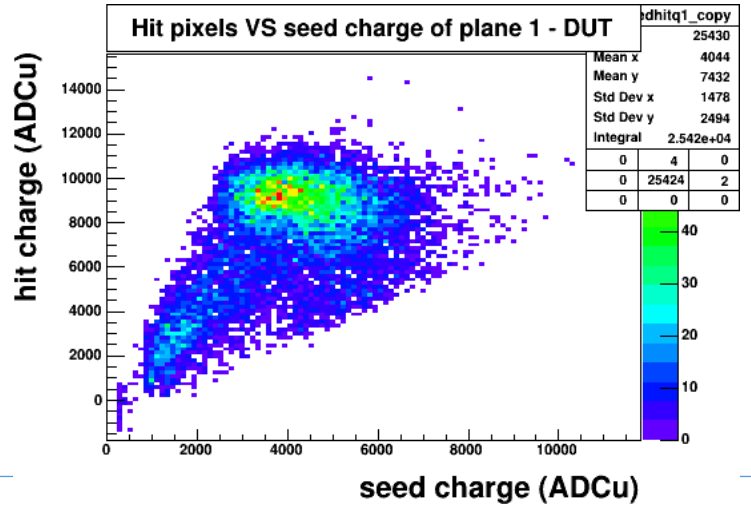


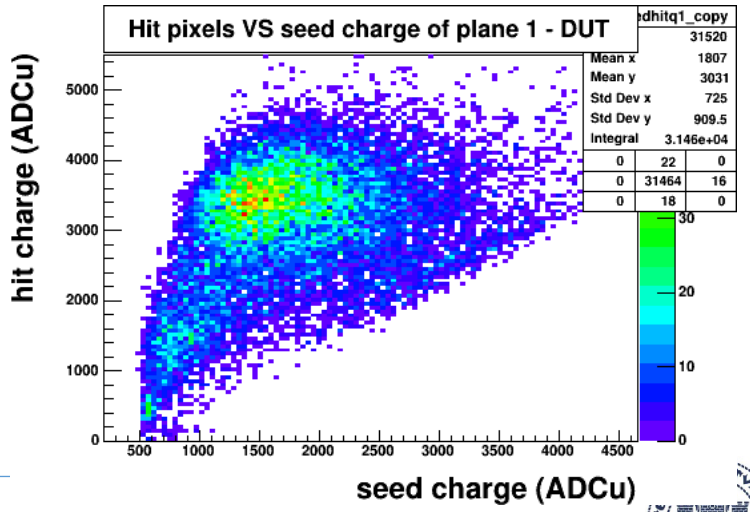
Vbb = -0.6 V



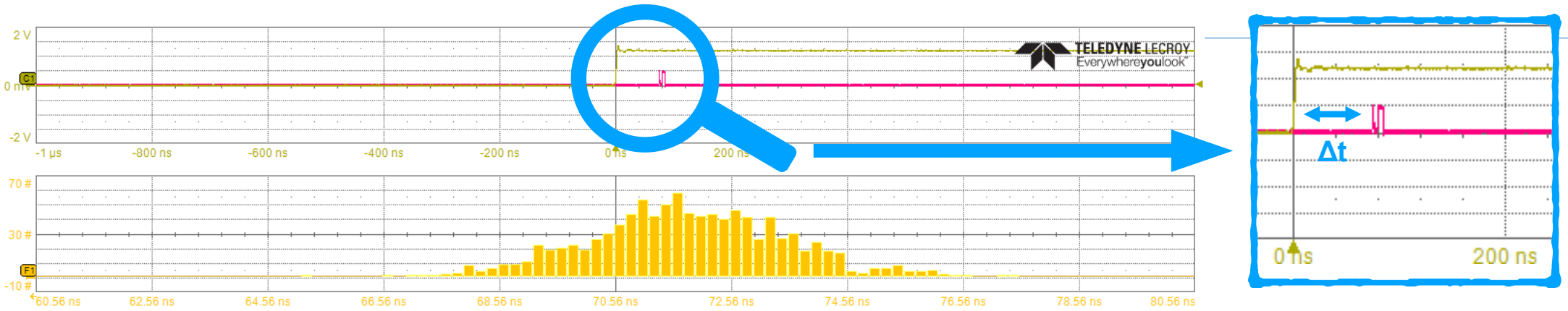
Vbb = -1.2 V





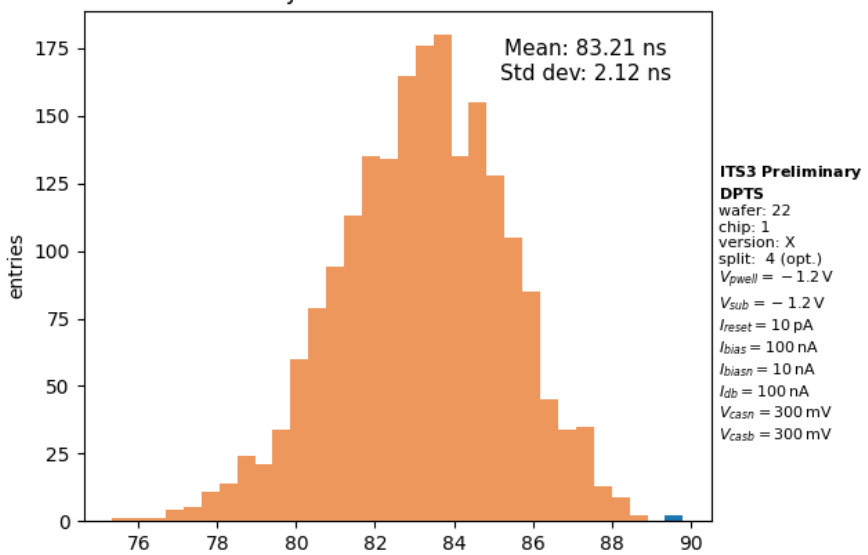


DPTS: Jitter measurement



Measure	P1:ddelay(C1,C2)	P2:freq(C1)	P3:- - -	P4:- - -	P5:- - -
value	73.624 ns				
mean	71.869 ns				
min	65.198 ns				
max	77.553 ns				
sdev	1.715 ns				
num	2.039e+3				
status	✔				

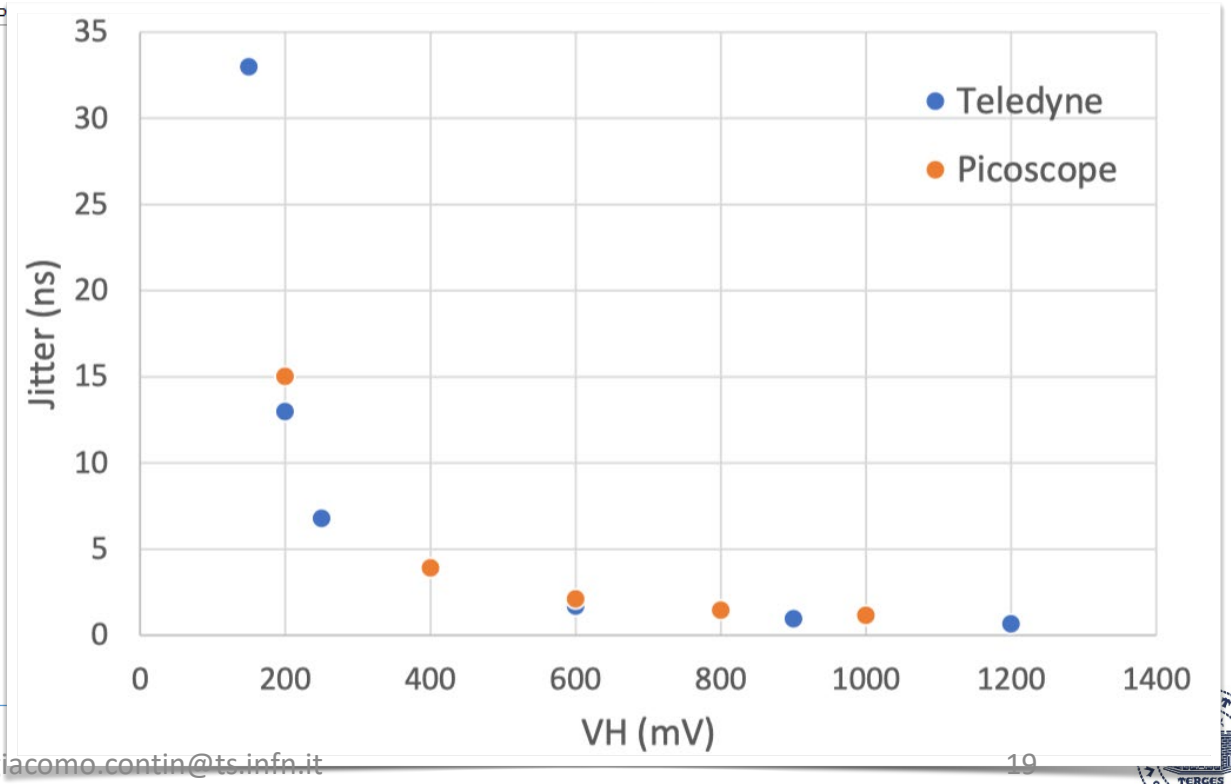
Jitter VH = 600 mV



Teledyne LeCroy Waverunner 9104, 1 GHz

Picoscope 6824E, 500 MHz

ITS3 Preliminary
DPTS
wafer: 22
chip: 1
version: X
split: 4 (opt.)
$V_{pwell} = -1.2$ V
$V_{sub} = -1.2$ V
$I_{reset} = 10$ pA
$I_{bias} = 100$ nA
$I_{biasn} = 10$ nA
$I_{db} = 100$ nA
$V_{casn} = 300$ mV
$V_{casb} = 300$ mV



Link to WP3 presentation

Practical example of new participation

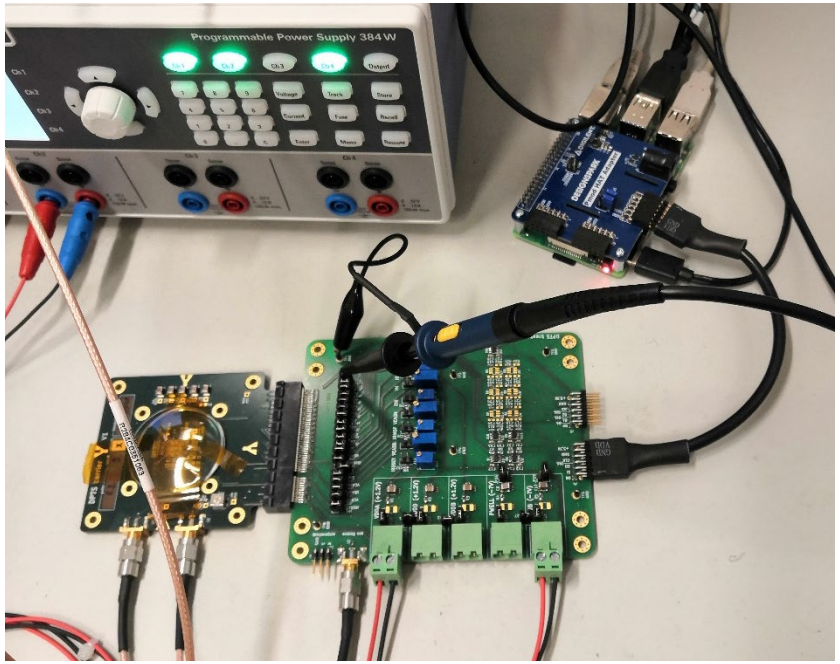
- Postdoc sent to CERN for 2 weeks to work with ITS3 experts
  - Previous experience with ALPIDE testing and electronics
  - Full hands-on sessions to catch up with DPTS system and tests
  - Guided hardware debugging
  - Independent script/procedure development / hardware improvement

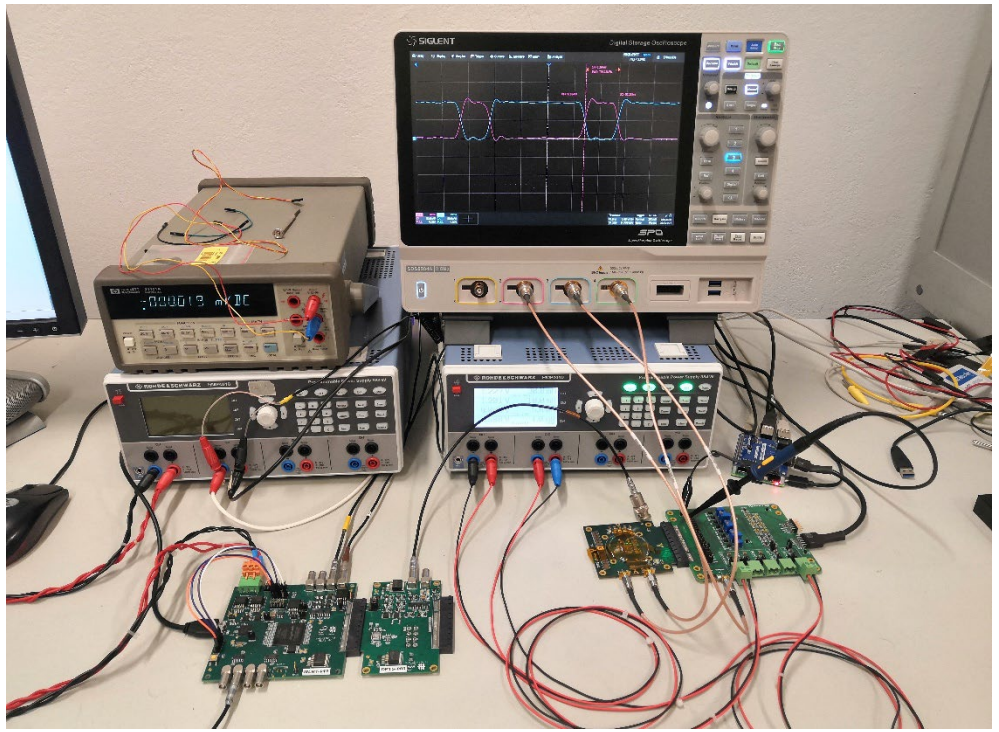
- In the meantime at the home institute:
  - Existing equipment for ALPIDE testing and general laboratory capabilities
  - Purchased large bandwith oscilloscope
  - Set up PC/Raspberry PI, power supplies and connections as needed
  - In contact with CERN to verify setup replica

- The postdoc is back at the home Institute:
  - Working with supervisors, training supervisors and students
  - Custom DPTS test system brought back from CERN with 1 working chip
  - ~10 DPTS chips + carriers: to be wire bonded locally
  - Received an official DPTS test system, to be troubleshooted and integrated w/ software/firmware

Current tasks back at the Home institute

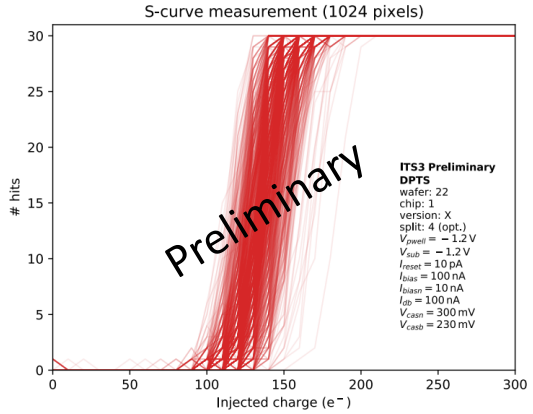
- Reproducing DPTS threshold scans with local system
  - Replicating custom DPTS test system
  - Implementing software classes for Siglent oscilloscope
  - Optimizing algorithm/scripts



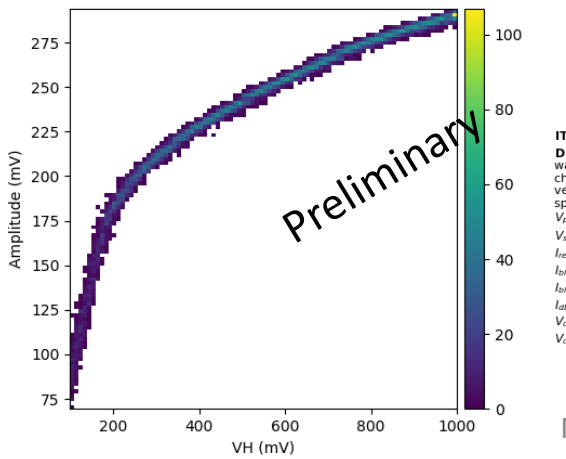


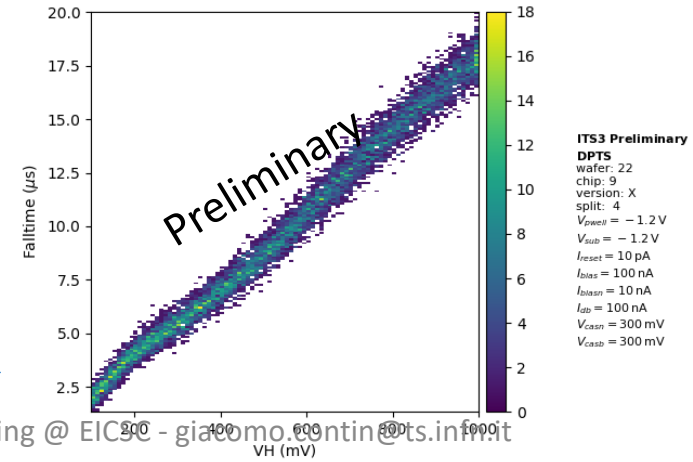
Current tasks back at the Home institute

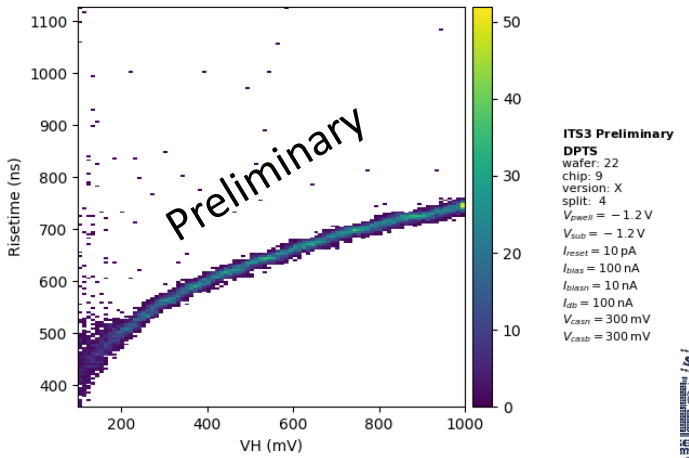
- Calibration: Threshold scans



- Developing measurement procedure/code: Analog output Vs pulse height

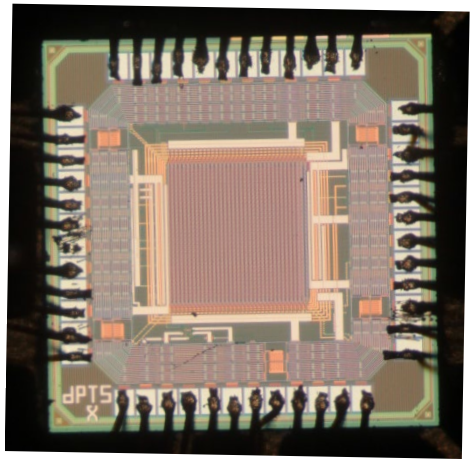


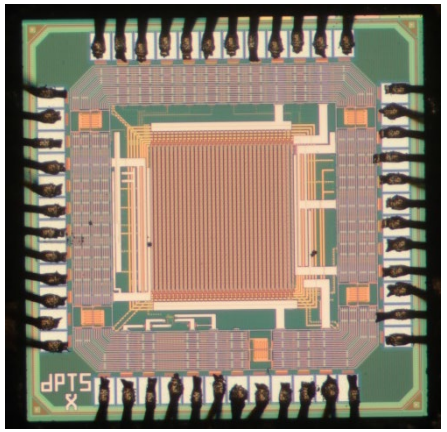




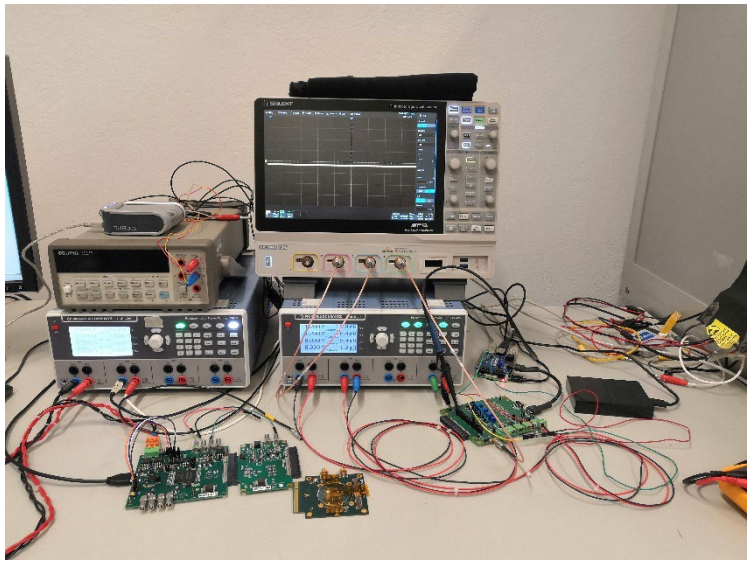
Current tasks back at the Home institute

- Commissioning the DPTS on carrier wire-bonding
  - Adjust force and positioning
  - Wire-bond different flavors/versions for full scan of parameters



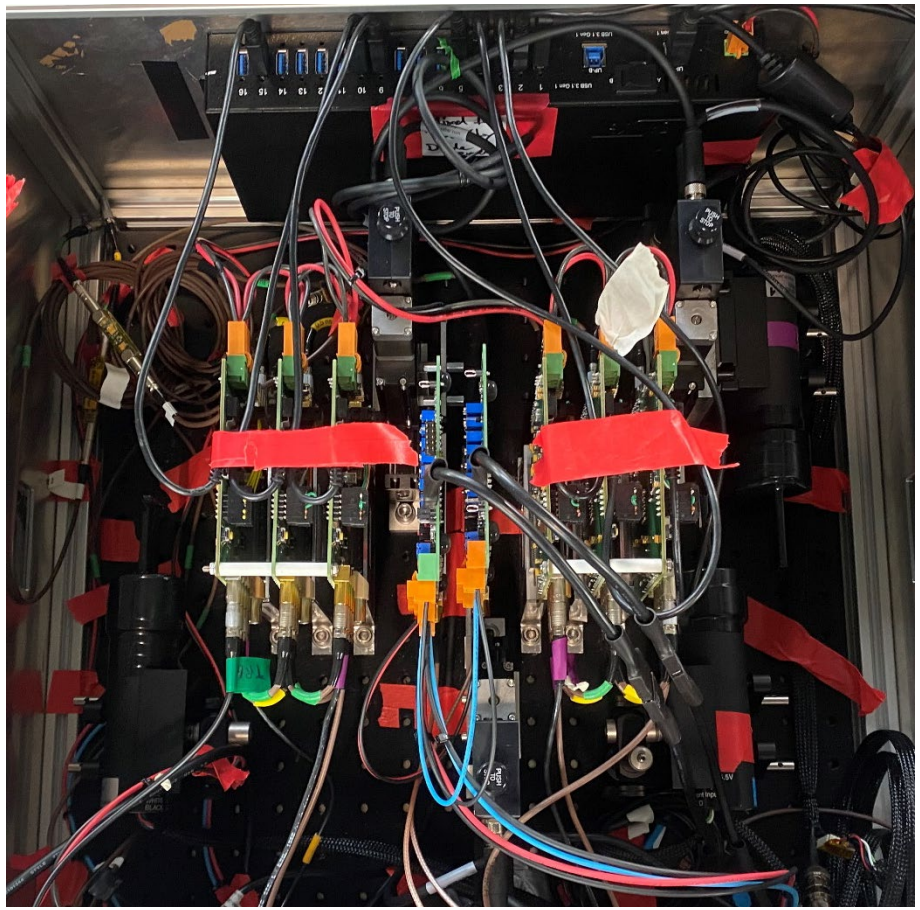


- Commissioning official DPTS DAQ-based system
  - In collaboration with firmware/software developers
  - Comparison with custom DPTS test system behavior

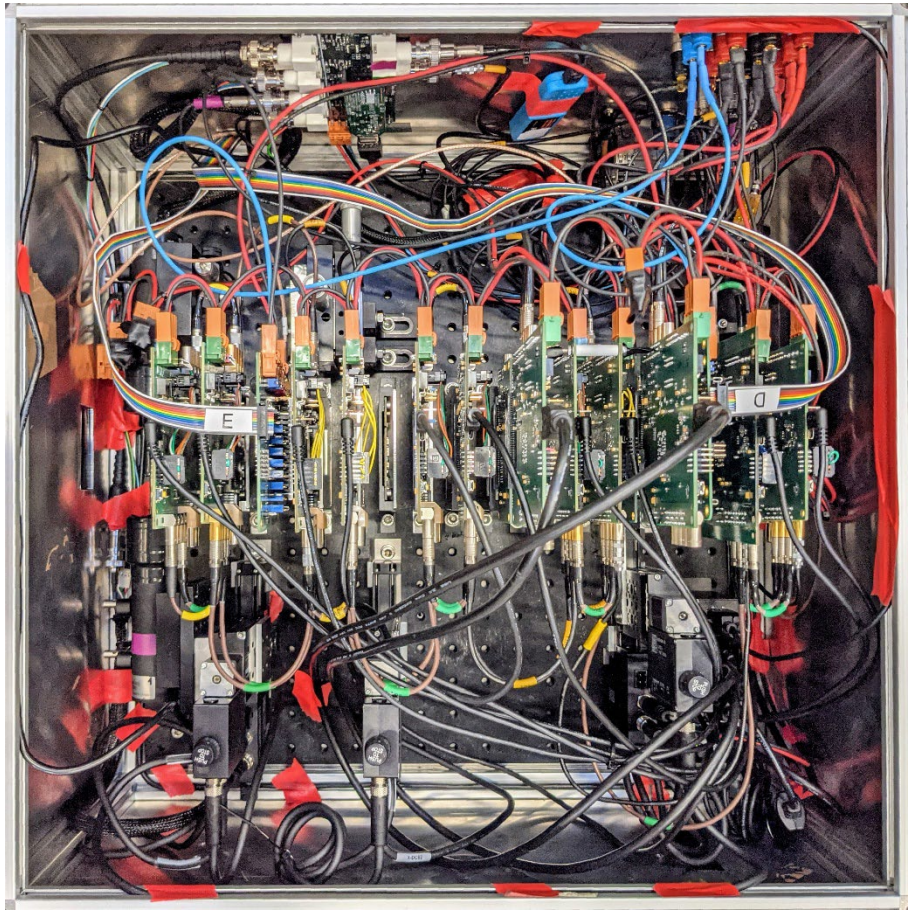


Beam test campaigns for MLR1 chips

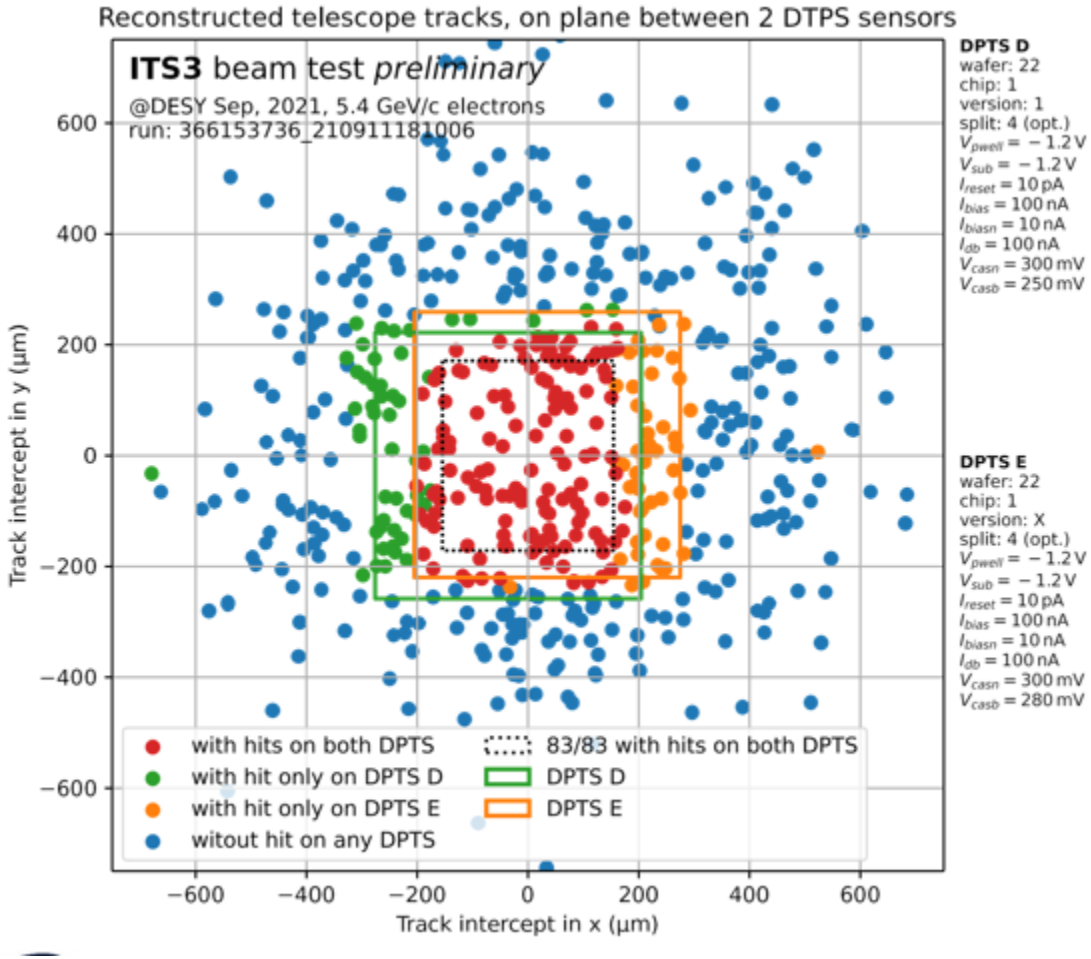
DESY September 2021: DPTS



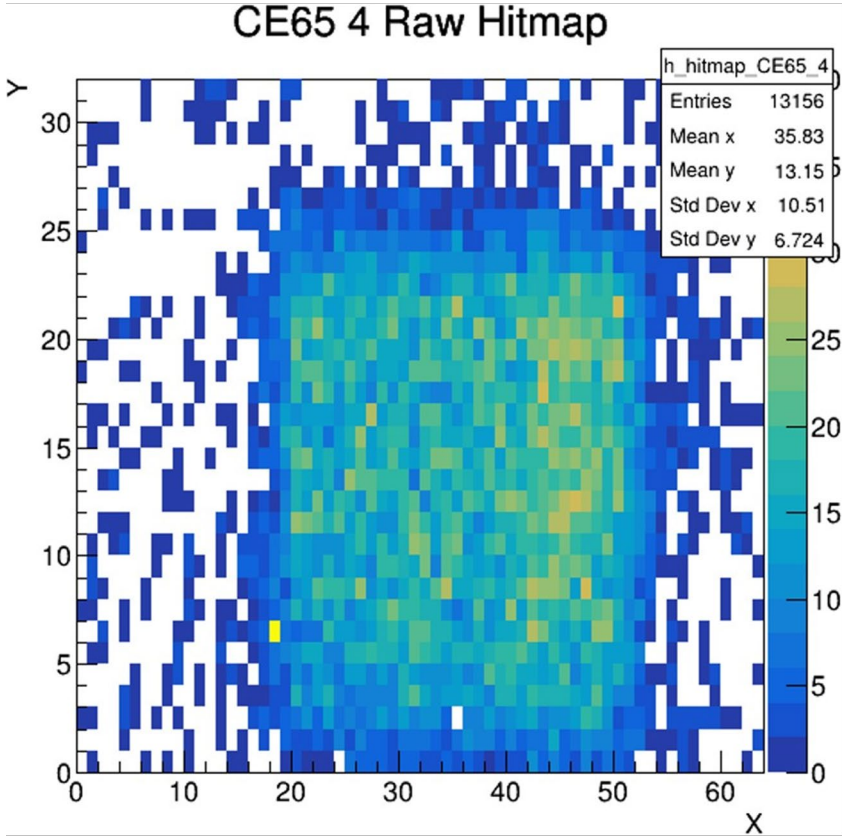
CERN PS Oct/Nov 2021: APTS, DPTS, CE65



Preliminary results from beam test data analysis



Sneak peak from DESY testbeam



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Participation in beam test data analysis

- Very welcome (at the moment understaffed)
- Does not require test system / lab equipment
- Can be done from remote
- Does require deep training
  - EUDAQ telescope framework
  - Beam test data format
  - Chip data format and interpretation
- Participation in beam test data taking is also welcome, if followed/preceded by data analysis / chip testing in laboratory

EIC SC Institute participation summary

Institute	Contact person	Also ALICE ITS3	Requested a Test system	Has a test system	Active Tasks
Birmingham	Laura Gonella	no	yes		
RAL	Fergus Wilson	no	yes		
Liverpool	Marielle Chartier	yes	yes		
Lancaster	Harald Fox	no	yes		
Brunel	Liliana Teodorescu	no			
Daresbury	Marcello Borri	yes	yes		
University of Chicago Illinois	Zhenyu Ye	no			
CAPADS Prague	Lukáš Tomášek	no	yes		
ORNL	Jo Schambach	no			
LBNL/UC	Barbara Jacak	yes	yes		
JLAB	Brian Eng	no	yes		
INFN Trieste	Giacomo Contin	yes	n.a.	yes	DPTS, APTS, Bent ALPIDE characterization

Conclusions

- First step: discussing with ITS3 leaders the insitute participation

- Effective contribution to testing can start immediately
  - **Training with experts at host institution (CERN or other groups)**
  - Laboratory facility and test system set up at the home institute
  - Independent work with local supervision
  - About 2 months preparation before starting independent work

- Effective contribution to data analysis can start immediately
  - **Training with experts to be agreed**
  - Can be done remotely, but a period ‘face-to-face’ is more effective