Powering the ATLAS ITk Strip Tracker

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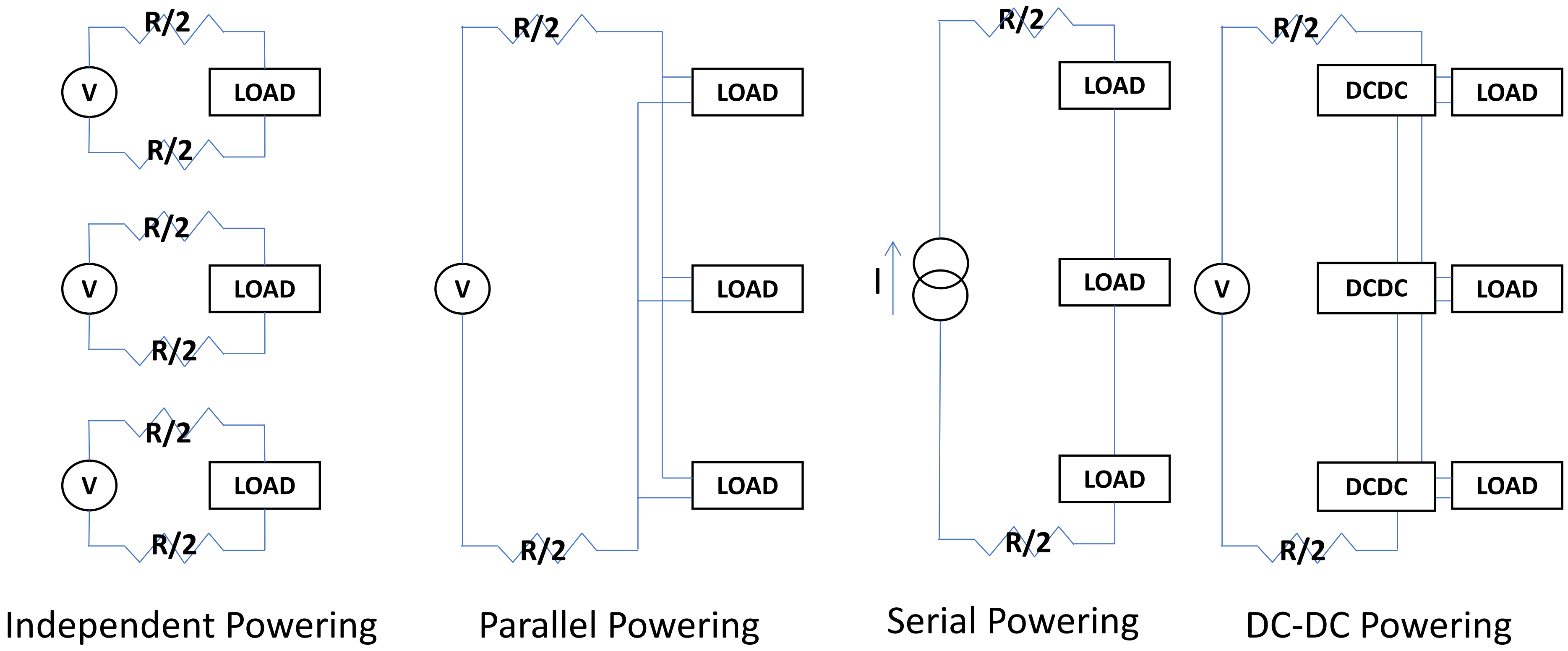
28/02/2022

Overview

- Introduction
  - powering options and initial prejudices
- Early ITk Strip Stave Prototypes with 250nm chipset
  - with DC-DC and Serial Powering
- Final Stave Powering Architecture
  - with on-module DC-DC conversion
- Full ITk Strip Power Chain
  - with additional DC-DC stage
- How does this fit with EIC?
  - first thoughts about how to take forward the work done at LBNL

Powering Schemes and Cables



Losses in off-detector cabling of total resistance R for n loads drawing current I:

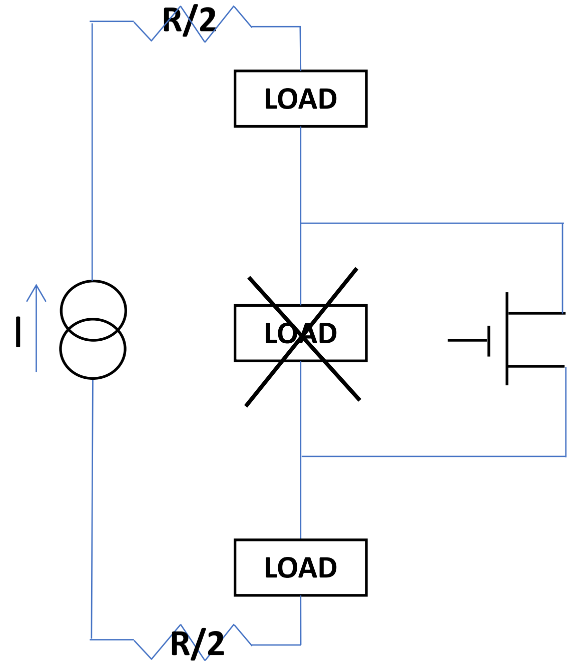
$P = nI^2R$ $P = n^2I^2R$ $P = I^2R$ $P = n^2I^2R / r^2$

where ratio r = Vin/Vout

Serial Powering and DC-DC Point of Load conversion offer more efficient cable usage than Independent or Parallel Powering. *Total system efficiency will be lower as this depends upon the efficiencies of bulk supplies, DC-DC converters & shunts which are neglected here.*

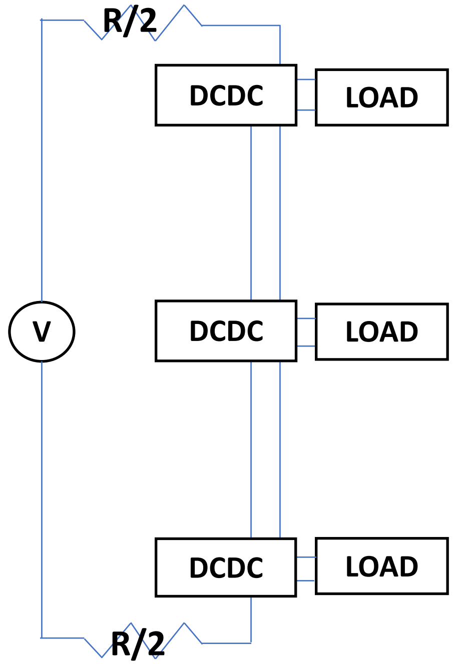
Serial Powering

- Elements of a serially powered system
  - Current Source
  - Shunt regulator / transistor within the load
  - Bypass shunt (to protect against failure of load)
- Current must be sufficient to cover the peak demand of the biggest load in the chain
  - Best suited to chains of identical devices
- Intrinsically low mass, needs little if any extra space
  - Useful for tracking detectors (especially pixels)

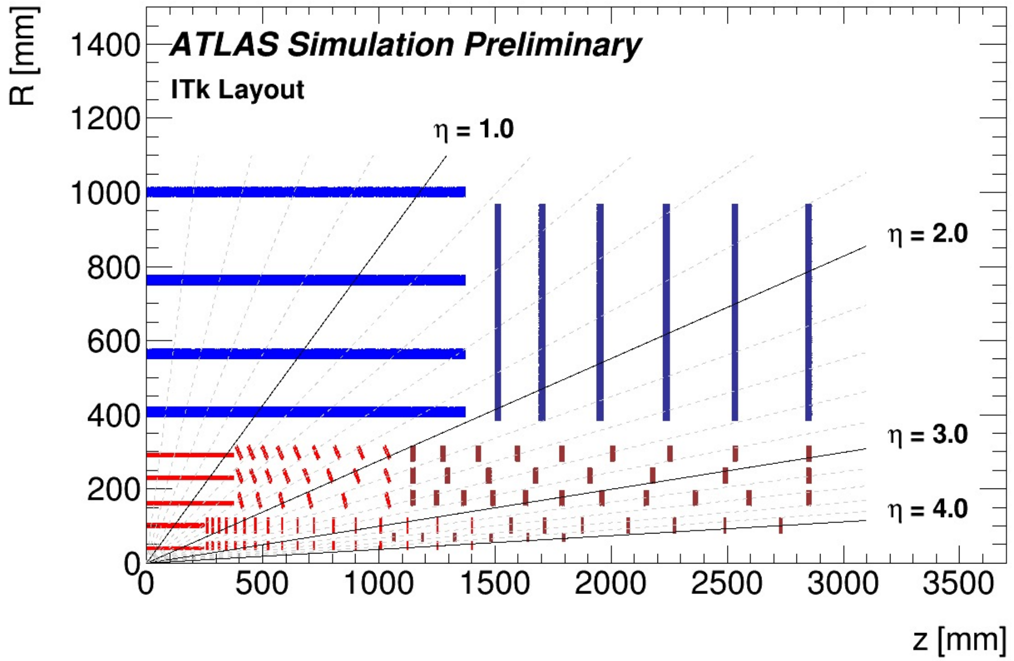


DC-DC Point Of Load Conversion

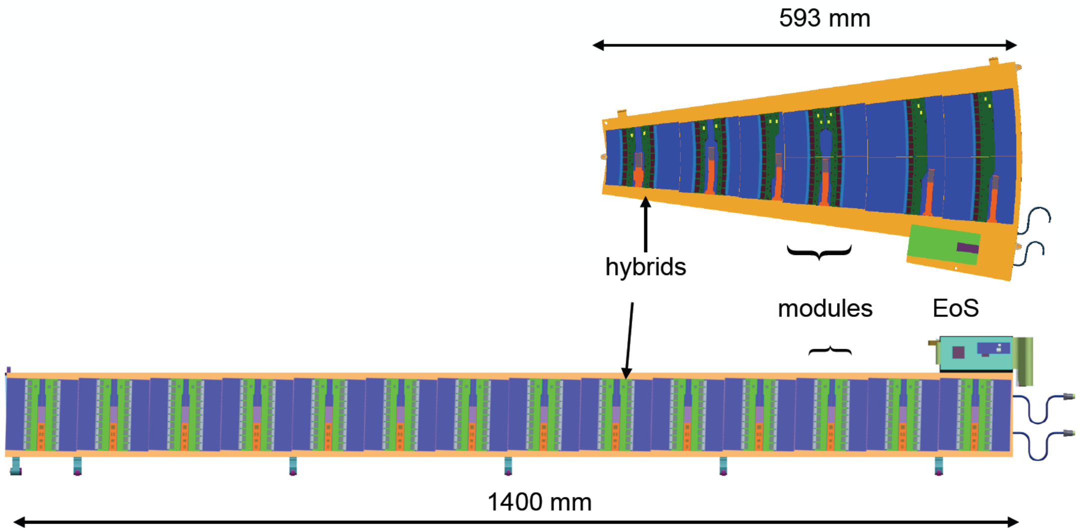
- Commercially available converters use
  - ferrite-cored inductors
    - may not be used in magnetic fields
  - not radiation hard
    - May not be used in HL-LHC environment
- We need custom converters
  - air-cored inductors
  - radiation hardened ASIC
  - *for tracker applications: low mass design*



ATLAS ITk Strip Layout



Discs are tiled with "petals"



Barrels are tiled with "staves"

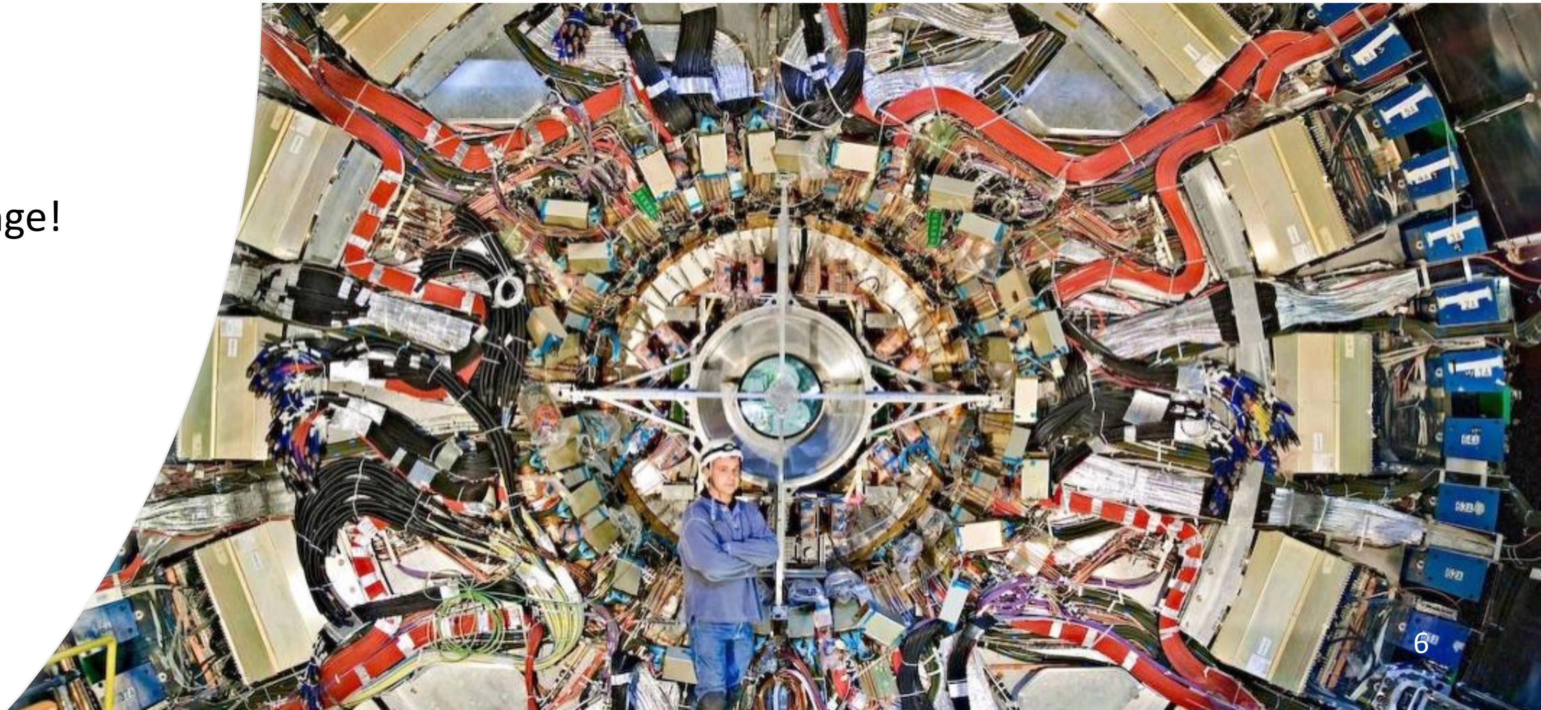
Strip layers are shown in blue. Comprises four barrels and two endcaps of six discs each.

Two inner barrels have Short Strips (2.4 cm strips)
Two outer barrels have Long Strips (4.8 cm strips)

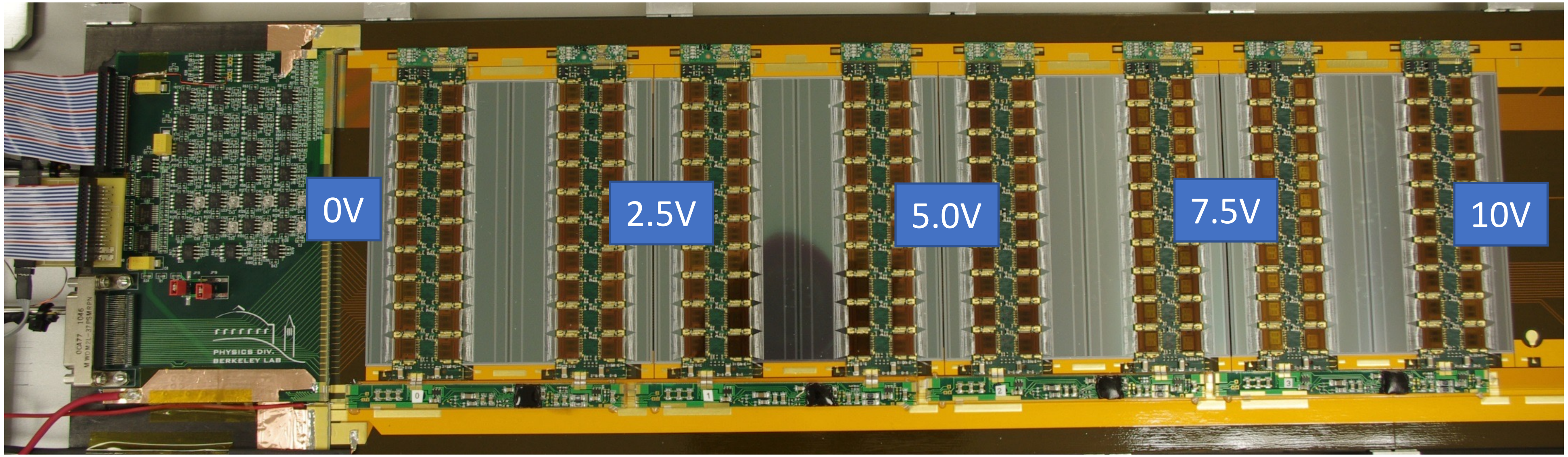
Most material shown today will relate to the Short Strip Staves used in the barrel region.

ATLAS ITk Strips will replace the present ATLAS SCT

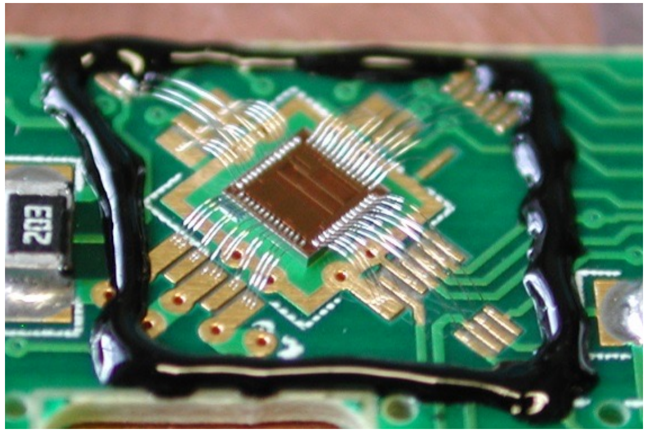
- 4088 Detector Modules
- Independent Powering
  - 4088 cable chains
  - 22 PS racks
  - 4 crates / rack
  - (up to) 48 LV and 48 HV channels / crate
    - Installation a **major** logistical challenge!
- Overall efficiency ~40%
  - Cable R => voltage drops
  - Voltage limiter in line to protect against spikes due to sudden drops in load



Stave250 SPP (2015)

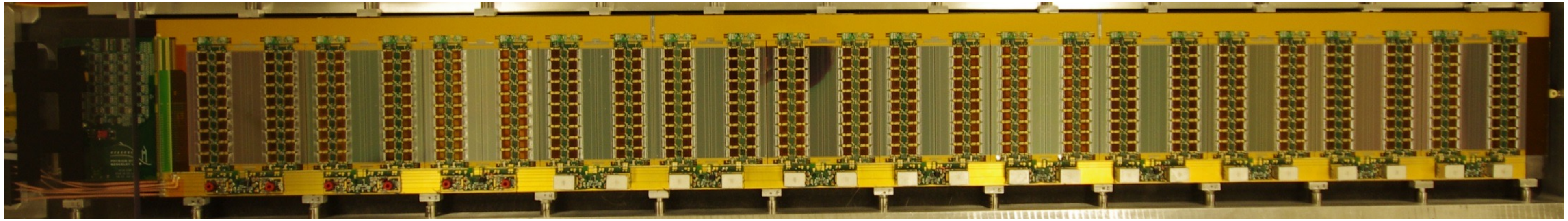


- Used the Serial Power & Protection (SPP) ASIC
  - shunt regulation
  - bypass (under DCS control)
  - over voltage protection
- Population stopped at 7 modules
  - Poor DTN performance
    - occupancy increase correlated with readout activity
  - Reliability issues with COTS FET used to implement bypass protection

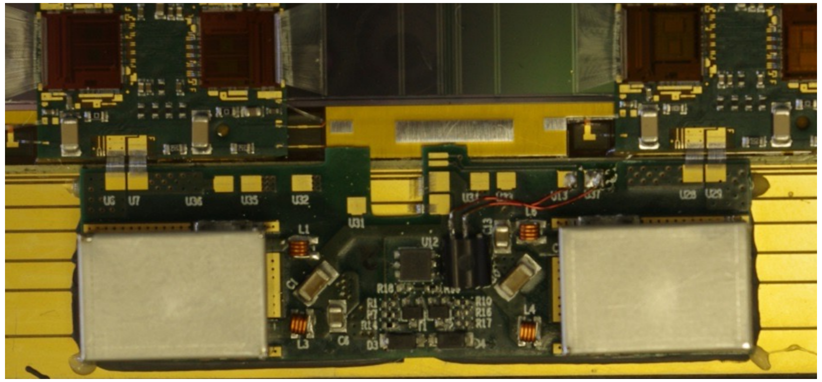


SPP chip

Stave250 DC-DC (2015)

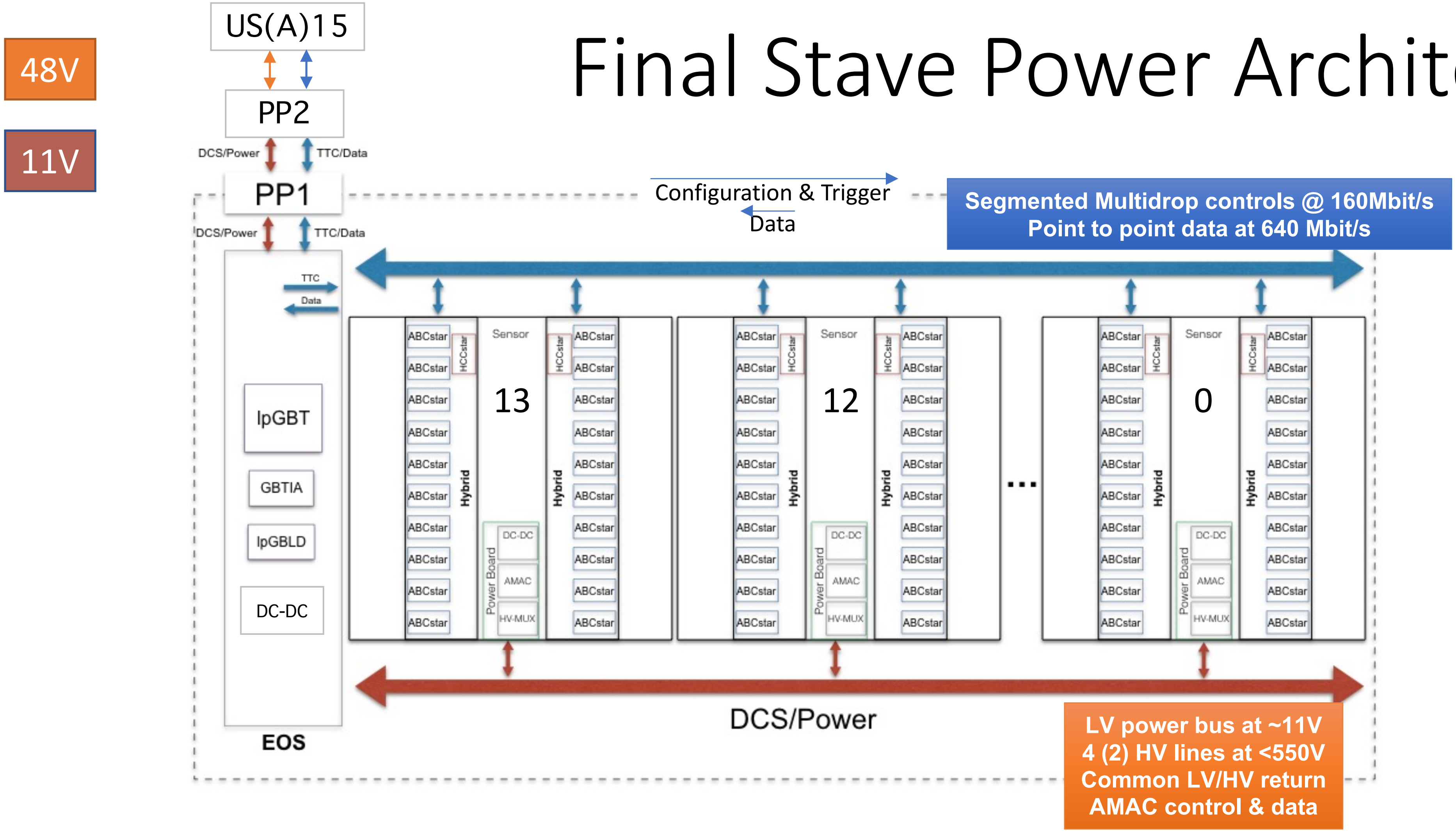


- 12 module stave side
  - Fully loaded and working
- "Tandem" DC-DC converter
  - Design by CERN group
  - Two converters in one PCB
    - Necessary due to high current demand of 250nm chipset – exceeds 4A limit
  - COTS LTC3605 chip
- "one wire" control
  - DS2413 chip
- Power bus split into 4 segments
  - Each drives 4 modules



Tandem DC-DC on Stave250

Final Stave Power Architecture



End of Substructure (EoS) card

- Links off-detector systems (electrical, optical) to the petal / stave

Each stave side has a common 11V feed

- EoS has its own dual stage DC-DC providing 2.5V and 1.5V
- Each module (of 14) has its own on-board DC-DC providing 1.5V

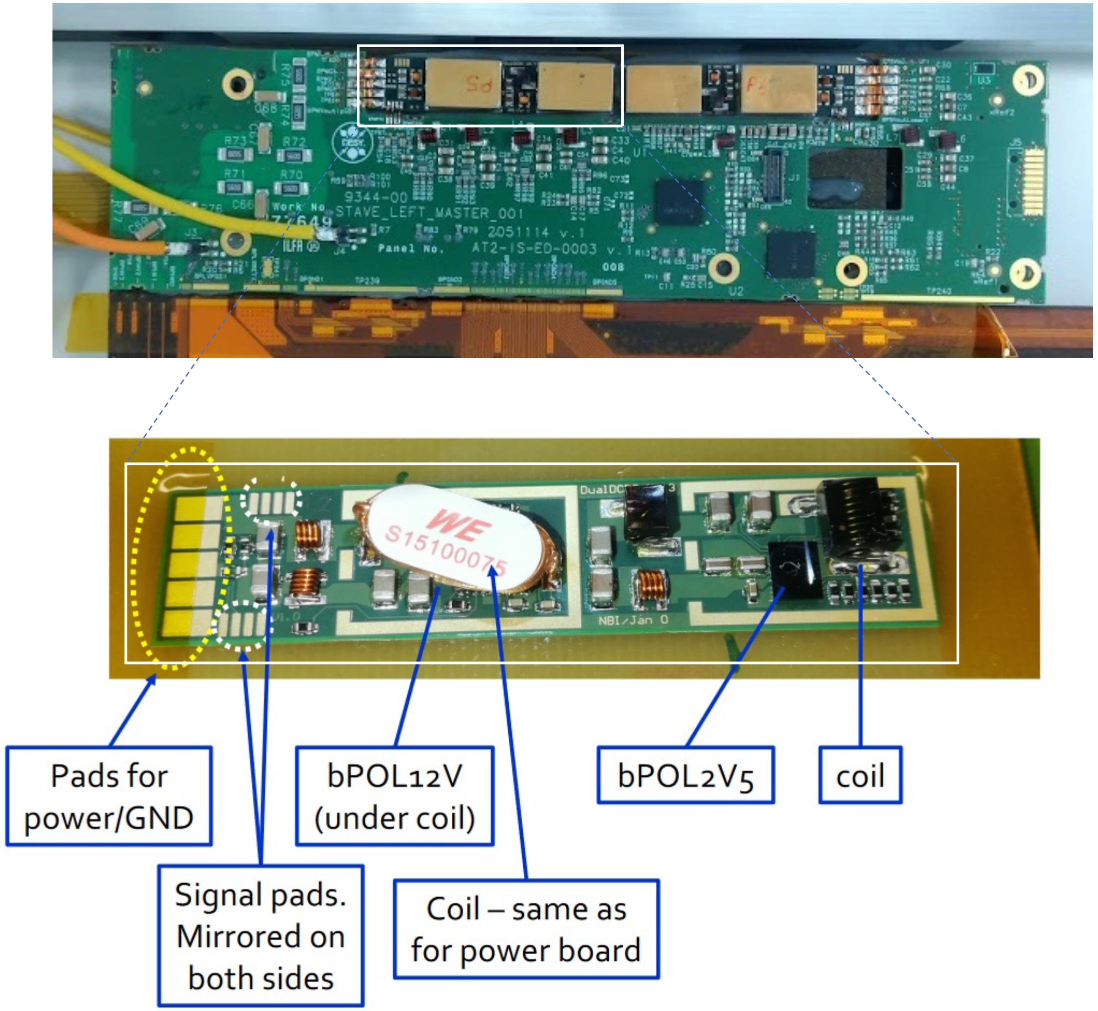
Bus Tape

- Large area copper/polyimide flex routing electrical services
- Engineered for < 200mV ground rise and <800mV volt drop at worst case load

Why 11V?

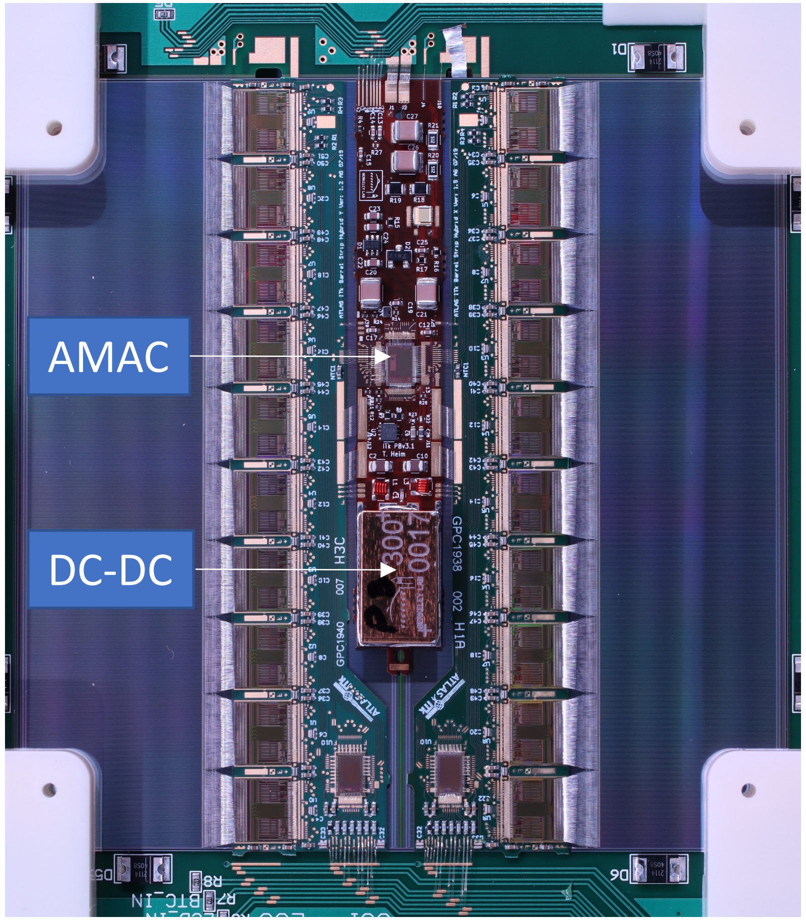
- This gives us the headroom we need to ensure we never exceed 12V at the stave, even if there is a significant, sudden drop in the current

DC-DC at EoS



- EoS requires
  - 2.5V for VCSEL bias
  - 1.2V for lpGBT transceiver
- This is achieved by a dual stage DC-DC converter, layout by NBI
  - 11V to 2.5V (bPOL12V)
    - Nominal 2 MHz switching frequency
  - 2.5V to 1.2V (bPOL2V5)
    - Nominal 4 MHz switching frequency
      - -> smaller inductor
- Due to clearance constraints, two converters with separate power feeds are mounted on one side of the stave
  - One to power each side's EoS

The Pre-Production Barrel Short Strip Module



Pre-Production SS Module in transport frame

Sensor 98 mm x 98 mm

- Four columns of 1280 strips

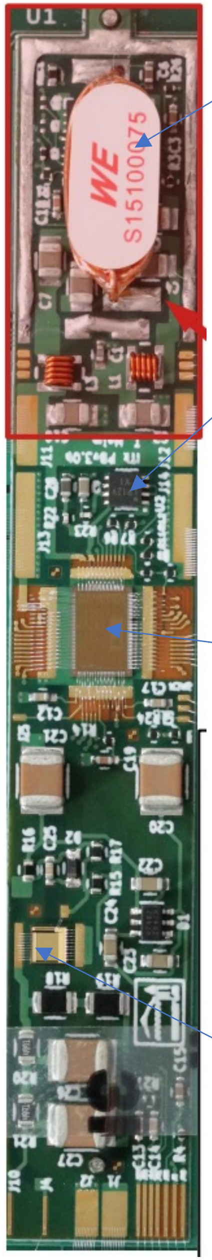
Two readout hybrids, each with

- 10 front-end chips (ABCStar)
- 1 Hybrid Controller Chip (HCCStar)
- ASICs receive 1.5V from DC-DC, internal regulators drop this to 1.2V for (analogue and) digital circuitry.

One Custom Powerboard comprising

- bPOL12V DC-DC (CERN)
- Autonomous Monitor And Control ASIC (AMAC)
- linPOL12V linear regulator (CERN)
- COTS GaNFET HV switch

Barrel Powerboard (LBNL)

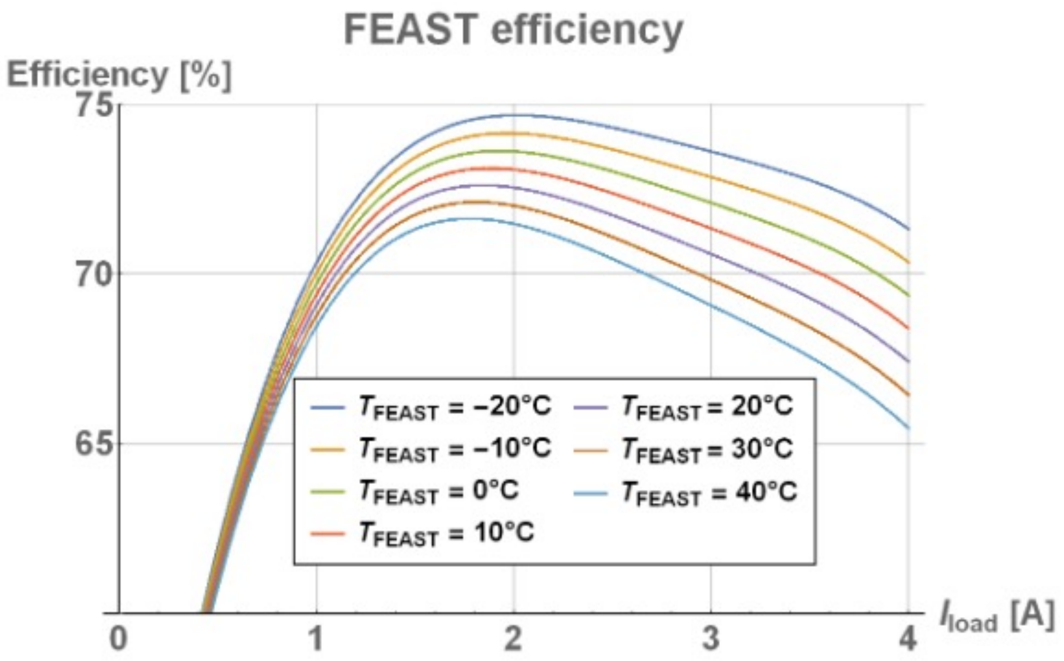


bPOL12V (FEAST) DC-DC
- custom 250 nH solenoid
- 4 mil Al shield box

linPOL12V
- Independent power for AMAC

AMAC: Autonomous Monitor And Control ASIC
- Current, Temperature, Voltage monitoring
- Interlock if programmable thresholds exceeded

GaNFET HV switch
- Source at up to -550V
- Gate driven by charge pump, in turn driven by 100kHz oscillator generated by AMAC

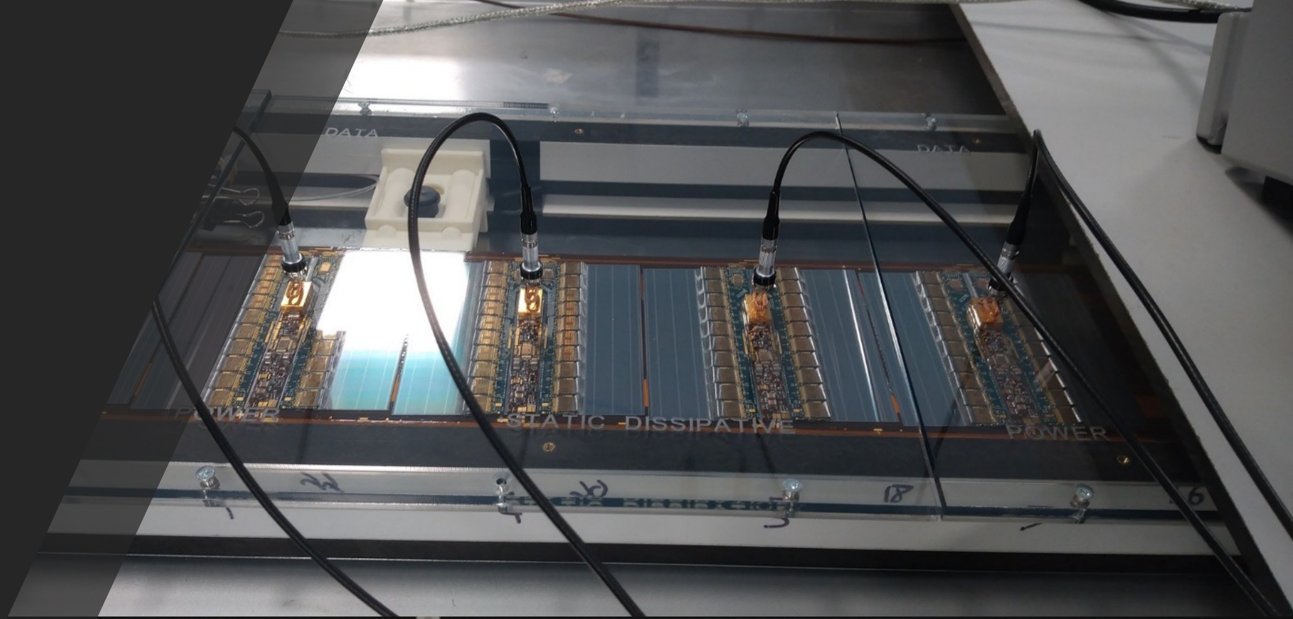


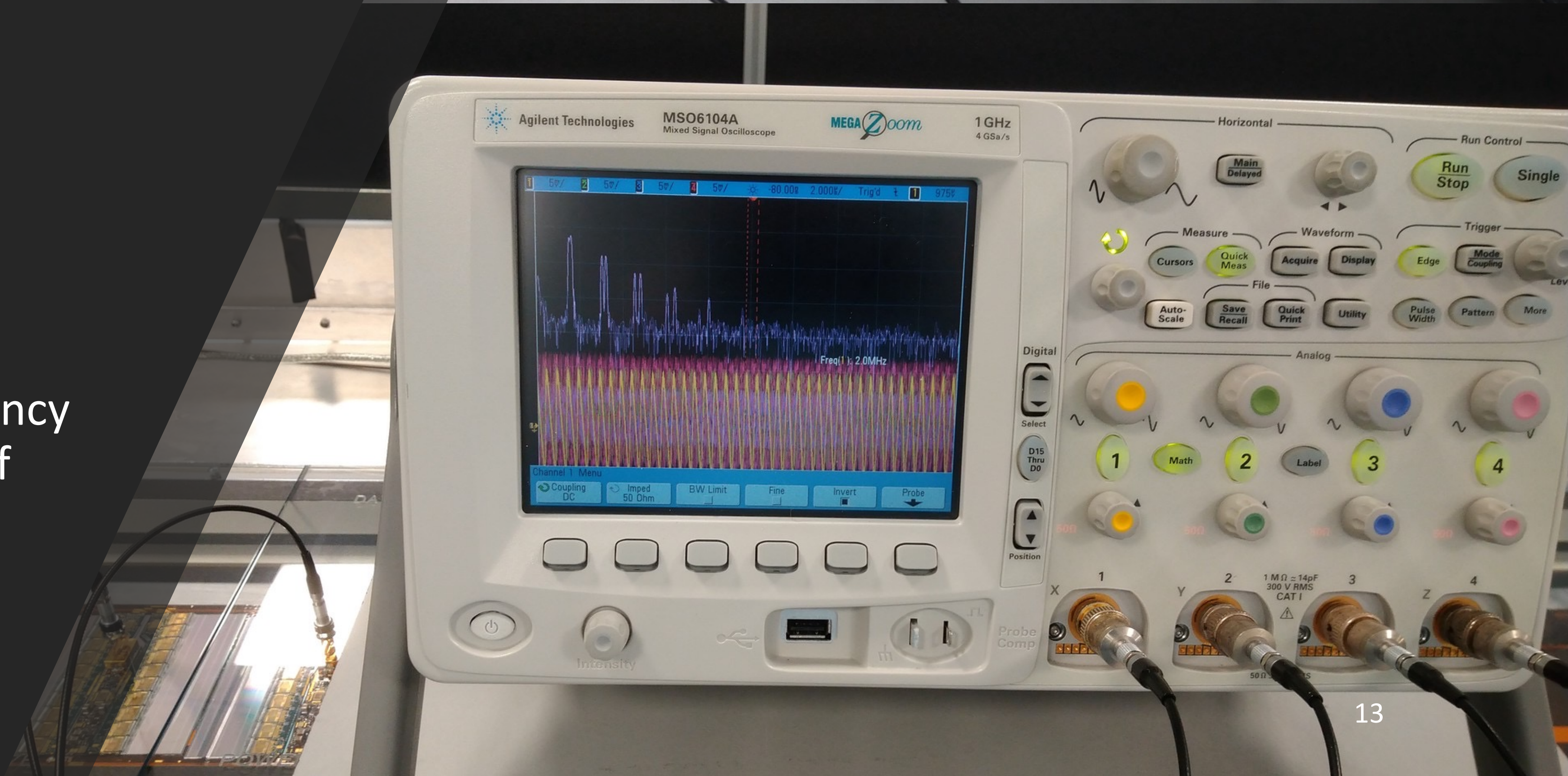
Efficiency for ITk Strip Barrel Powerboard FEAST with 11V input and 1.5V output (bPOL12V expected to be similar)
System designed assuming 4A limit: largest endcap modules exceed this and therefore have two DC-DCs

Magnetic Trigger Tests

To what extent do switching signals from the DC-DC converters couple into the front-end?

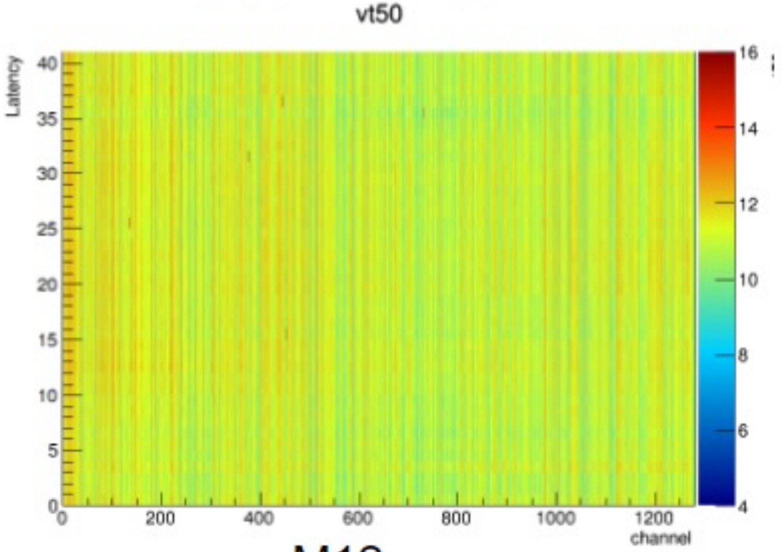
- Place a coil over each of four DC-DC converters
- Select one scope channel at a time under sw control
- Scope trigger output used to trigger DAQ
- Delay trigger signal in DAQ firmware
    - we can study sensor occupancy as a function of the phase of the switching signal



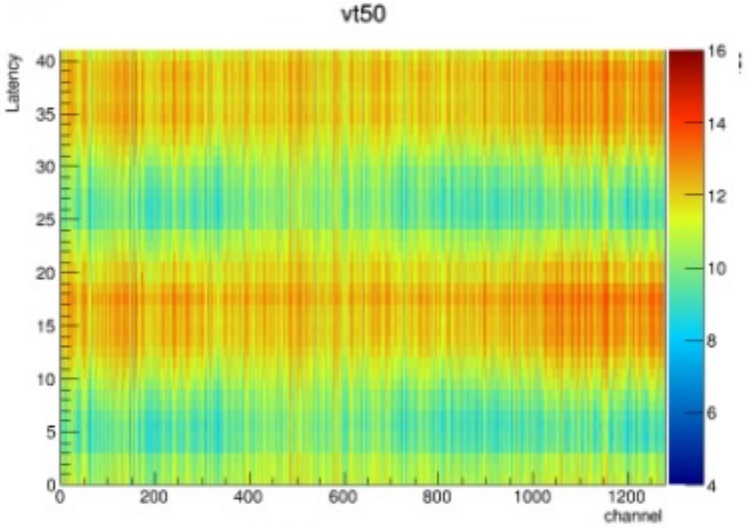


Magnetic Trigger study on stave 5SS (strips under DC-DC)

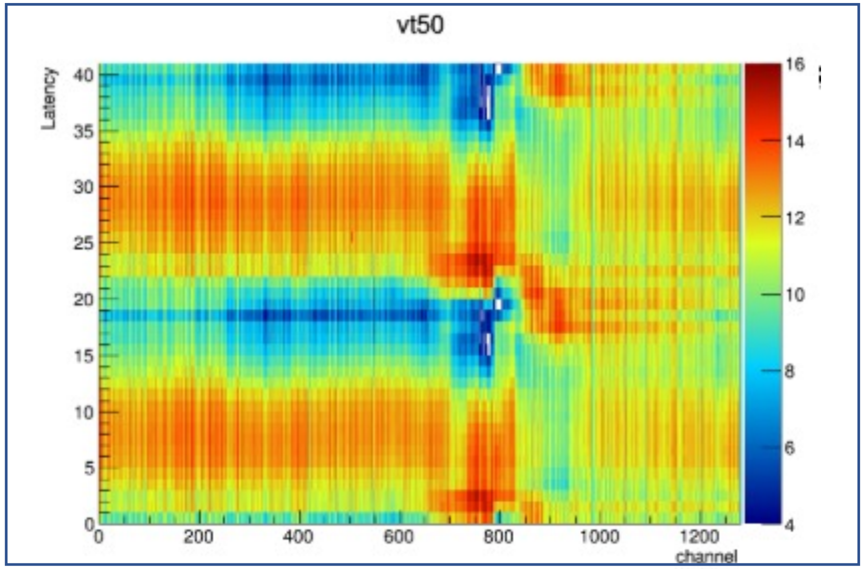
Triggering on this module!



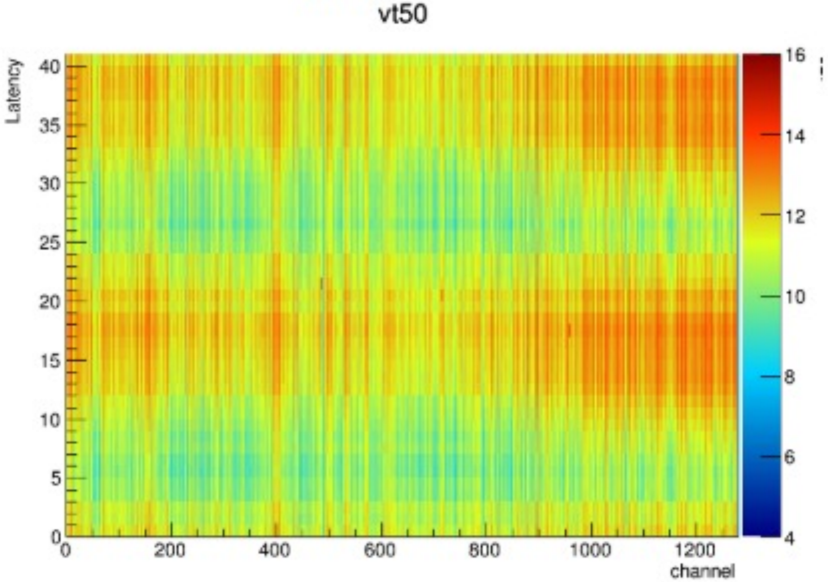
M12



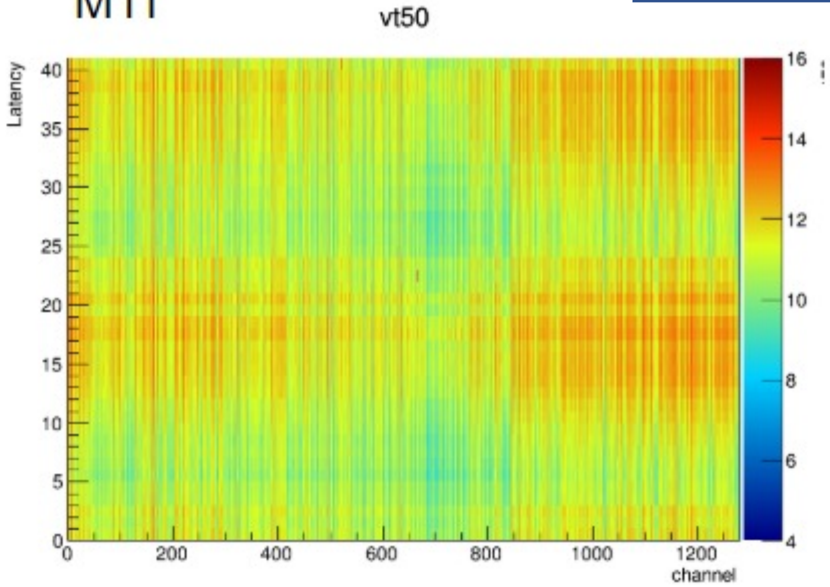
M11



M10



M9



M8

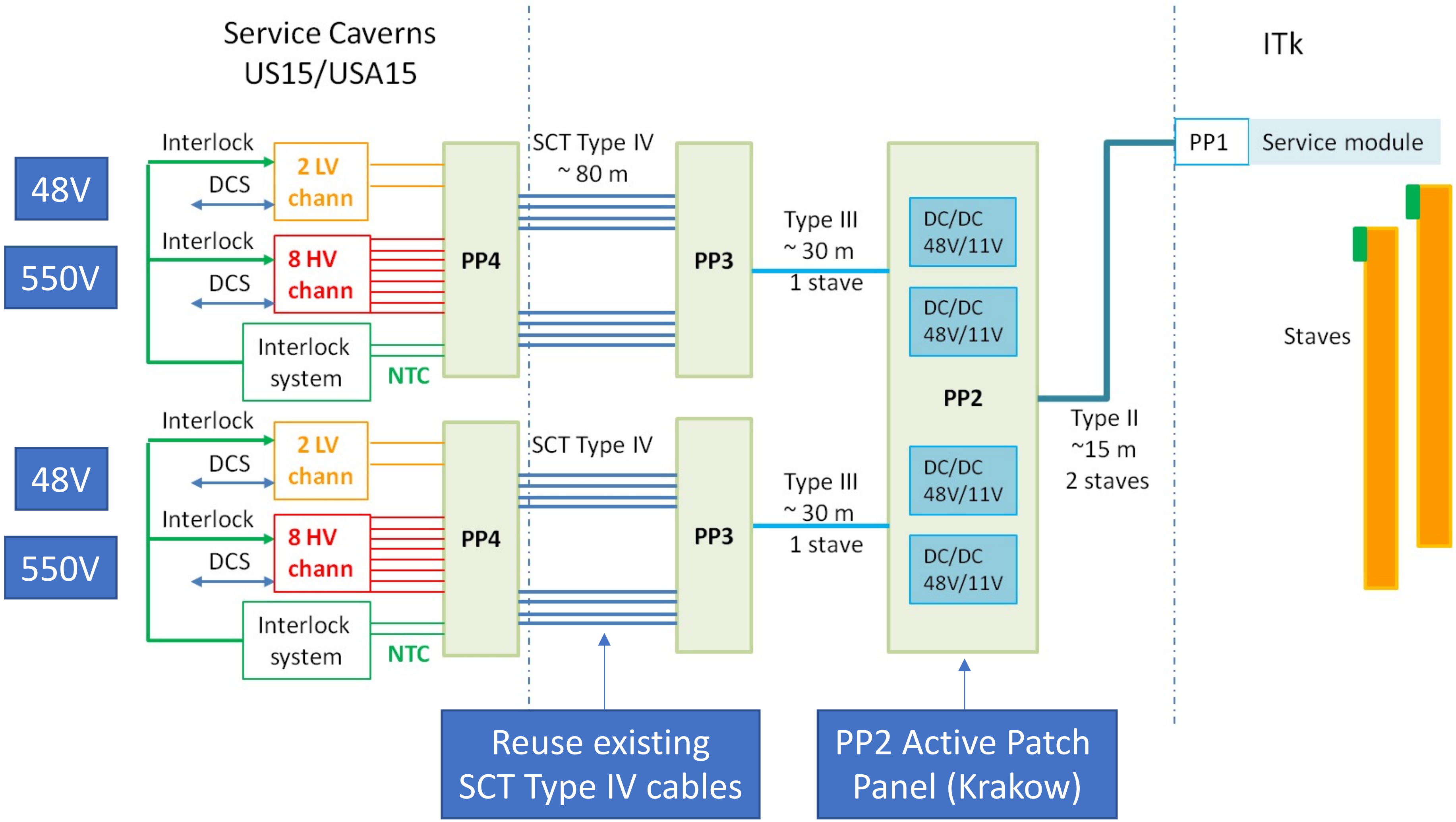
M10’s 2.4 cm long strips clearly see the “hot loop” of its own DC-DC in terms of pedestal variations.

This effect, whilst within acceptable limits, is expected to be reduced in production modules due to layout changes and a reduction in the speed of the switching transistors.

[Magnetic triggering — time-resolved characterisation of silicon strip modules in the presence of switching DC-DC converters - IOPscience](#)

Power chain for Two Short Strip Staves

Due to the length of the power chain (~140 m), a second DC-DC conversion stage is used to improve efficiency



- PP2 built mostly from COTS parts
  - Qualified to the required radiation level within the community
- Exception: uses AMAC for control and monitoring
  - Uniformity of control software
- Prototype uses silicon power transistors
  - Option to use GaNFET for improved efficiency under evaluation

Towards Production

- Staves with short and long strips have been built and tested using the prototype chipset
  - ABCStarv0, HCCStarv0, AMAC2A
  - Including the pictured short strip stave from 2021
- Staves are now being built using a mix of prototype and pre-production chips
  - ABCStarv1, HCCStarv0, AMAC2A
- HCCStarv1 and AMACStar were received in December 2021
  - Staves with the pre-production (= production) chipset will be assembled in the coming months

First thoughts about EIC

- Whilst it was difficult to make Serial Powering work with strips, it works well with ATLAS pixels.
  - Serial Powering could offer the lowest mass solution for EIC, however if this is to happen one would need to put design effort into shunt blocks in Tower 65nm technology right away.
- CERN's bPOL48V technology (rad hard driver for COTS GaNFET) may be an interesting DC-DC option
  - Intrinsically lower switch resistance so higher efficiency
  - Also allows higher conversion ratio 24V to 1.2V
    - 48V only as part of a 48V to 12V option, if I read the specification correctly
- Form factors can to some extent be tailored to reduce mass and required space
  - For example ITk strip powerboards use a custom solenoid, smaller decoupling capacitors
- Whichever solution is adopted, cooling may be the real challenge!