OAK RIDGE National Laboratory

eRD104: "Readout Services Reduction" Updates

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eRD104 Overall Plan

Services Reduction intent is to investigate methods to significantly reduce the services load for an EIC MAPS based tracking detector. This can be broken down into the largest components:

Powering (Birmingham, RAL)

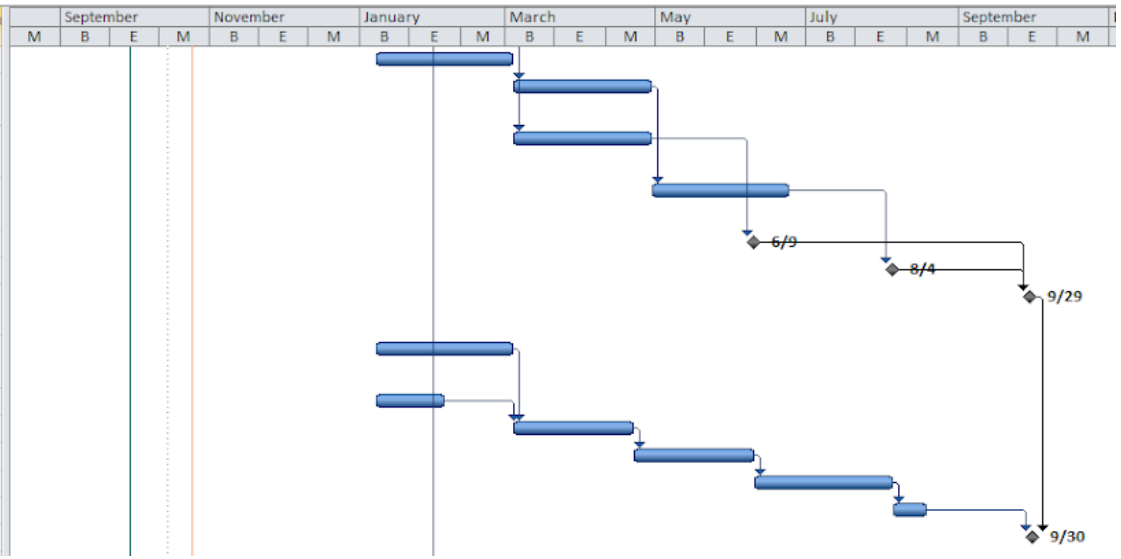
- Investigate the use of DC-DC converter-based architectures to significantly reduce the number of wires needed to power the detector. This will require that we introduce radiation tolerant DC-DC converters into the detector structure in proximity to the disc/stave connection points.
- Investigate the use of serial powering architectures with the same effect. This will require that we introduce regulation at the (stitched) sensor level either on die or as a hybrid arrangement.
- Assess detector design goals and apply the best overall optimization of available technologies studied under R&D to the final implementation of the detector (tracking and others who are interested in working on this)

Data (ORNL, BNL)

- Investigate the use of data aggregation on detector using radiation tolerant FPGAs to receive multiple data streams from sensor blocks (over twinax) and multiplex and transmit the data out via high-speed fiber ribbon connections to RDO boards. This will require functionality in the MUX boards to steer control and configuration and additional power for the MUX boards in detector. Again, the final R&D goal is to develop an optimized viable system for minimizing the services loads due to signal transmission.

2022 Work Plan and Schedule

	Task Mode	Task Name	Duration	Start	Finish	Predecessors	Resource Na
37		Gather serial powering data	40 days	Fri 1/7/22	Thu 3/3/22		
38		design and analyze DC-DC converter architectures	40 days	Fri 3/4/22	Thu 4/28/22	36	
39		design and analyse serial powering architectures	40 days	Fri 3/4/22	Thu 4/28/22	36	
40		cost/benefit analysis of serial and DC-DC	40 days	Fri 4/29/22	Thu 6/23/22	38	
41		report on serial powering	30 days	Fri 4/29/22	Thu 6/9/22	39	
42		report on DC-DC powering	30 days	Fri 6/24/22	Thu 8/4/22	40	
43		FY22 assessment report on powering options	40 days	Fri 8/5/22	Thu 9/29/22	41,42	
44		gather data rate and speed data	40 days	Fri 1/7/22	Thu 3/3/22		
45		rad tolerant FPGA survey	20 days	Fri 1/7/22	Thu 2/3/22		
46		architecture survey	35 days	Fri 3/4/22	Thu 4/21/22	44,45	
47		conceptual design(s)	35 days	Fri 4/22/22	Thu 6/9/22	46	
48		cost benefit analysis	40 days	Fri 6/10/22	Thu 8/4/22	47	
49		report on MUX options	10 days	Fri 8/5/22	Thu 8/18/22	48	
50		erd104 FY22 report	1 day?	Fri 9/30/22	Fri 9/30/22	49,43	



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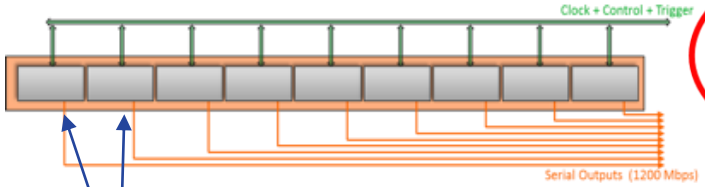
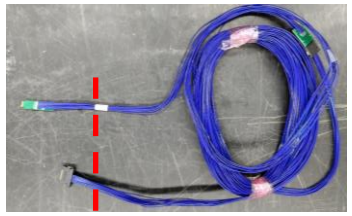
Starting Point: Current ALICE ITS-2 / sPHENIX MVTX

9-sensor **Stave**



ALPIDE **Sensors**



11.6 m twinax

Data (9 x 1.2Gbps),
40 MHz Clock, Control/Trigger

Readout Unit
Front End

85m
GBT Optical Links

Control

Data (3x3.2 Gbps)

Trigger

FELIX
Back End

PCIe

Clock/Trigger

DAQ and Slow Control

Trigger

DAQ Room

Power

Power

CAEN Power Supplies

Regulated power
13.3m

Power Board

Interaction Region

Experimental Hall

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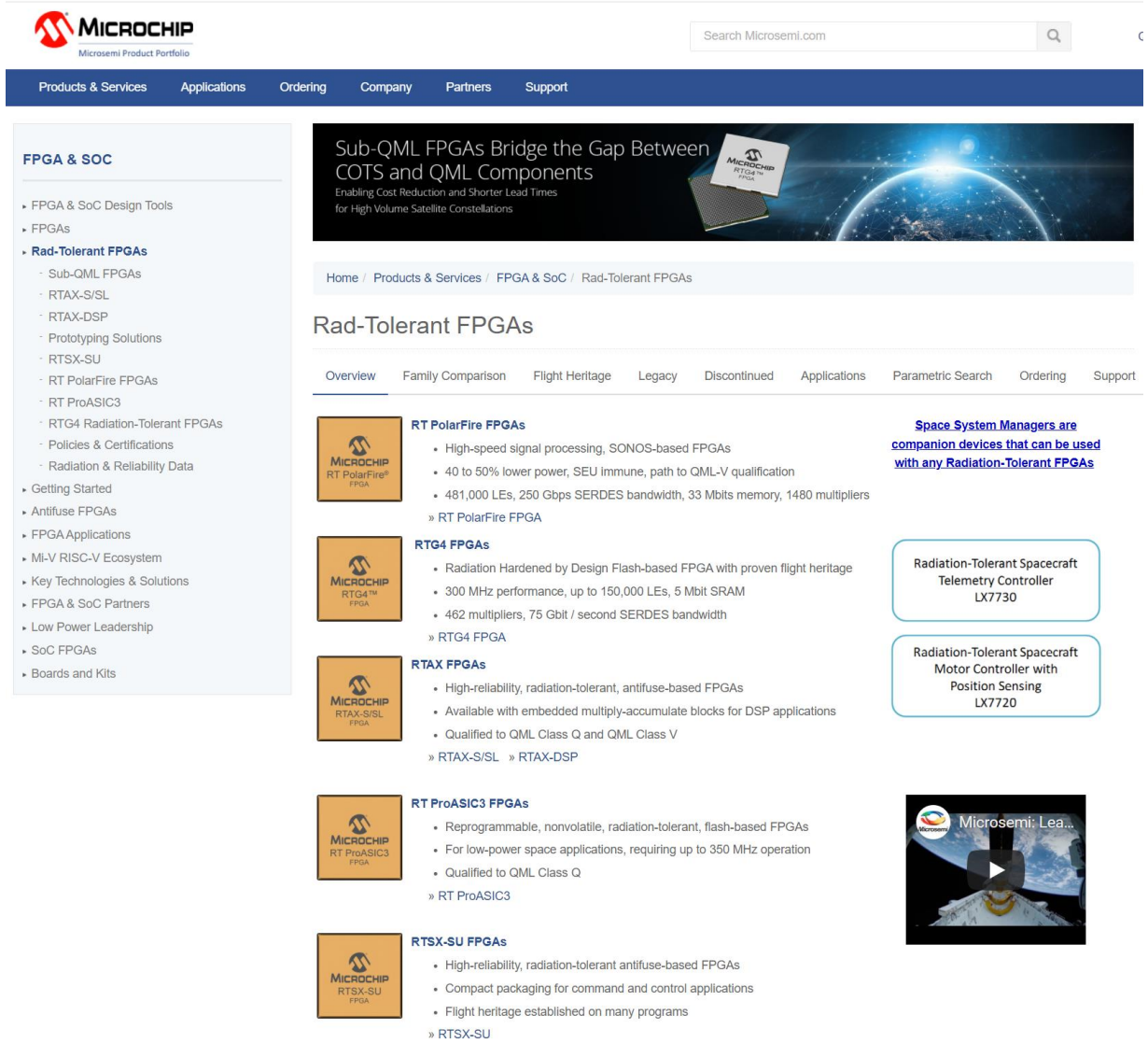
Radiation Tolerant FPGAs

e.g.:



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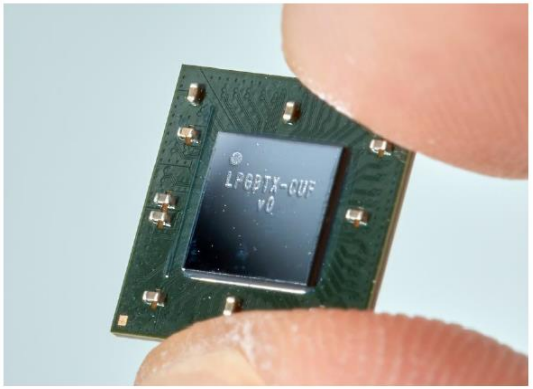
High-Speed Interconnects

Rad-Hard Optical Interconnect: "lpGBT"

More than a "Communications ASIC"

- Capable of
  - 5.12 or 10.24 Gbps (for uplinks)
  - 2.56 Gbps (for downlinks)
- Enables the implementation of RadTol links
  - DAQ
  - Trigger (constant and deterministic latency)
  - Experiment control [slow control]
- Implements Control and Monitoring Functions
  - Three I2C Masters
  - 16 – bit General Purpose I/O port
  - Output reset pin
  - 10 – bit ADC (8 multiplexed inputs)
  - 8 – bit voltage DAC
  - 8 – bit current DAC
  - Temperature sensor
- Designed for radiation hardness
  - Total Ionizing Dose (TID): 200 Mrad
  - Extensive SEU protection (TMR, FEC)



Pin count: 289 (17 x 17)
Pitch: 0.5 mm
Size: 9 mm x 9 mm x 1.25 mm

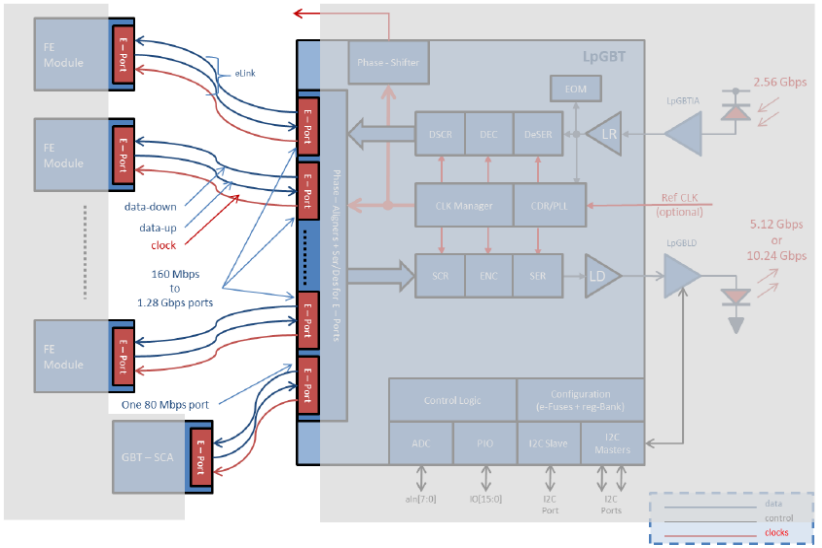
M. Firlej, et al., "An lpGBT sub-system for environmental monitoring and control of experiments" (Fri @ 09:50)

4

lpGBT Capabilities

Communicates with

- The counting room
  - Optical fibre links
- The FE modules / ASICs
  - Electrical links (eLinks)
- The Number and Bandwidth of eLinks is programmable
- For Down eLinks
  - Bandwidth: 80/160/320 Mbps
  - Count: 16/8/4
- For Up eLinks



Input eLinks (uplink)												
uplink bandwidth [Gbps]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mbps]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

5

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Outlook

- ORNL has a setup similar to the MVTX setup shown in the earlier slide, including the FELIX board and a stave with 9 ALPIDEs, that could serve as a testbed for a MUX board prototype
- Initial work on this eRD is mostly intellectual and can proceed in the absence of funding
- Funding was mostly requested to pay for consultation with engineers at ORNL and BNL
- Initial work after a conceptual design would be focused on evaluation of the concept with evaluation boards of the various components chosen