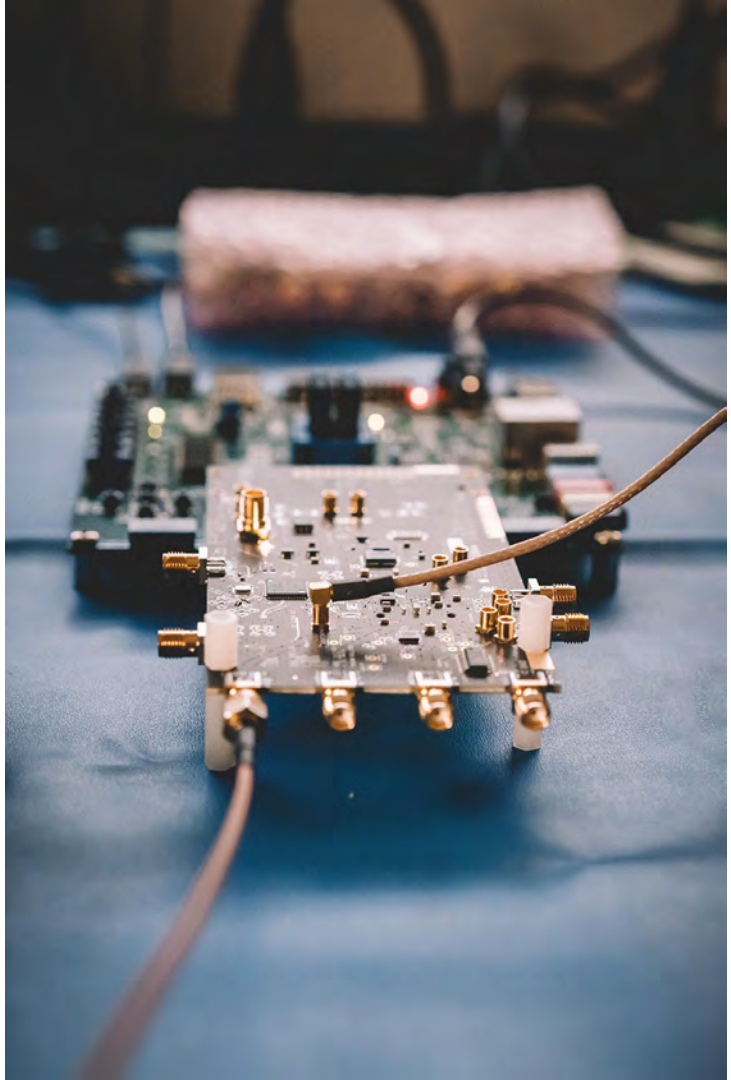

NALU SCIENTIFIC
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Digitizer ASIC Options for LAPPD Applications

March 21, 2022
Isar Mostafanezhad, Ph.D.
Founder and CEO at Nalu Scientific LLC

Work partially funded by US DOE SBIR Grants:

DE-SC0015231, DE-SC0017833, DE-SC0020457

https://indico.bnl.gov/event/15059/

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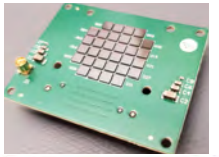
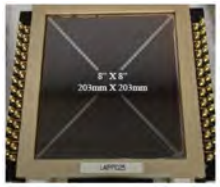
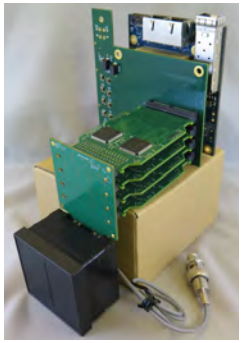
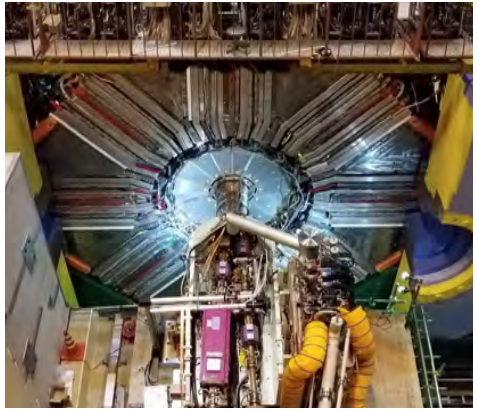
WAVEFORM DIGITIZER SoCs
FOR PRECISE TIME OF FLIGHT ESTIMATION









1. Front-end Chips:

- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP-C
- User friendly: FW/SW tools

2. Integration:

- SiPM
- PMT
- LAPPD
- Detector arrays

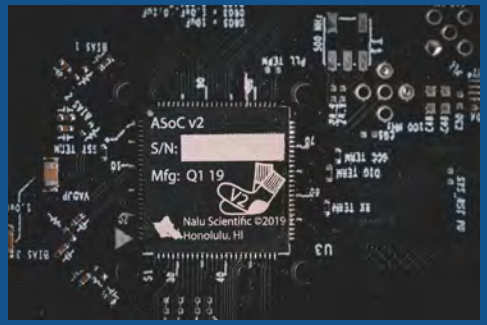
3a. Main application:

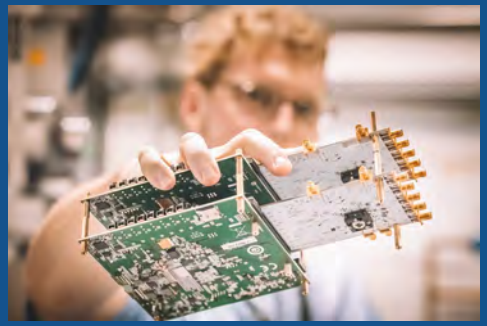
- NP/HEP experiments
- Astro particle physics

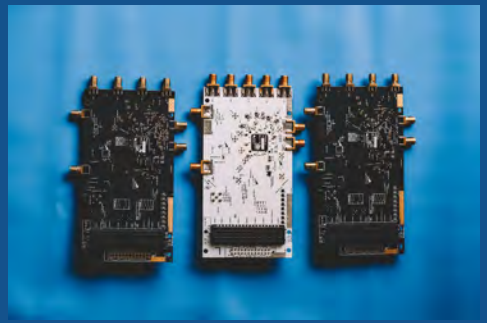
3b. Other applications:

- Beam Diagnostics
- Plasma/fusion diagnostics
- Lidar
- PET imaging

LAPPD photo courtesy of Incom.







ABOUT NALU SCIENTIFIC

Fast Growing Startup in Honolulu, Hawai'i

- Located at the Manoa Innovation Center near U. of Hawaii
- 18 staff members-diverse background
- Access to advanced design tools
- Rapid prototyping and testing lab

Technical Expertise

IC design:	Analog + digital System-on-Chip (SoC)
Hardware design:	Complex multi-layer PCBs
Firmware design:	FPGAs, CPUs
Software design:	GUI, analysis, documentation

Scientific Expertise - NP/HEP subject matter experts

- Physicists (3x) - Recent hire: Kevin Flood
- Electronics for large scientific instruments

Exclusive Distributor Agreement for North America

- Sales of ASICs, eval boards
- Enhanced OEM opportunities

CAEN Technologies Inc.

Nalu = 'wave' in native Hawaiian language

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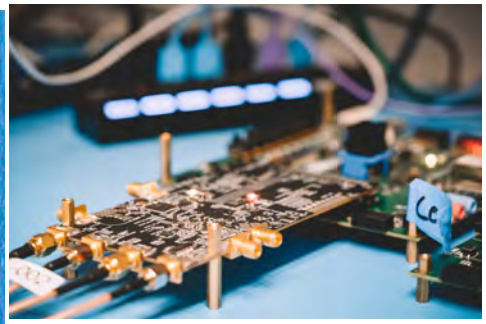
Current SoC-ASIC Projects

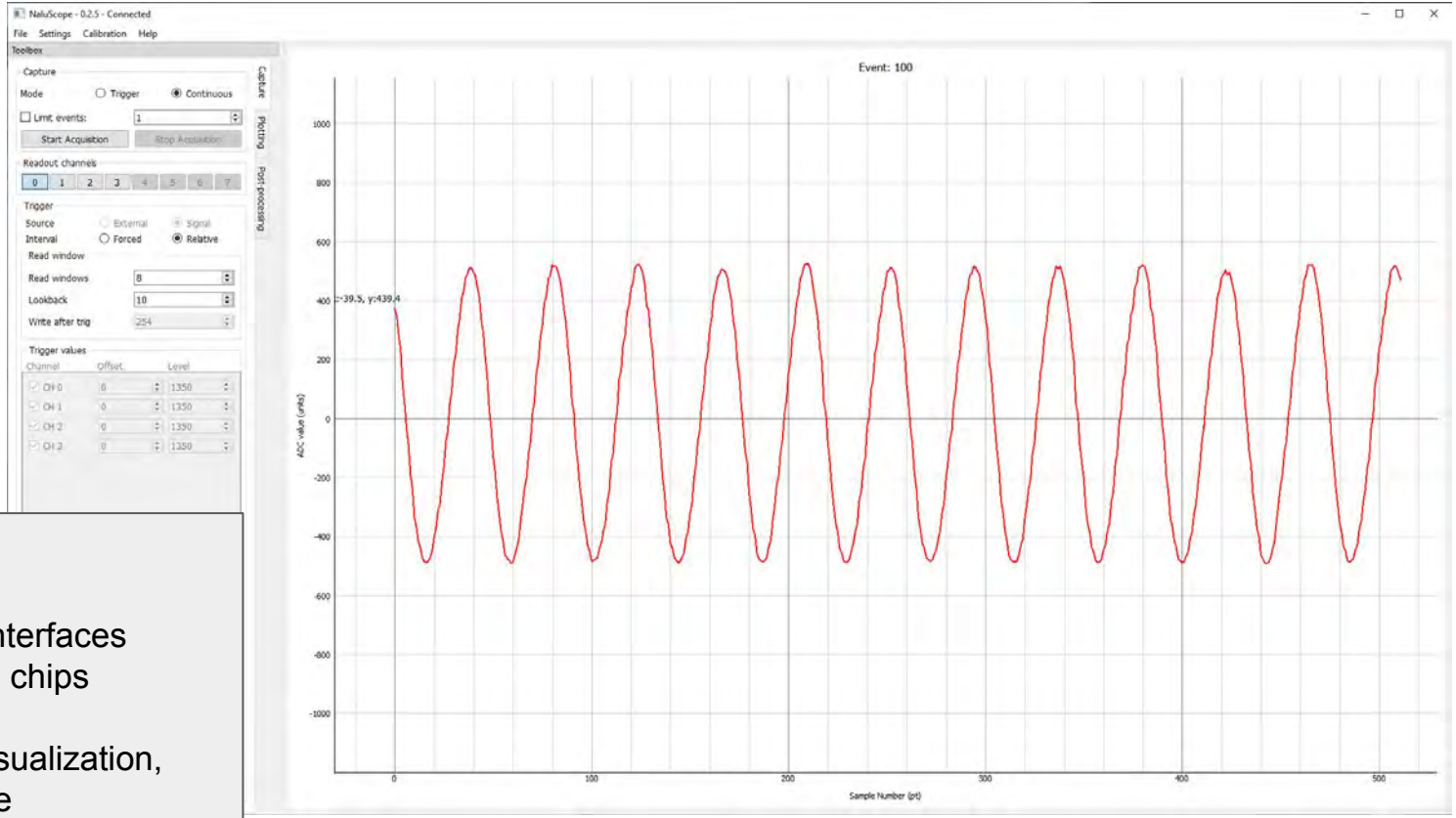
Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoC	1-3	0.6	2k	64	80-120	Rev 1 avail
AARDVARC	8-14	2.5	32k	4	4	Rev 3 avail
AODS	1-2	1	8k	1-4	100-200	Rev 2 avail
UDC	10	1.8	2048	16	5-10	Rev 1 avail
STRAWZ	5	2	2k	64	10	TBD
HPSoC	8-10	2	2k	64	4	Dec'23



- **ASoC**: Analog to digital converter System-on-Chip
- **HDSoC**: SiPM specialized readout chip with bias and control
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
- **AODS:** Low density digitizer with High Dynamic Range (HDR) option
- **STRAWZ:** Streaming Autonomous Waveform-digitizer with Zero-suppression
- **HPSoC:** High Pitch digitizer SoC: AC-LGADs specific readout

Work funded by DOE SBIRs. University of Hawaii as subcontractor.

NaluScope Common Software and GUI



- Windows/Linux PC
- USB interface
- GUI, CLI/scripting interfaces
- Common to all Nalu chips
- DAQ configuration
- Data exploration, visualization, curation and storage
- Plug and play with eval cards

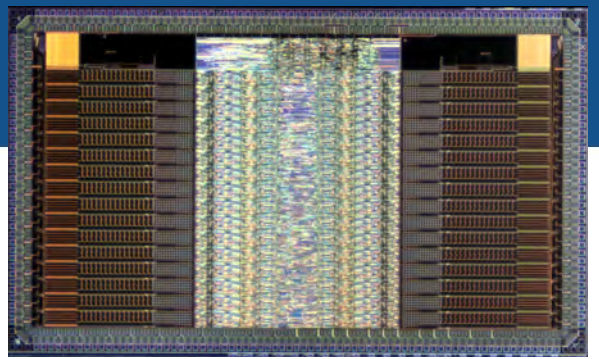
HDSoC V1 DESIGN DETAILS

High density waveform digitizer with dead-timeless readout

- High Density: 64 channels
- Highly integrated, SiPM gain + bias
- Commercially available, low cost CMOS

Parameter	Spec
Sampling Rate	1-2 GSa/s
ABW	> 600MHz
Depth	2k Sa
Trigger Buffer	~3 us*
Deadtime	0**
Channels	64
Supply/Range	2.5
ADC bits	12
Timing accuracy	80-120ps
Technology	250 nm CMOS
Power	TBD

- On chip calibration
- Serial interface
- On chip feature extraction
- Virtually dead-timeless
- 32 ch proto chip fabricated
- Phase II SBIR in progress
- Chip under test
- Next steps: more testing, rev 2 fab

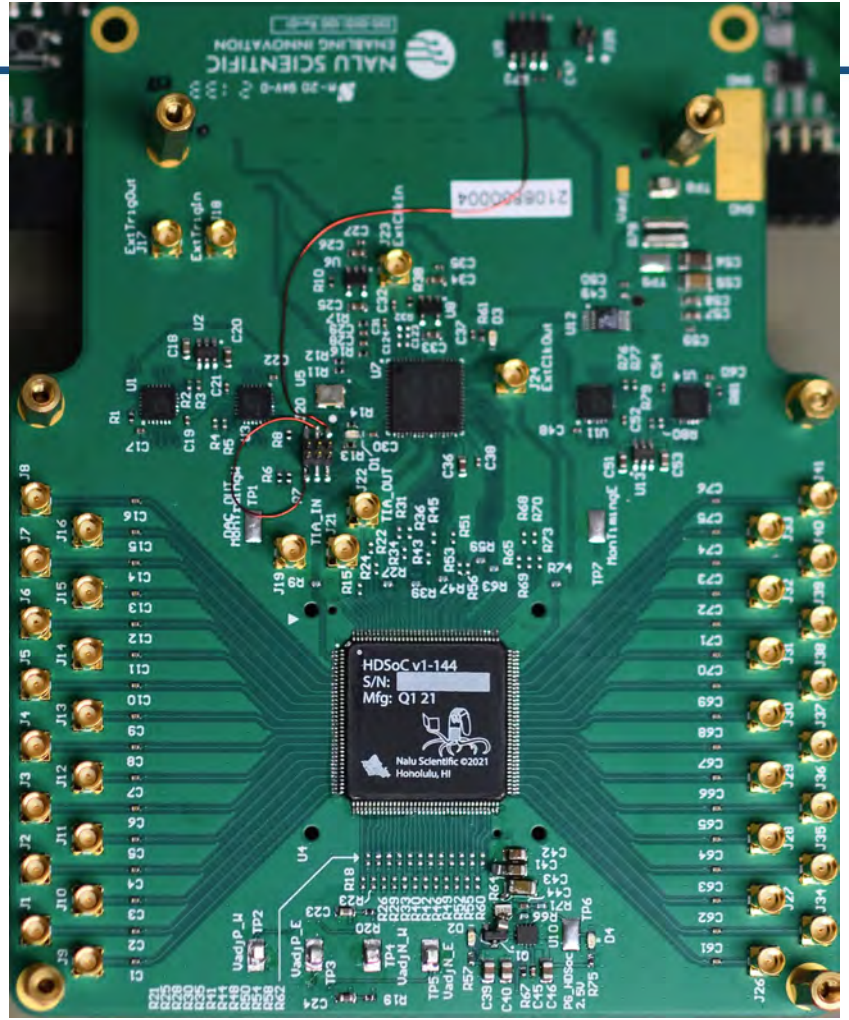


HDSoC v1 die shot

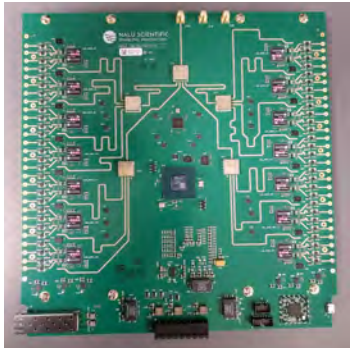
** Simulated Up to 240 KHz / ch with single serial link using on-chip self trigger and feature extraction.
Up to 400 kHz / ch with additional serial links.

HDSoC - Current Status

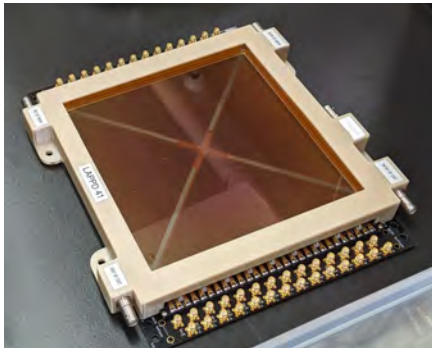
- **Fabrication:**
  - 32 channel prototype fabricated
  - 144 pin package purely for bring-up
  - Smaller QFN-100 available for integration
- **Testing (functional):**
  - FMC eval card under testing
  - FW, SW developed
  - Chip turns on, responds to commands
  - Timing generators works well
  - All channels can digitize and readout
  - TIAs work, need more tests
- **Next testing steps:**
  - Bias and readout SiPMs
  - Characterize TIAs
  - Test all digital functions and serial link
  - Optimize chip biases
  - Push for performance on data rate and quality



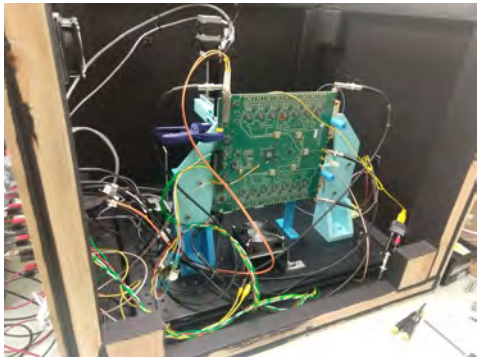
Integration efforts - HIPeR



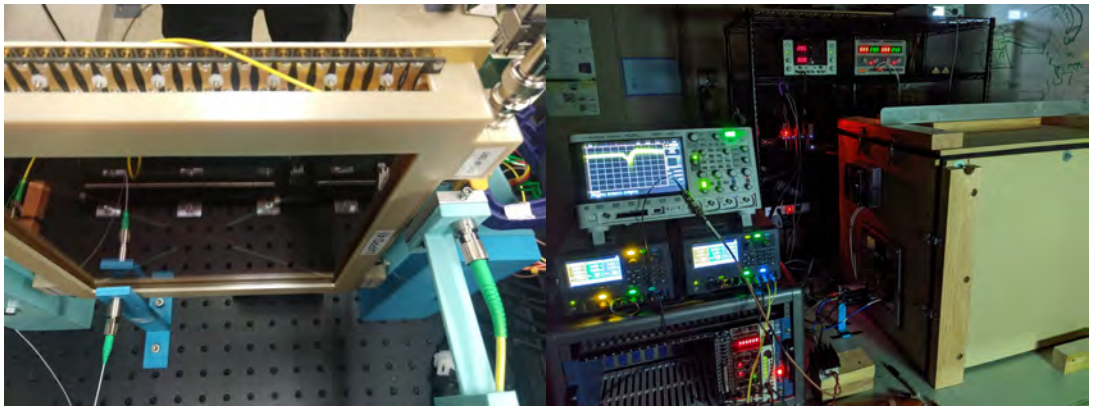
AARDVARC based readout

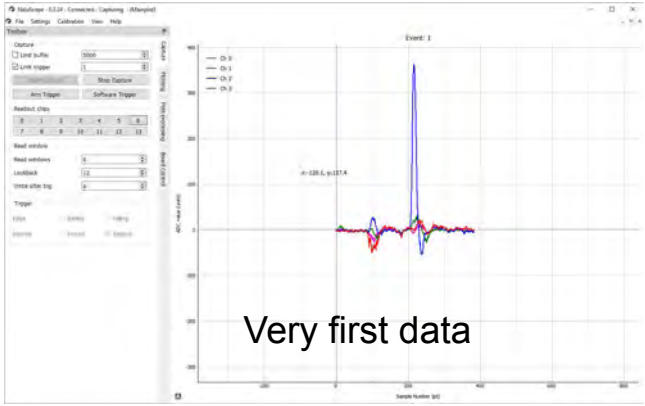


Incom's Gen 1 LAPPD



Integration and testing (UH)



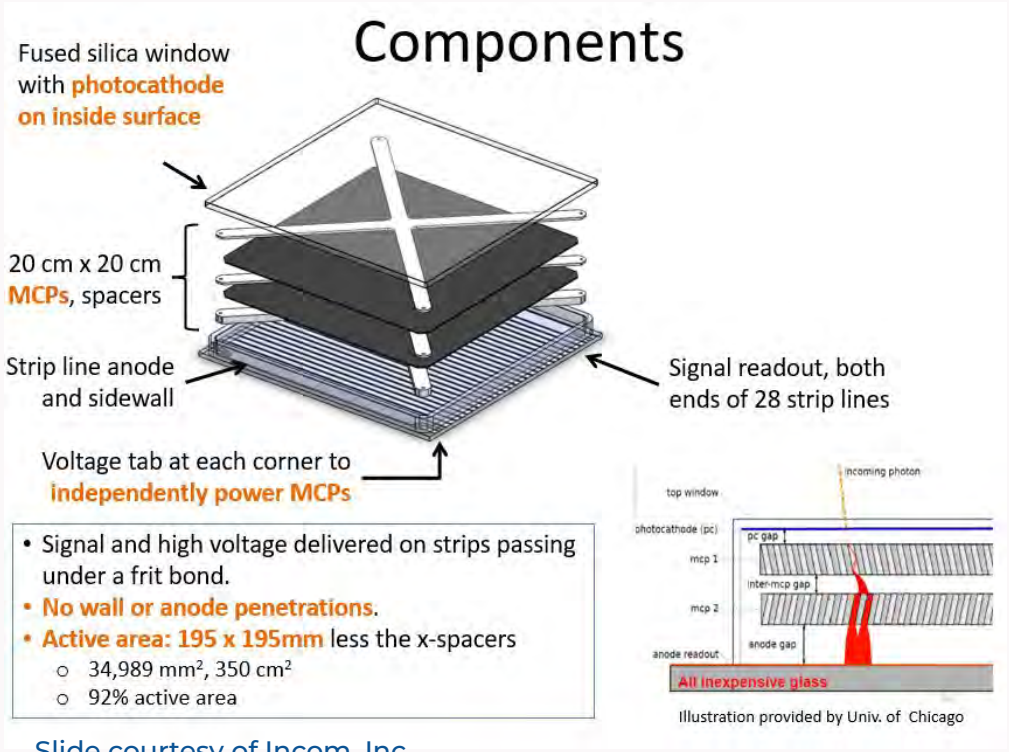


Nalu Scientific Phase I SBIR in collaboration with Incom and University of Hawaii.

IEEE NSS/MIC Conf Oct 2021, conference paper available

LAPPD Gen I

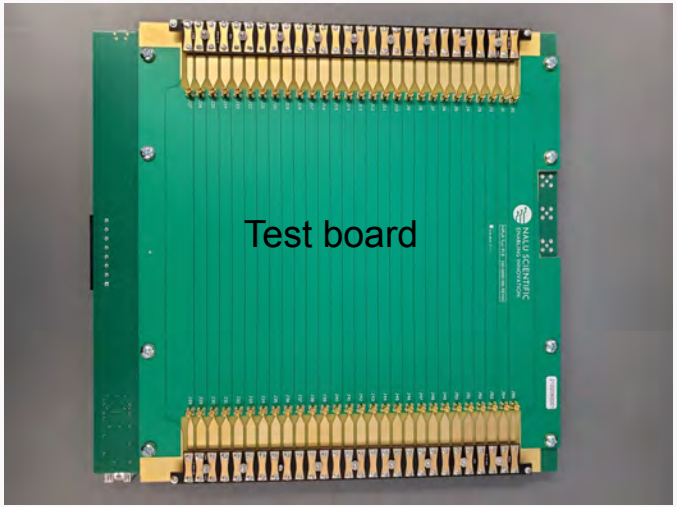
- Strip based readout:
  - MCP amplified p.e. are collected by metal strips
  - Strip identify “y” position of hit (sub-strip resolution possible via amplitude ratio of neighboring strips)
  - Arrival time difference on 2 sides of strip identify x position:
    - Requires very good timing resolution

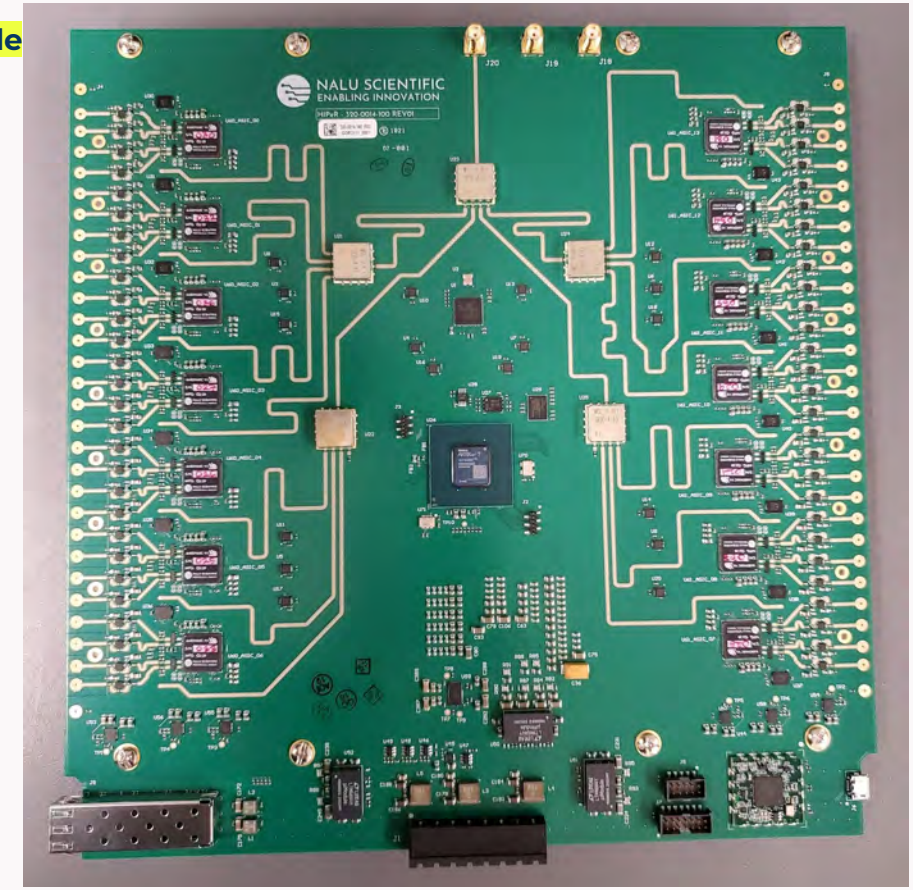


Slide courtesy of Incom, Inc.

IEEE NSS/MIC Conf Oct 2021, conference paper available

Fully Populated board





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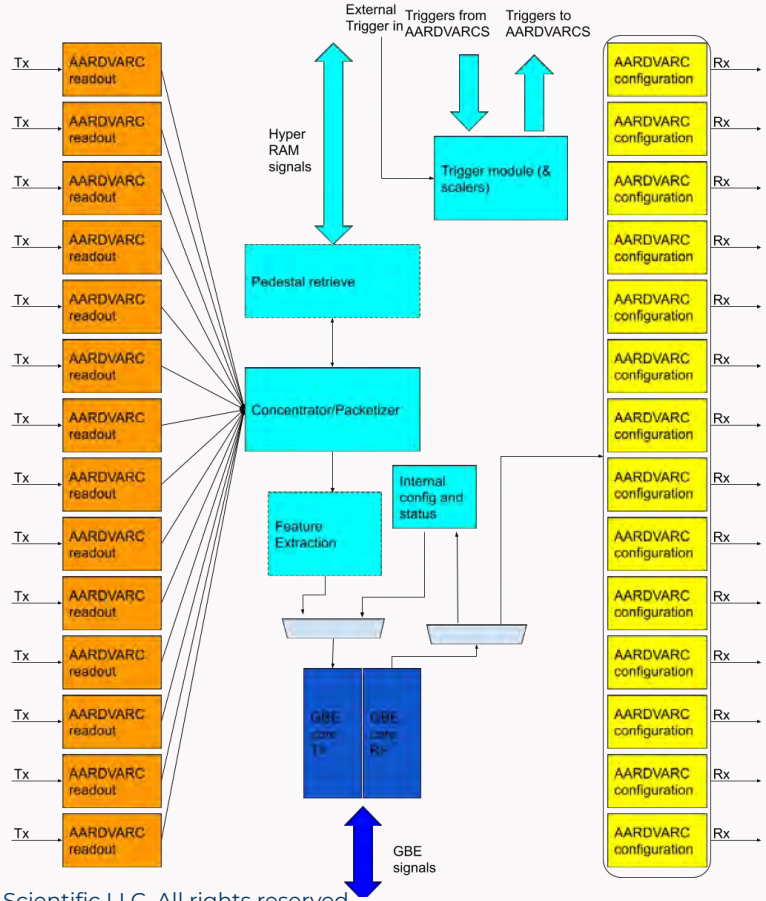
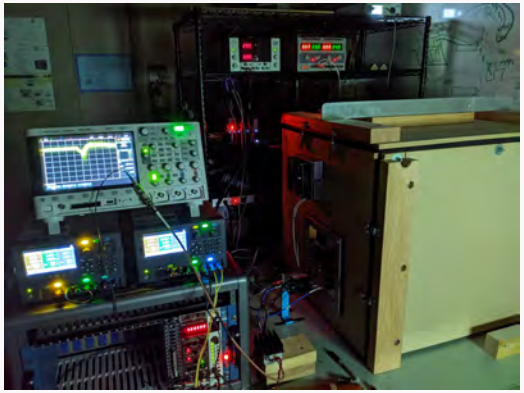
FW architecture

- **Modular structure:**
  - Easy to expand/add features
- **Individual readout modules**
- **Individual configuration modules**
- **Concentrator kept simple in Phase I:**
  - Pure packetization
  - Data pass through
  - Can add calibration/Feature extraction
- **Triggering module separate:**
  - External triggering:
    - Can still use individual channel triggers to limit data rate
  - Self triggering (streaming architecture)



LAPPD setup

- **Dedicated photodetector test setup:**
  - Large total area (61 x 61 x 76 cm^3), suitable for a full LAPPD tile
  - Vibration isolated optical breadboard.
  - Modular patchbay system
  - Gasketing to seal against light leaks.
  - 3D printed mounts for quick integration of LAPPD + readout electronics.
- **Scannable laser system:**
  - 30.5 x 30.5 cm^2 scanning area.
  - Fast PILAS laser.
  - Fixed neutral density filters + variable optical attenuator
  - Dual laser illumination positions
- **Thermal management:**
  - Thermoelectric cooling.
  - Temperature monitoring.
  - Temperature triggered power down safety interlocks.



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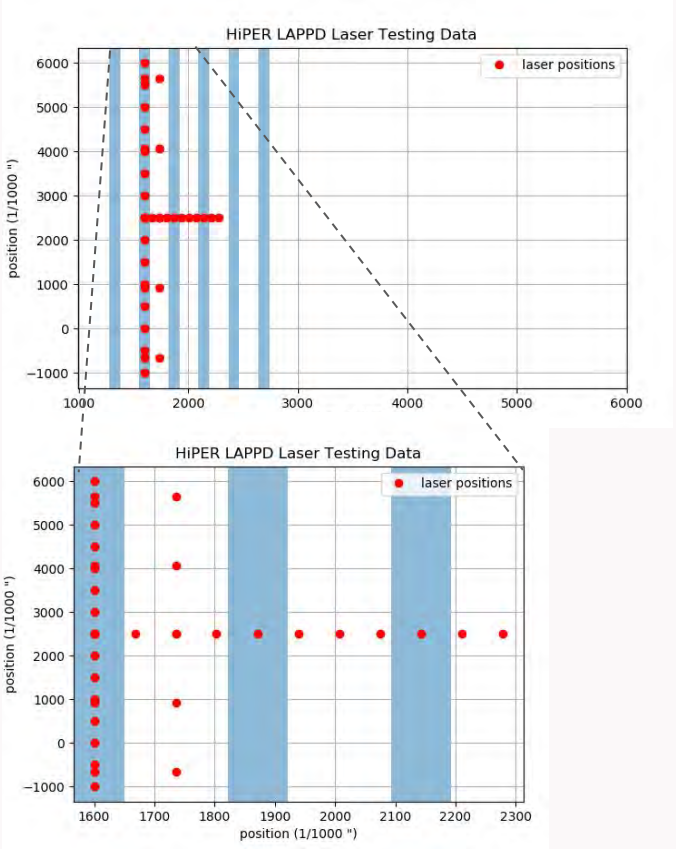
LAPPD scanning

- Acquisition has been repeated at various position for the incident laser pulse
- Used for probing the timing and positioning capability of the system
- In-between positions to estimate the position the y axis



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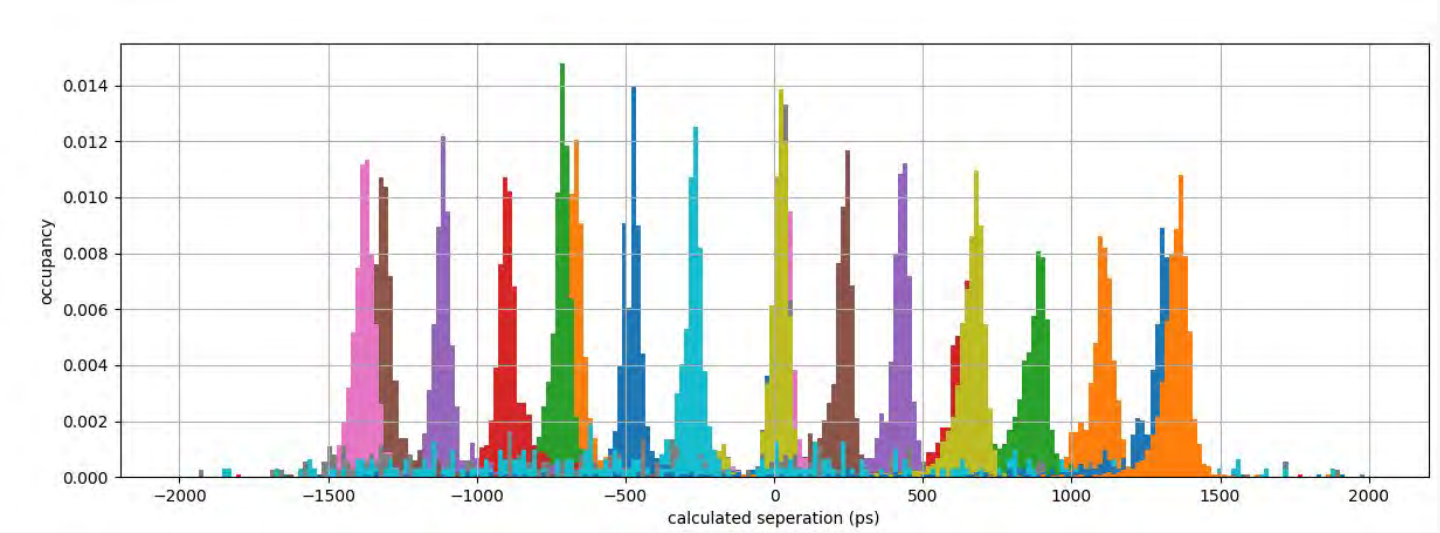
In strip position

- Scanning on a single strip
- Multiple acquisition in same position provide an histogram an estimate for x
- Histogram used to measure position and estimate error.



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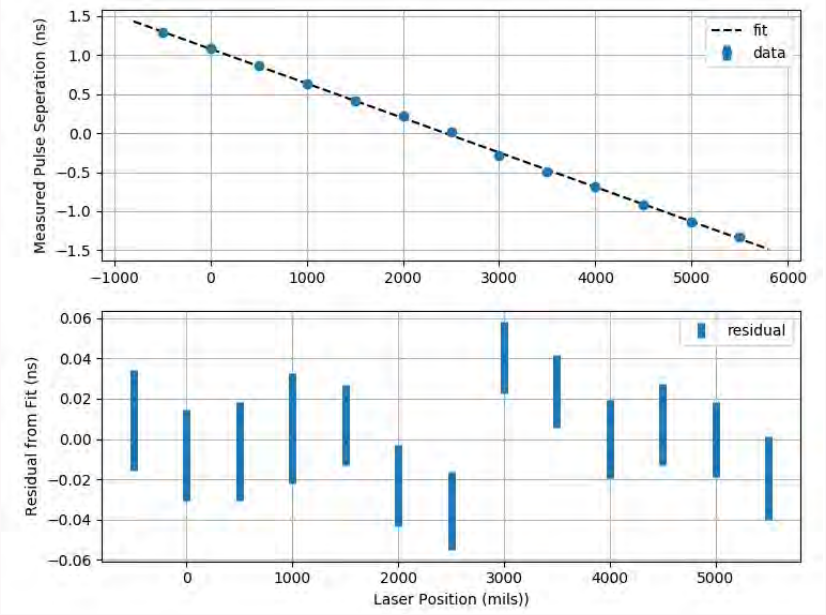
In strip position - results

- Mean from gaussian fit used for position expressed in time
- Standard deviation used for error bars
- Residuals from linear fit: typically 20 ps -> 2.3 mm
- More investigations into the outliers and effect of small pulses needed to confirm
- No chip timing cal yet

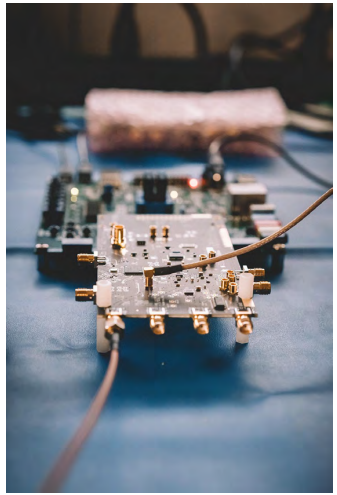


Summary

NALU SCIENTIFIC
ENABLING INNOVATION

CAEN Technologies Inc.

- Nalu Scientific Expertise:
  - FEEs for NP/HEP experiment readout
  - High integration (clock, memory, calibration)
  - Packaged chips and eval cards available
  - Additional testing under way including irradiation
  - Exclusive Distribution Agreement with CAEN
- Expertise:
  - NP/HEP electronics/FW development
  - Advanced ASIC/HW/FW/SW Design
  - Detector electronics design
- Funding:
  - SBIRs: covers costly chip development
  - Trade studies: initial assessment
  - Custom design contracts: Implementing new packaging and PCB designs
- Next steps - OPEN FOR BUSINESS
  - Continue chip+PCB development
  - Continue engagement with experiments in order to tailor the designs to evolving experiment needs
  - New integration efforts under way, incl. NP ML/AI ASIC/FPGA SBIR proposal currently under review
  - Eval boards available for testing



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