OAK RIDGE National Laboratory

# DAQ/Electronics/Readout Working Group Report

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U.S. DEPARTMENT OF ENERGY

# DAQ/Electronics/Readout Working Group

- Conveners: A. Camsonne, C. Cuevas, J. Landgraf, J. Schambach
- 23 Institutes expressed interest in working on DAQ
- Mailing list: eic-projdet-daq-l@lists.bnl.gov
- Indico category: https://indico.bnl.gov/category/409/
- Wiki: https://wiki.bnl.gov/eic-project-detector/index.php/DAQ
- Mattermost channel: https://eic.cloud.mattermost.com/main/channels/det1-daq
  signup: https://eic.cloud.mattermost.com/signup_user_complete/?id=i8gnmob4stdrpjfrezhegxs3ew

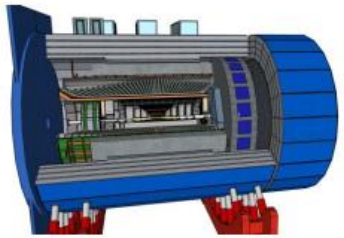
- Talks from last Streaming Readout Workshop X: https://indico.jlab.org/event/519/timetable/#all.detailed
- Live Notes from SRO workshop:
  https://docs.google.com/document/d/1vFz1Z9c4Ck7eaE_eMcJgzg_UNUsYwC1OnygzlX95yic/edit#heading=h.175xdrpf8ddv
- A summary report for the SRO workshop is here: https://docs.google.com/document/d/1X6Ms_oubcWx-8DUiExMFIJdCC6svWNbWKiz7OQjMCeQ/edit?usp=sharing

- Schedule: Future meetings will be Thursdays @ 9:00 EDT

# Executive Summary

- Since DPAP decision we had 10 WG meetings with participation between 10 and 20 collaborators and a workshop on Streaming Readout ("Streaming Readout Workshop X")
- There is wide agreement within the DAQ WG on the general scheme of the streaming readout
- Nonetheless there are still two detectors for which software triggering (or at least selection based upon correlation with other detectors) is planned:
  - dRICH under the assumption of SiPM readout
  - Far backward where high-rate data is consolidated into beam parameters using histogramming, but sampling is desired in conjunction with central detector activity.
- We have had and plan to continue to have reports on the developments in the detector groups
  - Reports so far: Calorimeters (O. Hartbrich), MPGD (I. Mandjavidze), TOF (T. Ljubicic), Far Forward & Far Backward (J. Landgraf), RICH (A. Camsonne), dRICH (P. Antonioli)
- The most pressing topic for us is the common parts of the detector interface that needs to be shared among all detector FEEs. This includes the timing system (lpGBT disadvantages outweigh advantages),the data interface, and the configuration interface. This is a pressing item because a shared scheme needs to be available before final FEE design can be completed. It's also a complex task that will need detailed analysis of the detector needs to be properly evaluated.

# ~~Detector 1~~ EPIC Streaming DAQ

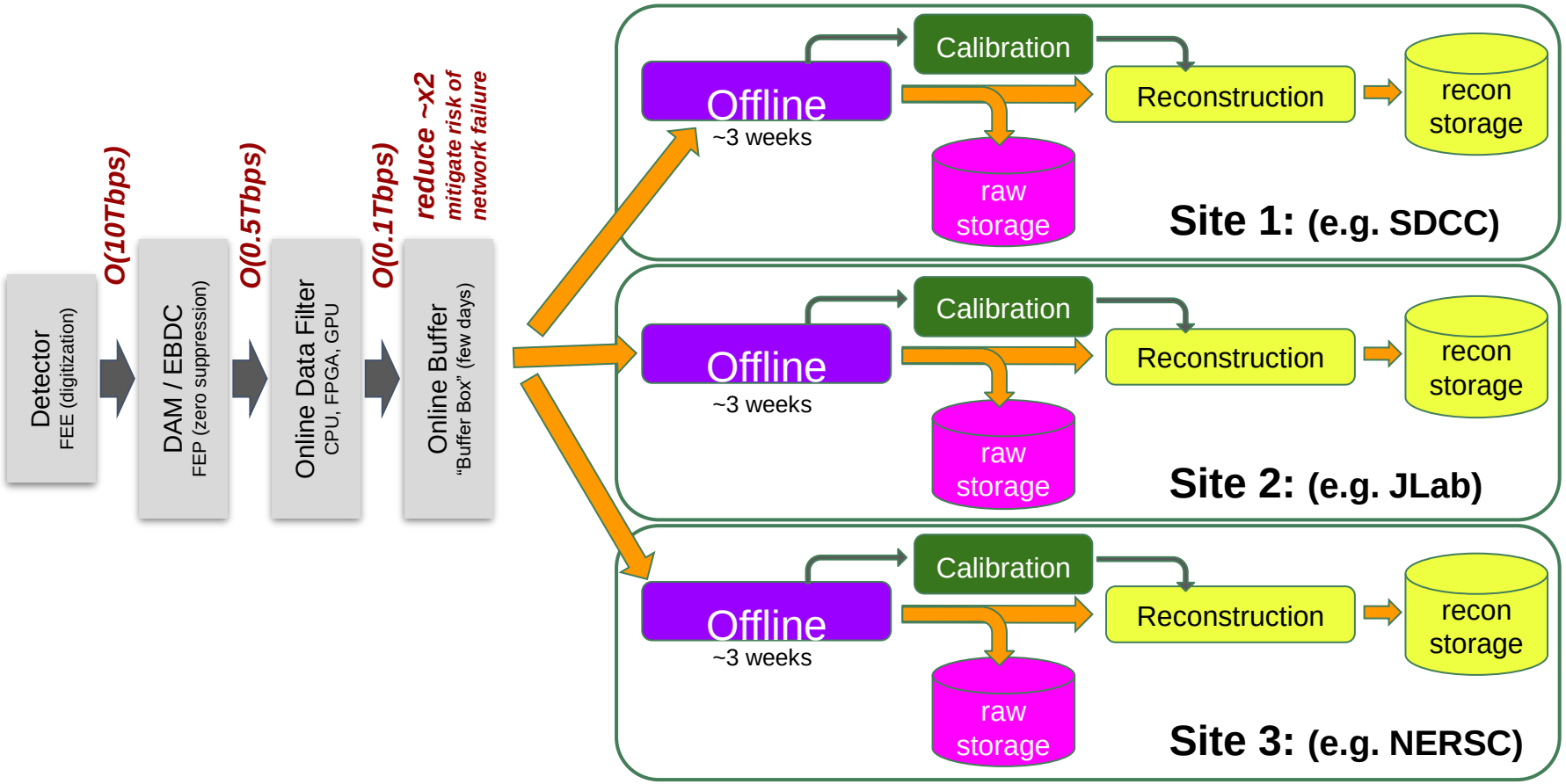


FEE = Front End Electronics
AGG = Front End Aggregation
DAM = Data Aggregation Module
EBDC = Event Buffer / Data Compressor

Timing System
Detector Control
FEE
AGG
DAM
EBDC
Network Switch
Online Data Filter
Buffer Box
Monitoring
To permanent storage and nearline processing

O(2 Pbps)
O(10 Tbps)
O(0.5 Tbps)
O(0.1 Tbps)

# DAQ as part of overall Computing: Online to Offline Stream




(from: David Lawrence – ECCE Computing Model – Streaming Readout Workshop IX)



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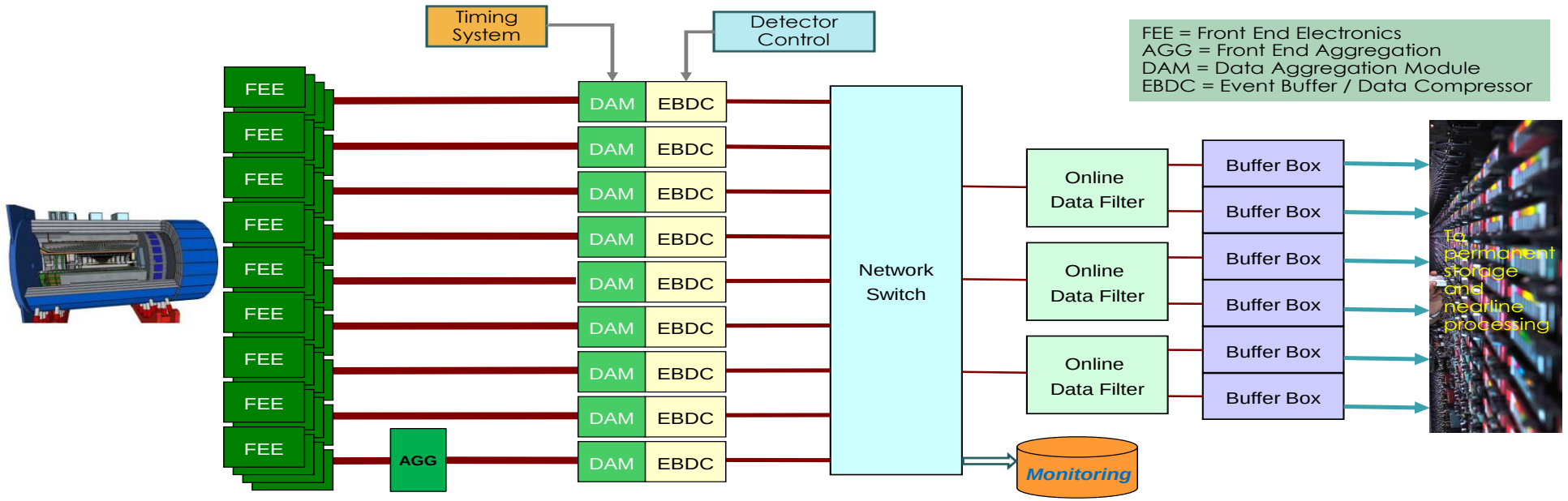
# Streaming DAQ Architecture




- Wide acceptance in the community for a streaming DAQ scheme. This included the YR reference detector & all three EIC proposals
- No External trigger
- All collision data digitized but aggressively zero suppressed at FEE
- Low / zero deadtime
- Event selection can be based upon full data from all detectors (in real time, or later)
- Collision data flow is independent and unidirectional -> no global latency requirements
- Avoiding hardware trigger avoids complex custom hardware and firmware
- Data volume is reduced as much as possible at each stage
- The “Front End Processing”, programmable hardware between the FEEs and the DAQ computers, is deemphasized relative to the yellow report, but should not be precluded.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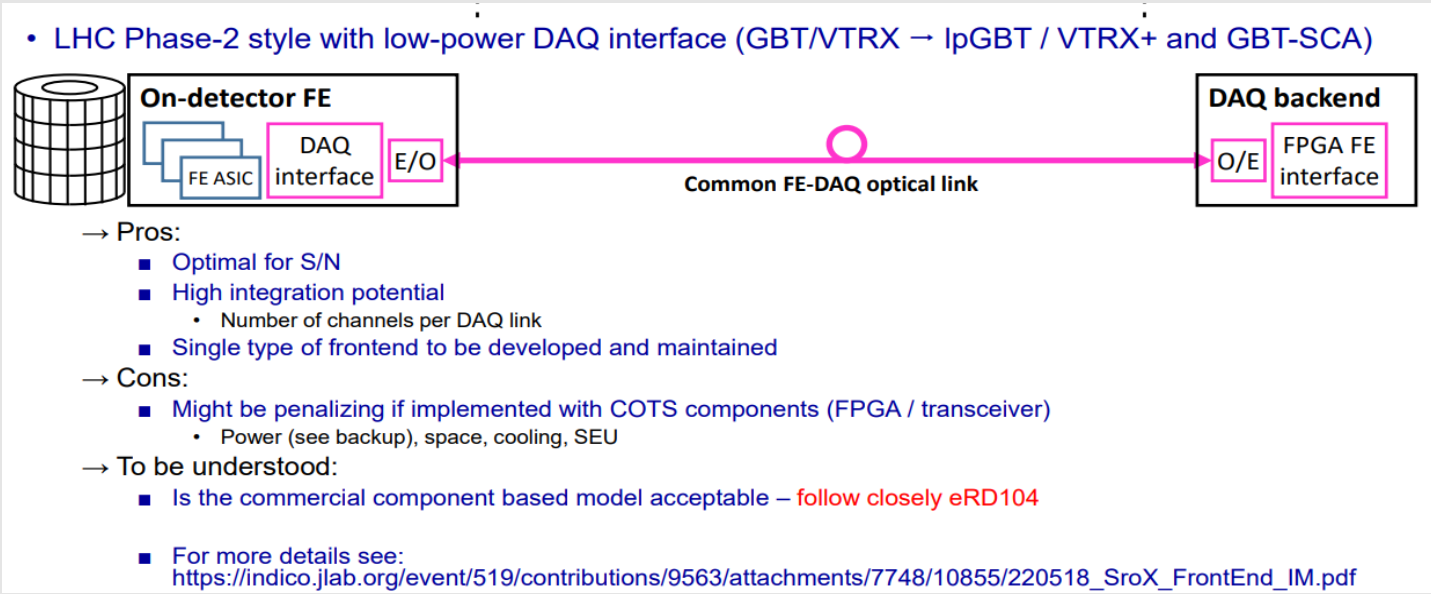
# FEE Organization

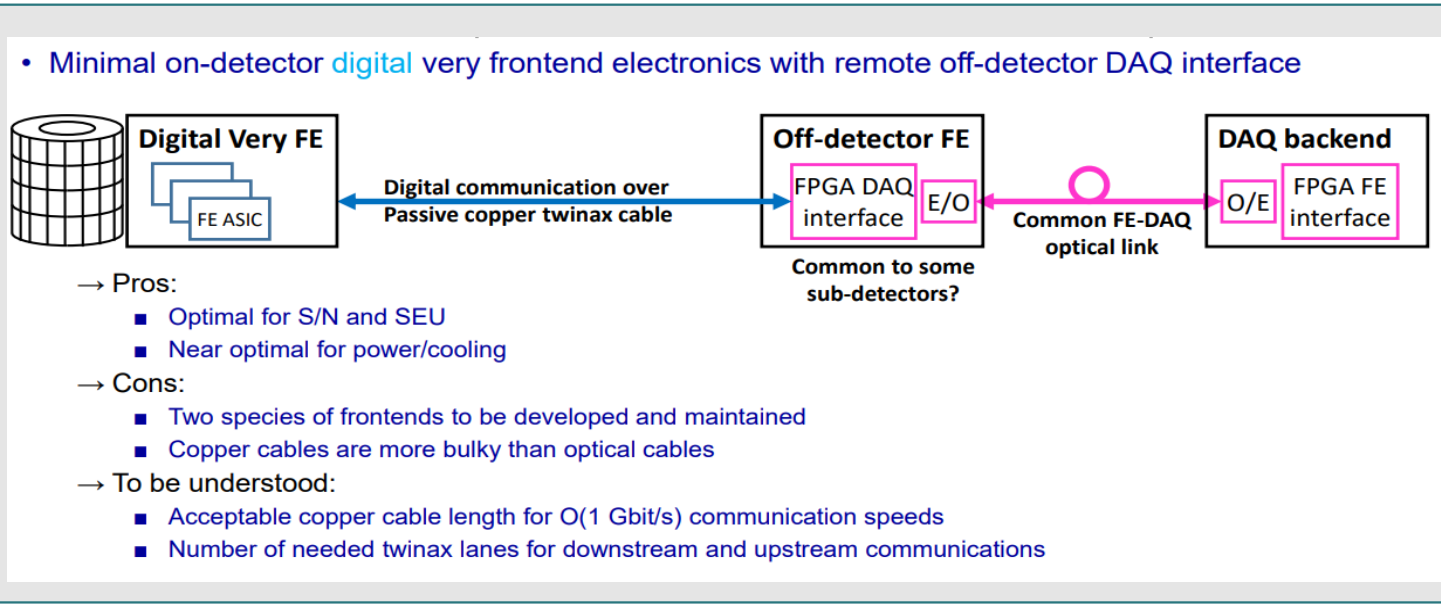
The FEE organization will contribute to the selection of the components:

One of the first decisions we made is whether we need the lpGBT

For EIC the main advantage of lpGBT would be the low power use (<1/4 of FPGA solutions), and low-jitter recovered clock distribution

Disadvantages outweigh the advantages for us, and include the 40MHz clock, and procurement/support



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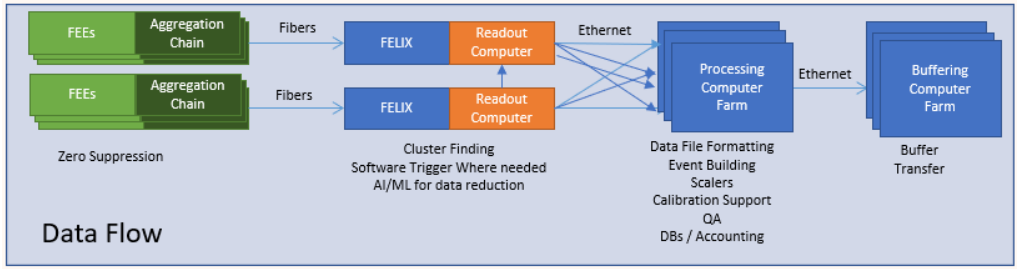
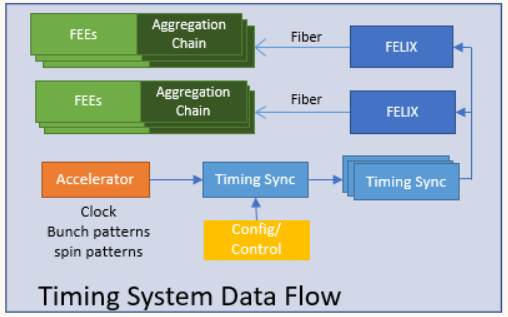
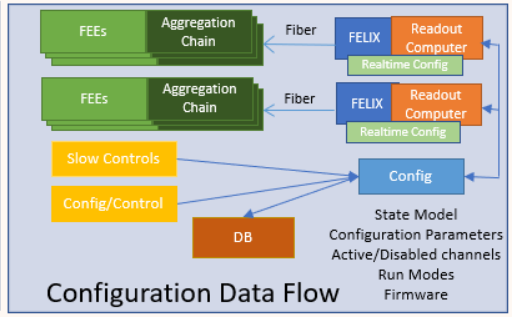
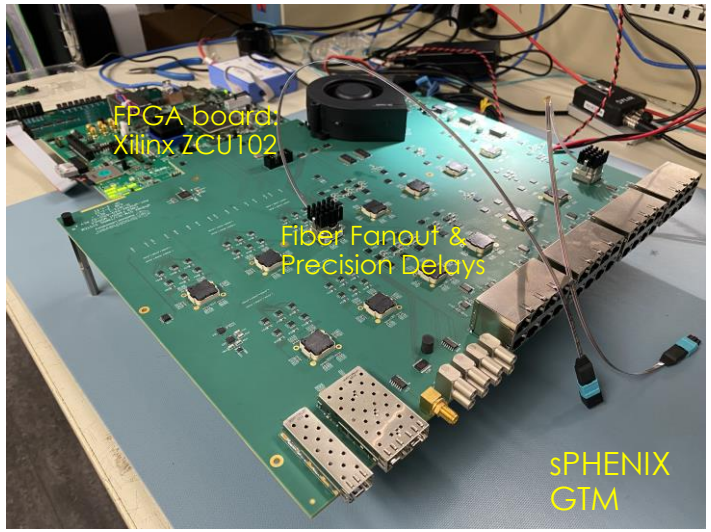
# Timing System: Synchronization and Fast Control

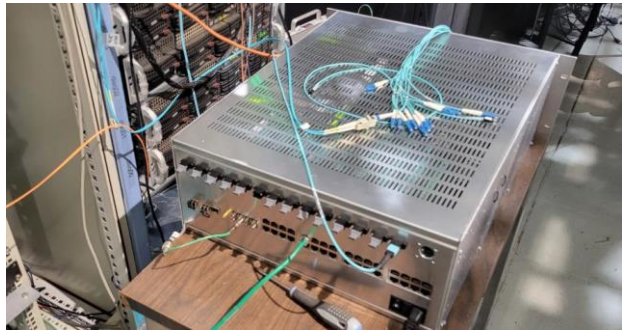
- Need fast control system (for control/feedback/sync) that is O(10ns) level
  - Distinct from slow/detector controls, routes with fixed timing constraints
- Fast Control Topics:
  - Beam crossing counter
  - Precision timing distribution (e.g., TOF O(10-20ps))
  - Synchronization and fast control
  - Busy feedback and flow control; potential triggers
  - Accelerator Interface: Spin states, luminosity, polarization, etc.
  - FEE clock counters resets



- Synchronization: Some multiple of beam clock (98.5MHz)
  - e.g., 8 Gbps can transmit 8 bytes per beam clock
- Maintain master non-reverting BX counter
  - e.g., 64bits never rolls over in lifetime of EIC (6k years)
- Transmit section of BX counter (20-40bits) to DAM & FEE to embed directly into hit data
- Strawman: sPHENIX "Global Timing Module" (GTM)

e.g. sPHENIX GTM: embedding 12 bytes at 6 times 9.4 MHz beam clock

| clock count | | 0 | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|---|
| bits 0-7 | mode bits/BCO | mode bits | BCO bits 0-7 | BCO bits 8-15 | BCO bits 16-23 | BCO bits 24-31 | BCO bits 32-39 |
| bit 8 | beam clock | 1 | 0 | 0 | 0 | 0 | 0 |
| bit 9 | LVL1 accept | X | 0 | 0 | 0 | 0 | 0 |
| bit 10 | endat0 | X | X | X | X | X | X |
| bit 11 | endat1 | X | X | X | X | X | X |
| bit 12 | modebit en. | 1 | 0 | 0 | 0 | 0 | 0 |
| bits 13-15 | | 3 user bits | 0 | 1 | 2 | 3 | 4 |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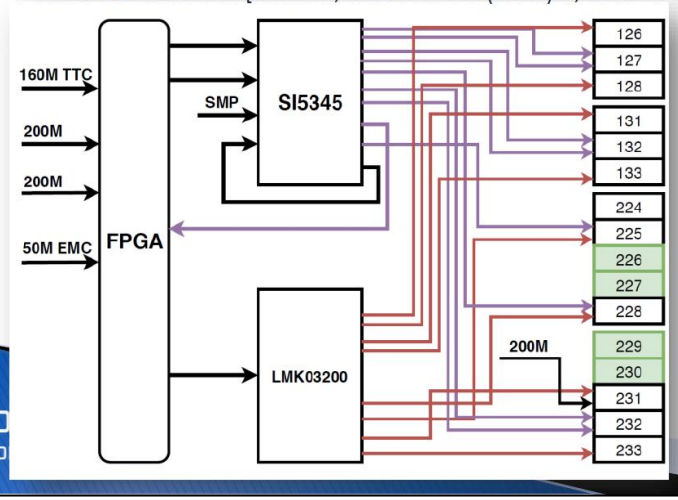
# Dedicated Clock Distribution (as demonstrated in FELIX)

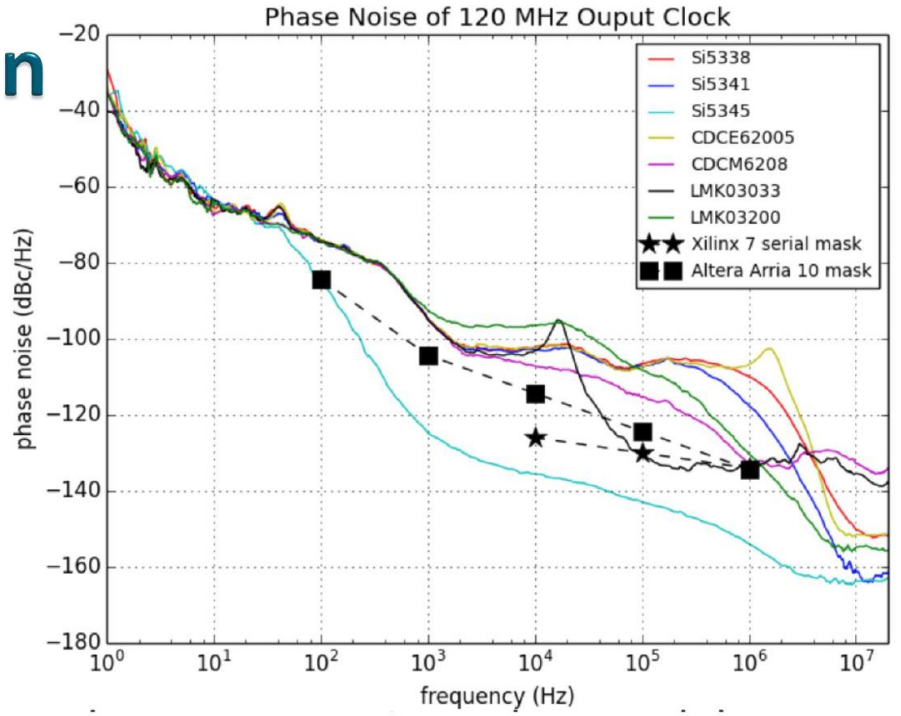
## Clock distribution precision

- FELIX is designed with clock jitter to provide stable clock to FEE
- Precise enough for robust transceiver lock, ps-level at 10kHz-1MHz in current part selection
- Caveat is sync over many FELIX's clock over many detector components and all frequency ranges, e.g AC-LGAD TOF and beam line detector.
  - Contribute to the uncertainty of TOF measurement, 20-30 ps total uncertainty
  - Therefore, ToF should consider a dedicated precision clock distribution, monitoring and calibration

FELIX v712 clock tree [K. Chen, IEEE TIM. 69 (2019) 7, 4569-4577]




[K. Chen, ATLAS Phase-I FELIX Design Review]




| Device | SI5338 | SI5345 | SI5341 |
|---|---|---|---|
| Jitter (ps) | 8.58 | 0.09 | 6.39 |
| Device | CDCM6208 | LMK03200 | LMK03033 |
| Jitter (ps) | 2.06 | 5.91 | 2.74 |
| Device | CDCE62005 | | |
| Jitter (ps) | 8.61 | | |

The jitter from 10 kHz to 1 MHz

Jin Huang <jihuang@bnl.gov> Streaming Readout workshop X 17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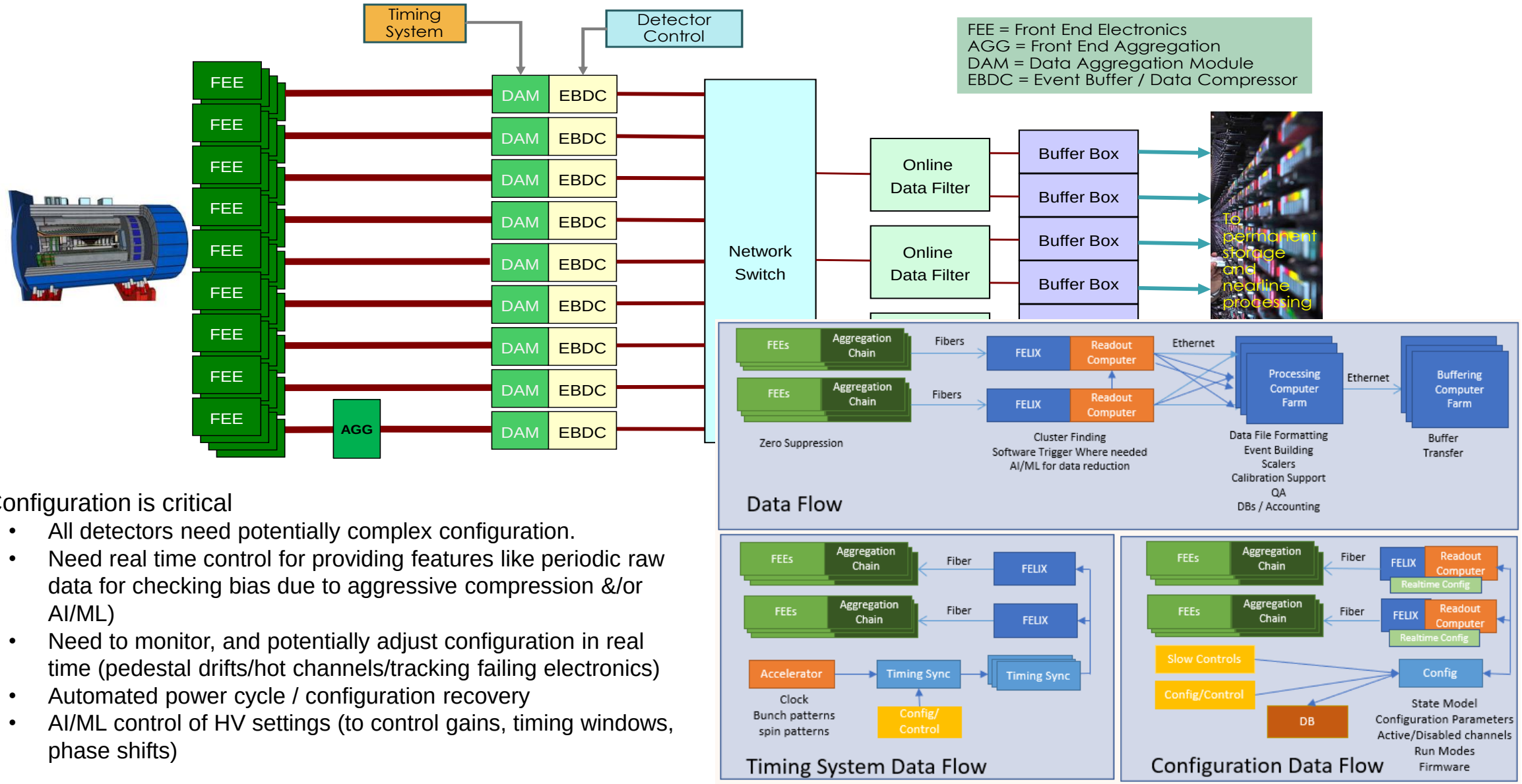
# Detector "Slow" Control System




- Configuration is critical
  - All detectors need potentially complex configuration.
  - Need real time control for providing features like periodic raw data for checking bias due to aggressive compression &/or AI/ML)
  - Need to monitor, and potentially adjust configuration in real time (pedestal drifts/hot channels/tracking failing electronics)
  - Automated power cycle / configuration recovery
  - AI/ML control of HV settings (to control gains, timing windows, phase shifts)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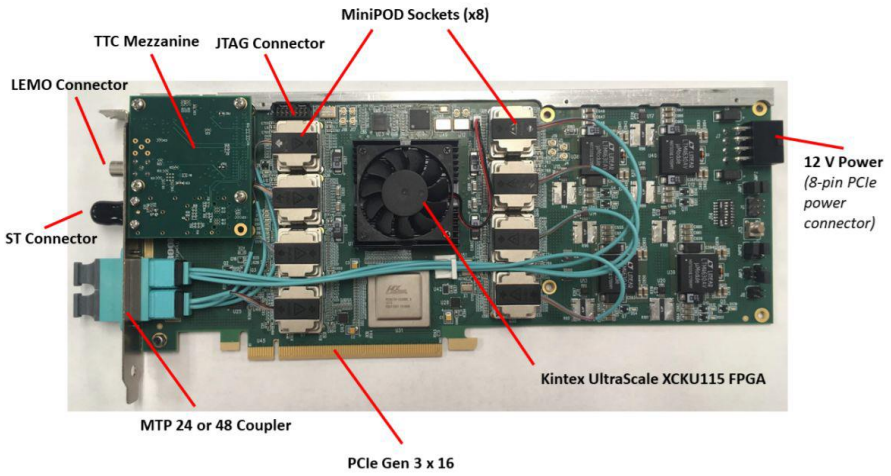
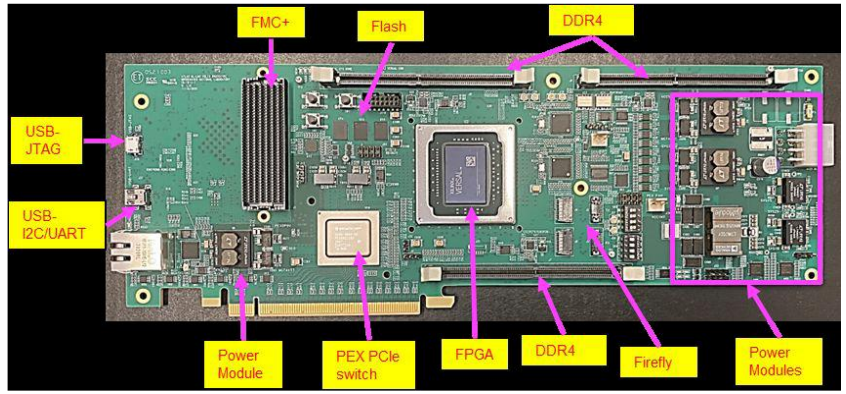
# DAM Candidate: ATLAS "FELIX"




Current ATLAS Phase 1/ sPHENIX FELIX BNL-712v2

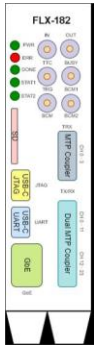


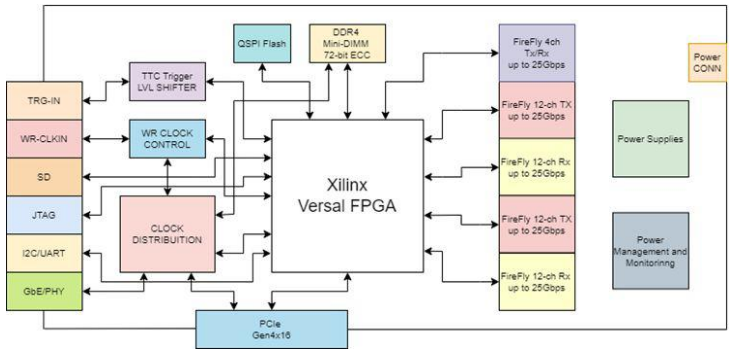

FELIX FLX-181 Prototype (BNL)

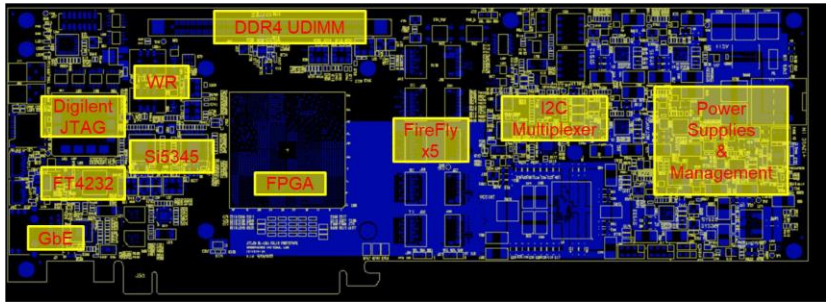
Assembled 24ch FLX-181 with 25 Gbps FireFly FMC+

(Hao Xu, BNL, DAQ WG meeting 7/21)

Current Design of FELIX FLX-182





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# FELIX Status

## FLX-182 Status

- Design passed FELIX review, will be sent out for fabrication in this week
- First assembled board is expected to be delivered in early September 2022
- 7 boards will be produced if there's no big design issues, by December 2022
- Small production for more boards is possible once FPGA is available

## Architecture and Interfaces

- PCIe Gen 4 x 16 lanes
- Transceiver
  - Transceiver Type: Samtec FireFly transceiver
  - Transceiver Speed: up to 10 Gb/s ("CERN-B") or 25 Gb/s
- Number of Optical Connectors per Card
  - At least 24 bi-directional connections to front-end electronics
  - A separate bi-directional connection to the TTC/BUSY system
- Configuration
  - Boot from JTAG/QSPI/SD card
  - Remote FPGA configuration from Multiple Flash Partitions
- DDR4/Flash Memory/SD card
- I2C
- External Electrical Interface
- Voltage Protection
- Temperature Protection

## Plan for 48-ch FELIX

- FPGA: Versal Premium, e.g. VP1552
- Transceivers: Up to 100+ GTYP/GTM
- PCIe Gen 5 up to 16 lanes
- If FPGA is available as planned, design will start in Q1 of 2023, first board is expected to be available in Q3 2023.

# Scale of System

## ECCE

| Detector system | DAM boards | Channel/Fiber Count |
|---|---|---|
| **Barrel** | | |
| Si Tracker | 4 | 100 fibers |
| uRWell | 12 | 278,000 channels, 576 fibers |
| AC-LGAD TOF | 30 | 1400 fibers |
| hpDIRC | 5 | 200 fibers |
| BECAL | 2 | 9,088 channels , 72 fibers |
| iHCAL + oHCAL | 1 | 3,264 channels, 26 fibers |
| **Forward** | | |
| AC-LGAD TOF | 6 | 300 fibers |
| dRICH | 5 | 220 fibers |
| FEMC | 8 | 47,850 channels, 375 fibers |
| LFHCAL | 10 | 58,590 channels, 460 fibers |
| **Backwards** | | |
| mRICH | 7 | 288 fibers |
| AC-LGAD TOF | 3 | 150 fibers |
| EEMC | 1 | 2878 channels, 24 fibers |
| **Far-Forward** | | |
| B0 Detector, Roman Pots, Off-Momentum Detectors, ZDC | 26 | 7.4M |
| **Far-Backward** | | |
| Luminosity Monitor & Low-$Q^2$ Tagger | 18 | 4.9M |
| Sum | **138** | |

## ATHENA

| Detector | Number of Channels | Detector Readout Technologies |
|---|---|---|
| DIRC | 100k | MCP-PMT |
| DRICH | 300k | SiPM * |
| ERICH | 225k | SiPM * |
| EcalBarrelScFi | 4000 | SiPM using FPGA based readout boards derived from the STAR DET-ADC board |
| EcalEndcapN | 3080 | SiPM |
| EcalEndcapP | 26600 | SiPM |
| EcalImgBarrel | 619M | MAPS* |
| HcalEndcapN | 10000 | SiPM |
| HcalEndcapP | 2375 | SiPM |
| HcalBarrel | 26600 | SiPM |
| Inner Vertex Tracker | 60B | MAPS* |
| MPGDTrackerBarrel | 66k | Micromegas |
| urWELLTrackerEndcap | 50k | uRWELL |
| GEMTrackerEndcap | 28k | GEM |
| B0Silicon [[2]] [3] | 400M | MAPS* |
| B0preshower | 260k | AC-LGAD readout with ALTIROC ASIC |
| RP | 550k | AC-LGAD readout with ALTIROC ASIC |
| OffM | 320k | AC-LGAD readout with ALTIROC ASIC |
| ffiZDCSi | 213k | Silicon strip detectors - DC-LGADs |
| ffiSDCSciFi | 576 | PMTs |
| ZDCSiPb | 500k | If silicon used, less if silicon fibers used. |
| ZDCScint | 36-72 | PMTs; depends on whether two sections are read-out indepdenently. |
| TOF | 332k | AC-LGAD |
| Luminosity monitoring and Low Q tagging | 4000 | 6 PMT based calorimeters * |

Reconciliation is in progress (see backup slides)
But roughly:

- 4.5k Fibers,
- 2.5M channels + 12k MAPS sensors (72B MAPS pixels)
- 120-140 Felix Boards

Huge number of channels but (relative to CERN) small total data throughput.

The number of fibers are set by detector and electronics topology and position, not data throughput.

Noise reduction is key! One hit/bunch crossing could require 5% of full data bandwidth!


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# ASICs R&D

| ASIC Proposed | Detector | Institution(s) | R & D |
|---|---|---|---|
| ALCOR | RICH | INFN | Current version for low rate. Increase data throughput. Test streaming mode |
| ASTROPIX | Imaging Barrel eCAL | ANL in collaboration with NASA | Customization for Imaging calorimeter, improved power and energy resolution |
| ALPIDE ITS3 | Si Tracker | EIC R&D Silicon Consortium in collaboration with CERN | 65nm technology ITS3, lower material budget |
| SALSA | MPGD | CEA SACLAY in collaboration with University of Sao Paulo | Update version of SAMPA for better performance and better support for streaming |
| ALTIROC | TOF | Omega / CEA SACLAY / CNRS | Customization for EIC / AC-LGAD streaming |
| HDSOC64 | DIRC, ZDC | NALU | 64 channels version of HDSOC |
| HGCROC | Calo's | Omega Microelectronics | 40MHz -> 50MHz? Streaming? |
| MAROC 3A | RICH | WeeRoc / CAEN / Omega | Long conversion time (102 us), 12-bit @ 40 MHz |

Advanced prototype for TDR - start production around 2026 and ASIC choice will be frozen at that date
All ASICs are based on existing design : development of new chip mostly for improved data links for better rate capability and streaming support making the R&D fairly low risk,
SALSA is a new iteration of SAMPA with higher channel density / higher sampling rate / lower power consumption
Other ASICs will be chosen in conjunction with project from available ASICs for better standardization

- ~July 2022 - capture all major updates and initiate any needed R&D initiatives.
- ~May 2023 - finalize input into P6.

# Some Comments on the ASICs mentioned…

- MAROC will likely not be used with the (slow) ADC method, but only hit info. ALCOR is favored over MAROC..
- ASTROPIX and HGCROC are designed for 40MHz, how to use them with 100MHz is still being discussed…
- HDSOC could work almost everywhere for calorimeters, but maybe FADC would be better suited for streaming (e.g., FADC chips from ALPHACORE or Pacific Microchip)…

# Backup



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# Summary of Proposed Data Reduction Techniques

- ❑ Timing windows with respect to the collision time (FEE)
- ❑ Zero Suppression (FEE)
- ❑ Elimination of hits not part of tracks (AI/ML tracking in FEP, or any point later)
- ❑ Elimination of hits not part of Cherenkov rings (AI/ML in FEP, DAM, or EBDC)
- ❑ Feature Extraction (FEE, or any point later)
- ❑ Cluster Finding (DAM, or any point later)
- ❑ Software Trigger (DAM, or EBDC)
- ❑ Lossless compression (EBDC or later)

We should also investigate features to keep the data clean in order to improve the above techniques

- ❑ Automated thresholds (ex. pedestals)
- ❑ Automated filters for common mode noise suppression
- ❑ Dynamic control of calibrations in slow controls &/or FEEs
- ❑ Dynamic monitoring / removal of aberrant channels
- ❑ Automated recovery of single bit upsets

| Tracking Detector Specific Requirements | Spec | DAM Boards |
|---|---|---|
| Tracking | 7 m^2 MAPS ITS-2 & ITS-3 sensors | |
| 3 layers silicon for vertex | ITS-3 curved silicon | |
| 2 layers silicon for sagitta | ITS-2 type staves but ITS-3 improvements | |
| 4 layers silicon disks backward | | |
| 5 layers silicon disks forward | | |
| 3 layers of MPGD | | |
| | | |
| MAPS | 5GB/sec total throughput | |
| | 71B pixels | |
| | 12k MAPS sensors | |
| | ~300 data fibers | 6 |
| | | |
| MPGD | | |
| | 100k channels | |
| | <10Gb/sec total zero-suppressed data volume | |
| | Assume 512 channels per FEE (with 8 ASICs) | |
| | 200 FEEs / data fibers | 4 |
| | 10Gb/sec -> .05Gb/sec per fiber | |
| | Iraqli estimate -> 1.9Gb/sec per fiber | |
| | | |
| Use Reconstructed clocks to avoid fiber proliferation | | |

| Calorimeters Specific Requirements | Spec | DAM Boards |
|---|---|---|
| Forward ECAL (PbWO (+SiGlass)) | 3000 channels | |
| Backward ECAL | 3000 channels | |
| | | |
| Barrel ECAL | 8000 channels | |
| Imaging Barrel ECAL (If used) | 10,000 Pb/SciFi | |
| | 50M channels Astropix<br>"2 level data aggregation inside detector, 1 data link per stave<br>Count of Staves? | |
| | | |
| Barrel HCAL (ECCE version) | 3,000 channels | |
| (Athena version) | 26,600 channels (off detector electronics) | |
| | | |
| Forward pECAL (Athena Version) | 25,000 channels (off detector electronics) | |
| | | |
| Forward FHCAL (Ecce Style) | 60,000 channels | |
| High granularity HCAL inset | 8k channel | |
| | | |
| Except for the Imaging barrel all SiPM | ~110k channels | |
| | Assume 64 channels / FEE -> 1600 fibers | 34 |
| Backward HCAL uncertain. | | |
| Use Reconstructed Clock to reduce fiber | | |

| Far Forward Specific Requirements | Spec | DAM Boards |
|---|---|---|
| B0 | | |
| 3 MAPS layers | 300M Pixel (3x20x20cm @ 20x20 um pitch. ~300 sensor) | |
| 1 AC-LGAD | 150k (500x500um pitch assumed) | |
| | | |
| | | |
| 2 RP and 2 OffM | | |
| 4 x 500k AC-LGAD layers | 8M total channels | |
| | | |
| ZDC | | |
| Crystal | 400 channels APD | |
| 32 x 2600 ch silicon pad | 11,520 HGCROC as per ALICE FoCal-E pad layers | |
| 4 x 40,000ch silicon pixel | 160k | |
| 2 boxes scintillator | 72 | |

| Far Backward Specific Requirements | Spec | DAM Boards |
|---|---|---|
| Low-Q tagger 1: 2 layers of (40x40cm) (500umx500um pitch) | 1.3M | |
| | | |
| Low-Q Tagger 2: 2 layers of (30cmx20cm) (500umx500um pitch) | 480k | |
| (or smaller…) | | |
| 2 Calorimeters | 700 Channels total | |

| Cherenkov PID Specific Requirements | Spec | DAM Boards |
|---|---|---|
| dRICH | 300k channels | |
| | Max dark current rate 1830 Gb/sec | |
| | 40Gb/sec fiber | |
| | Dedicated Timing fiber for timing window application | |
| | ~310 fiber (assuming 64 channel FEB + 16 FEB x ROB) and 6.5Gb/sec fiber | ~24 |
| | | |
| pfRICH (if used) (assume 75% of dRICH) | 225k | |
| | | |
| mRICH | ? | |
| | | |
| DIRC | 100k channels | |

| TOF Specific Requirements | Spec | DAM Boards |
|---|---|---|
| Channels | | |
| Depends on strip size (.5mm x 1cm or .5mm x .3cm) and/or pixel size (.5mm x .5mm) | 3-50M channels | |
| | | |
| fibers | 240 - 500 | 5 – 10 |
| Rate per fiber | .5Gb/sec – 5 Gb/sec | |
| Rates to tap | 4-6 Gb/sec | |
| | | |
| Dedicated fiber for high resolution clock | | |