

# INTT Stuff Meeting Material

RIKEN/RBRC

Itaru Nakagawa

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1. INTT Software Management
2. Software with FELIX Readout Test/Development
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# Software Manpower Potential Resources

	BNL	Purdue	RIKEN	NWU	JAERI	Taiwan
	Rachid	Wei	(Yasuyuki)	Takashi	Shoichi	Ming
	Raul		Itaru	Maya		Rong-Shyang
PD		Milan	Genki			
Ph.D Candidate						Kai-Yu
2 <sup>nd</sup> Year Graduate			Hikaru	Yumika Runa		Cheng-Wei
1 <sup>st</sup> Year Graduate		Joseph?		Yuka		Wei-Che
UG			Tomoya, Ryota, Kazuma			

# Software Tasks

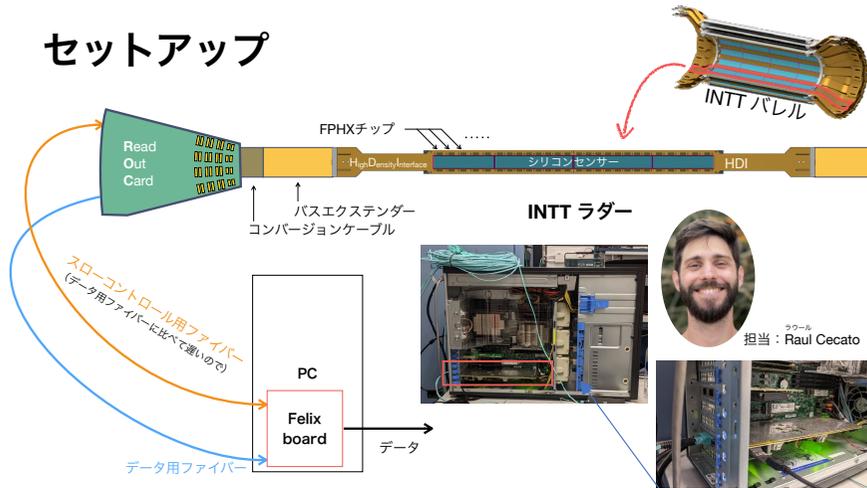
\*Need FELIX environment for development/testing

Item	Personnel/Institute	Comment
GEANT INTT Model	Genki (RBRC)	
Track Reconstruction	Cheng-Wei (NCU)?	To be a member of the big offline software group.
Online Monitor	Joseph, Wei (Purdue)	
Unpacker*	Joseph (Purdue)	
Ladder QA Database	Milan (Purdue)	
LV, Bias Control GUI	Steve Boose (BNL)	
Expert GUI*		FPHX parameter control
DAQ operation database*		Record FPHX parameters in DB
DAQ start script*	DAQ group + INTT personnel	SC sequences
Calibration/Pedestal Scripts*		Automated script. Dump results into DB.
FELIX FPGA	Raul + INTT personnel	

Else?

# Transition to FELIX Readout

## セットアップ



Courtesy of Genki

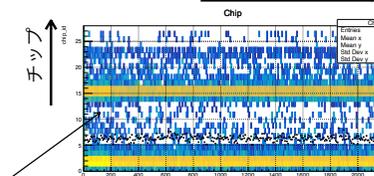
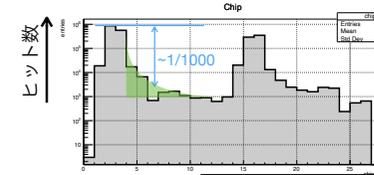
Server \$8,000

## データ

#26	#25	#24	#23	#22	#21	#20	#19	#18	#17	#16	#15	#14
#13	#12	#11	#10	#9	#8	#7	#6	#5	#4	#3	#2	#1

### FEM リードアウト

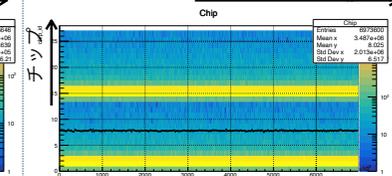
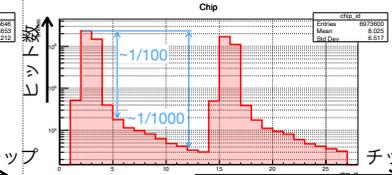
測定時間 (分) 5  
 パラメーター Module, chip, ch, ADC, BCO, BCOfull, etc



Cut: module==6 → C3 ポート

### Felix リードアウト

測定時間 (分) 5  
 パラメーター Chip, ch, ADC, BCO.



Cut: なし

- Should shift from FEM-NIDAQ base standalone to FELIX base readout in BNL test bench as long as the FELIX is ready for testing.
- Need 2<sup>nd</sup> FELIX test bench. Purchase another \$8,000 server and FELIX board (available?)

# Transition to FELIX Readout



- It is important to have an environment for Raul's development and testing/our control software development simultaneously. This way, Raul and we can feed back each other.

# Expert GUI

- Can be modified from FVTX version
- Written in python

FVTX Expert GUI - WikiOffline

2019/06/01 14:58

The FVTX Expert GUI was developed in python using Tk support through the Tkinter library. phoenix20 is the only machine in 1008 that has an appropriate python installation.

Unfortunately, phoenix20 is also the only machine that has broken remote password login. You can only log in directly to phoenix20 as phoenix if you have added your public key to the authorized\_keys file on the phoenix account.

## Organization

The FVTX Expert GUI is organized into four tabs:

- Slow Control
- Power Map
- Latch Database
- Bias Control

Additionally the Slow Control tab is organized into four additional levels

- Detector
- ROC
- Wedge
- Chip

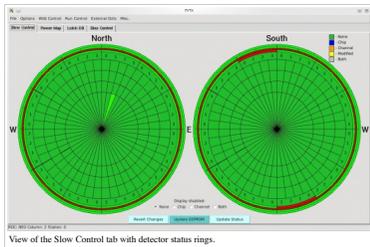
## Slow Control

### Graphical Representation

The Slow Control tab of the expert GUI is comprised of the frontal view of both detector arms (North/South) when looking *out* from the interaction point.

As such, the locations of **East** and **West** are reversed for each arm.

To aid in orientation **E** and **W** labels are placed in the corresponding locations.



View of the Slow Control tab with detector status rings.

- From the inside out the various layers of information provided are:
  - Station 0 wedges
  - Station 1 wedges
  - Station 2 wedges
  - Station 3 wedges
  - ROCs
  - The numbering here is the ROC *column* of the wedges in that same phi slice
  - Status rings

[https://www.phenix.bnl.gov/WWW/offline/wiki/off/index.php/FVTX\\_Expert\\_GUI#Overview](https://www.phenix.bnl.gov/WWW/offline/wiki/off/index.php/FVTX_Expert_GUI#Overview)

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Side 0 Chip Settings [Editable]						Side 0 Controls					
Vref	1	1	1	1	1	Vref	1	1	1	1	1
DAC 0	8	8	8	8	8	DAC 0	8	8	8	8	8
DAC 1	16	16	16	16	16	DAC 1	16	16	16	16	16
DAC 2	32	32	32	32	32	DAC 2	32	32	32	32	32
DAC 3	48	48	48	48	48	DAC 3	48	48	48	48	48
DAC 4	80	80	80	80	80	DAC 4	80	80	80	80	80
DAC 5	112	112	112	112	112	DAC 5	112	112	112	112	112
DAC 6	144	144	144	144	144	DAC 6	144	144	144	144	144
DAC 7	176	176	176	176	176	DAC 7	176	176	176	176	176
N1Sel	6	6	6	6	6	N1Sel	6	6	6	6	6
N2Sel	4	4	4	4	4	N2Sel	4	4	4	4	4
FB1Sel	4	4	4	4	4	FB1Sel	4	4	4	4	4
LeakSel	0	0	0	0	0	LeakSel	0	0	0	0	0
P3Sel	0	0	0	0	0	P3Sel	0	0	0	0	0
P2Sel	4	4	4	4	4	P2Sel	4	4	4	4	4
G5Sel	2	2	2	2	2	G5Sel	2	2	2	2	2
BW5Sel	4	4	4	4	4	BW5Sel	4	4	4	4	4
P15Sel	5	5	5	5	5	P15Sel	5	5	5	5	5
InjSel	0	0	0	0	0	InjSel	0	0	0	0	0
LVDS Current	7	7	7	7	7	LVDS Current	7	7	7	7	7
Accept Hits	<input checked="" type="checkbox"/>	Accept Hits	<input checked="" type="checkbox"/>								
Global Inject	<input type="checkbox"/>	Global Inject	<input type="checkbox"/>								
Serial Select	0+1	0+1	0+1	0+1	0+1	Serial Select	0+1	0+1	0+1	0+1	0+1
Channel Mask	<input checked="" type="checkbox"/>	Channel Mask	<input checked="" type="checkbox"/>								

Wedge level window for modifying register values. All fields are editable.

Reg	Desc	Value
3	Vref	1
4	DAC 0	8
5	DAC 1	16
6	DAC 2	32
7	DAC 3	48
8	DAC 4	80
9	DAC 5	112
10	DAC 6	144
11	DAC 7	176
12	N1Sel	6
12	N2Sel	4
13	FB1Sel	4
13	LeakSel	0
14	P3Sel	0
14	P2Sel	4
15	G5Sel	2
15	BW5Sel	4
16	P15Sel	5
16	InjSel	0
17	LVDS Current	7
2	Accept Hits	<input checked="" type="checkbox"/>
2	Global Inject	<input type="checkbox"/>
2	Serial Select	0+1

["https://www.phenix.bnl.gov/WWW/offline/wiki/off/index.php/FVTX\\_Expert\\_GUI"](https://www.phenix.bnl.gov/WWW/offline/wiki/off/index.php/FVTX_Expert_GUI)

# sPHENIX DAQ

- Do we have standalone rc like PHENIX?
- How many BCLKs before the trigger decision?
- How events are built thru EBDC?
- Etc..

**uBNL Journal Club**  
 Date/Time: Wednesday 23 February 2022 from 17:00 to 18:00  
 Location: BNL  
 Chair: Gabot David  
 Description: Zoom link  
<https://stonybrook.zoom.us/j/96552659346?pwd=al0cxd9qZGM4YTRWwW1DRFhXbStzd09>

Wednesday 23 February 2022  
 17:00 **sPHENIX DAQ (1100)** (transparencies)

Martin Purschke  
 (Brookhaven National Laboratory)

Powered by [CDS Agenda](#)

**DAQ Overview**

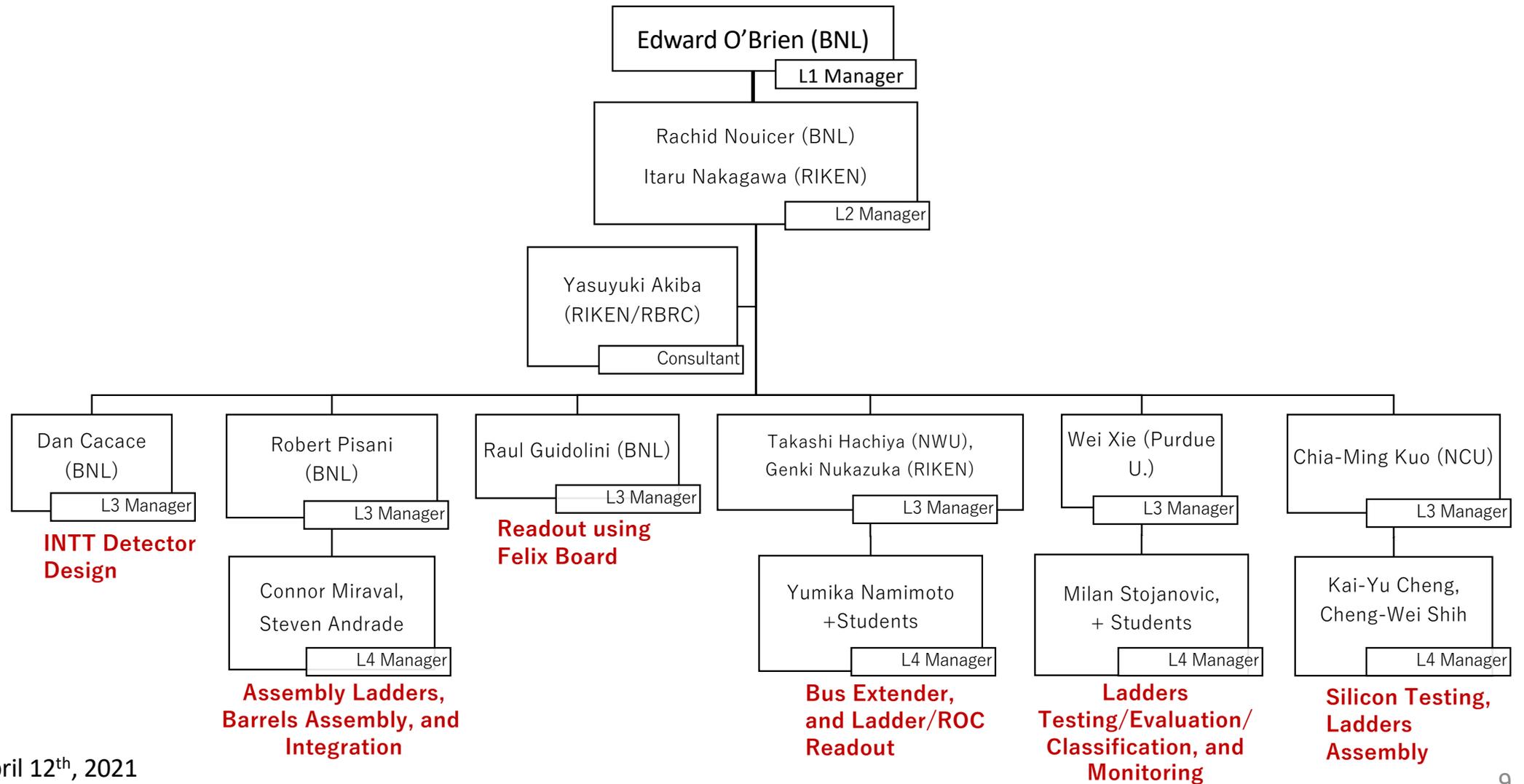
- DCM-2 receives data from digitizer, zero-suppresses and packages
- SEB collects data from a DCM group (~20)
- EBDC Event Buffer and Data Compressor (~40)
- Buffer Box data interim storage before sending to the computing center (6)

**On Detector** | **Rack Room**

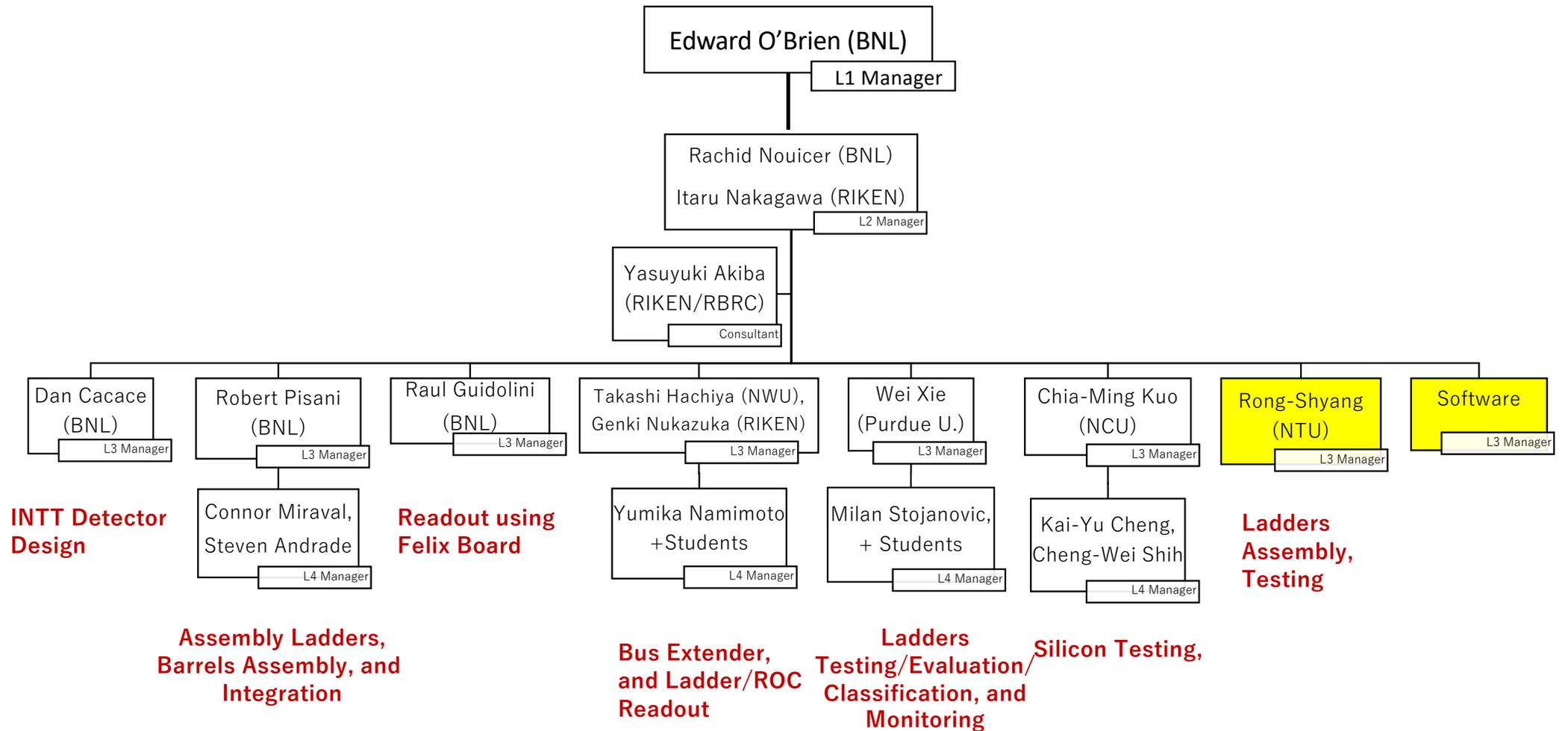
To HPSS (Computing Center)

We should be more familiar with sPHENIX DAQ system. Planning to invite Martin for QA session soon. 8

# Management Chart (Presented in the FELIX review)



# Management Chart (Update Proposal)



# Proposed plan for INTT Publications

Topics	Target Journal	Leading Author	Timeline	Remaining Issues
Bus Extender (Electric)	The Japan Institute of Electronics Packaging	Takashi Kondo (TIRI)	2022/May	To be announced from Takashi later
Bus Extender (Mechanical)	NIM	Takashi?	2022/Summer	Final evaluation of the yield rate
2021 Beam Test	ELPH Ann. Rprt. NIM	Genki?	2022/Summer	Efficiency (Thick tail by MC, BG contamination)
INTT Ladder	NIM	Itaru/Rachid?	2022/Summer	
INTT Barrel	NIM		2023	

# Backup Slides