

Zhenyu Ye @ UIC

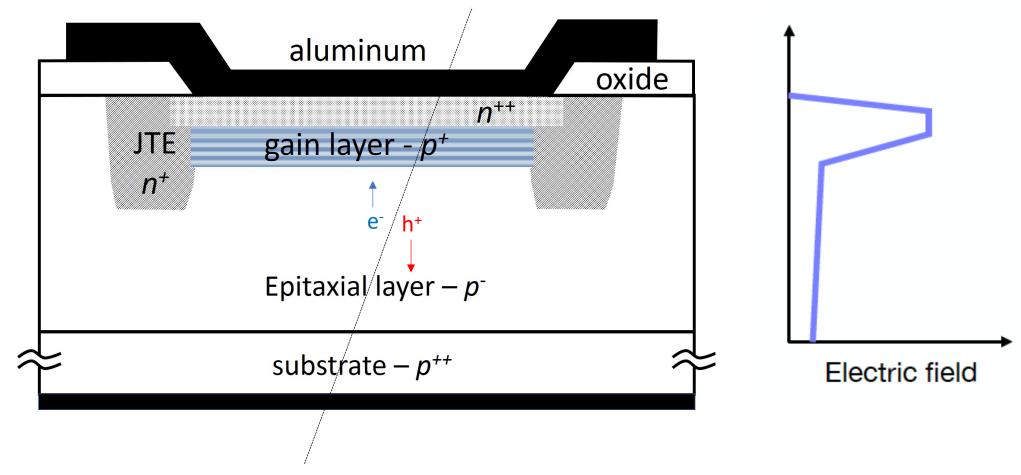
With inputs from colleagues @ BNL, CNRS/IN2P3 IJCLab/Omega, Fermilab, LANL, NCKU, Rice, ORNL, UC Santa Cruz

Meeting indico page: https://indico.bnl.gov/category/323/

Mailing list: https://mailman.rice.edu/mailman/listinfo/lgads-eic

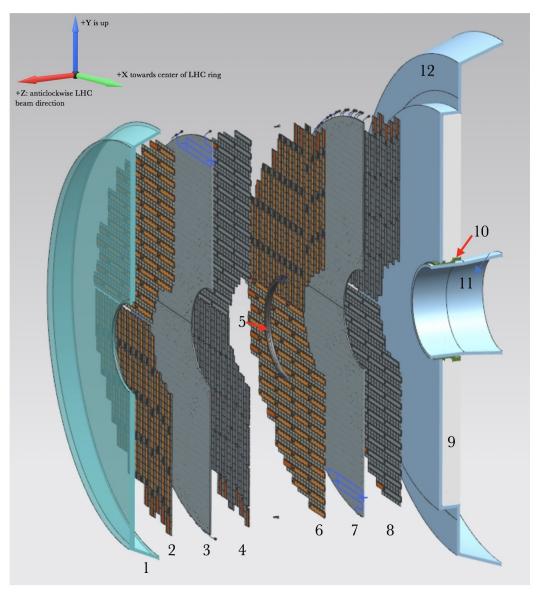
Proposal: https://wiki.bnl.gov/conferences/index.php/ProjectRandDFY22

Low Gain Avalanche Detector

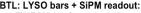


Ultra-fast silicon detectors with a highly doped p+ gain layer Moderate internal gain: 10-30

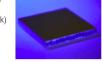
CMS Endcap Timing Layer



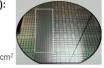
- 1: ETL Thermal Screen
- 2: Disk 1, Face 1
- 3: Disk 1 Support Plate
- E: Disk 1, Face 2
- 5: ETL Mounting Bracket
- 6: Disk 2, Face 1
- 7: Disk 2 Support Plate
- 8: Disk 2, Face 2
- 9: HGCal Neutron Moderator
- 10: ETL Support Cone
- 11: Support cone insulation
- 12: HGCal Thermal Screen

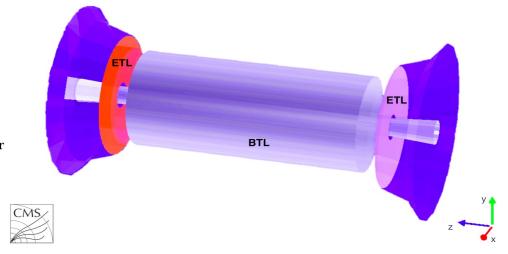


- TK/ ECAL interface: |n| < 1.45
- Inner radius: 1148 mm (40 mm thick)
- Length: ±2.6 m along z
- Surface ~38 m²; 332k channels
- Fluence at 4 ab⁻¹: 2x10¹⁴ n_{ss}/cm²



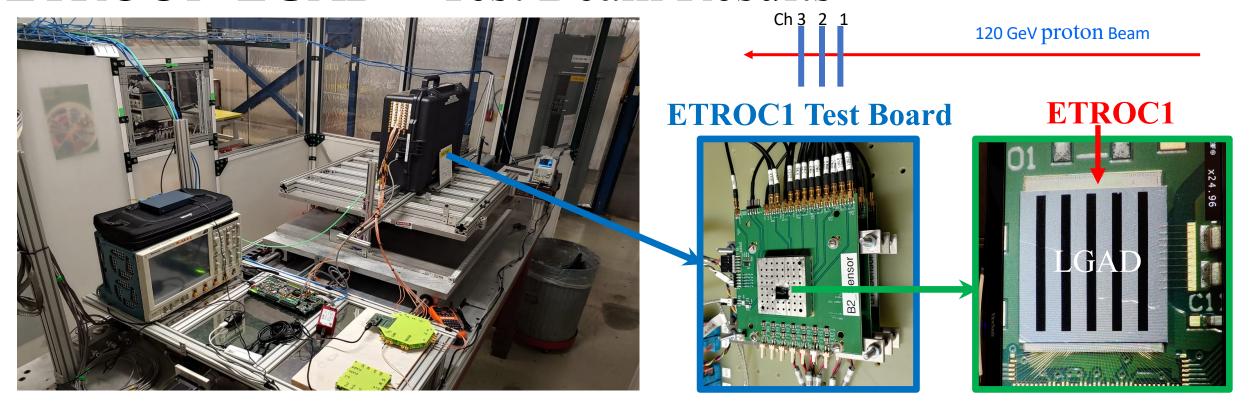
- ETL: Si with internal gain (LGAD):
- On the HGC nose: 1.6 < |η| < 3.0
- Radius: 315 < R < 1200 mm
- Position in z: ±3.0 m (45 mm thick)
- Surface ~15.8 m²; ~6M channels
- Fluence at 4 ab-1: up to 2x10¹⁵ n_{eq}/cm

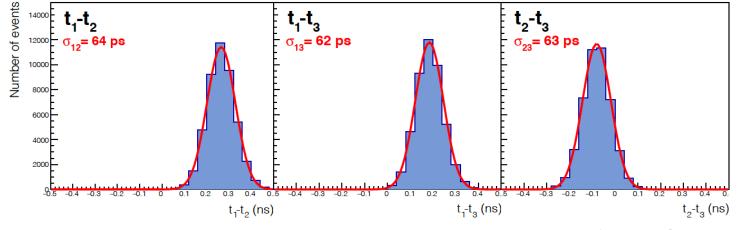




- On the CE nose: $1.6 < |\eta| < 3.0$
- Radius: $315 < R < 1200 \, mm$
- Position in Z: $\pm 3.0 m$ (45 mm thick)
- Surface $\sim 15.8 \, m^2$; $\sim 8.6 \, \text{M}$ channels
- Weight 282 kg/side; Power: 26kW/side
- Two disks on each side allowing up to two measurements per track
 - 50 ps per hit \rightarrow 35 ps per track

ETROC1+LGAD – Test Beam Results





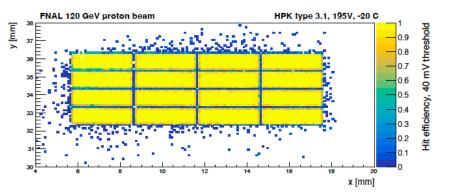
From preliminary analysis of the data from ongoing beam test at FNAL, the resolution of single LGAD+ETROC1 devices with large signal amplitude is 42-46 ps.

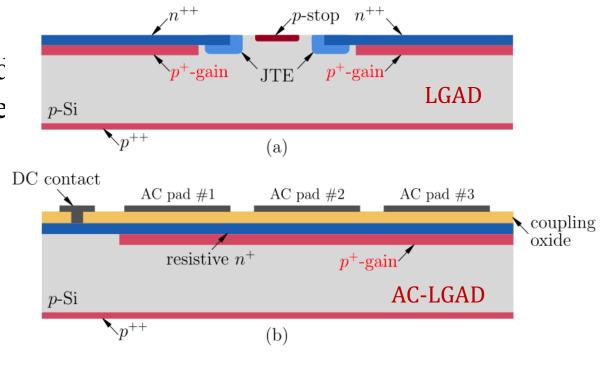
$$\sigma_i = \sqrt{0.5 \cdot \left(\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2\right)}$$

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AC-Coupled LGAD

• Due to the presence of JTE and the gap between LGAD cells, 100% fill factor can not be achieved in LGAD. The position resolution is limited to be $\sqrt{1/12}$ of cell size.





- AC-LGAD: replacement of the segmented n⁺⁺ layer by a less doped but continuous n⁺ layer. Electrical signals in the n⁺ layer are AC-coupled to neighboring metal electrodes that are separated from the n⁺ layer by a thin insulator layer.
- AC-LGAD not only provides a timing resolution of a few tens of picoseconds, but also 100% fill factor and a spatial resolution that are orders of magnitude smaller than the cell size.

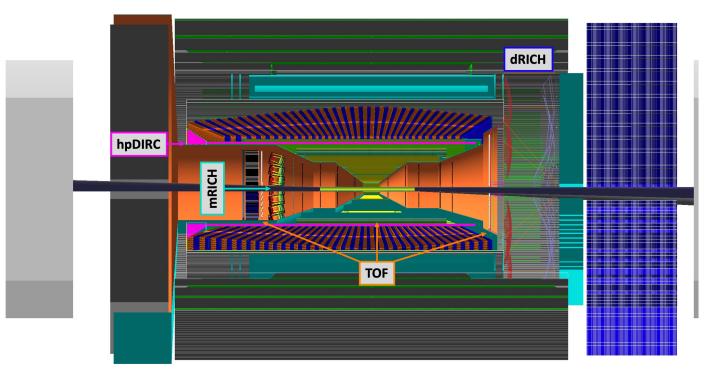
 Therefore, it is a good candidate for 4D detectors at future high energy experiments.

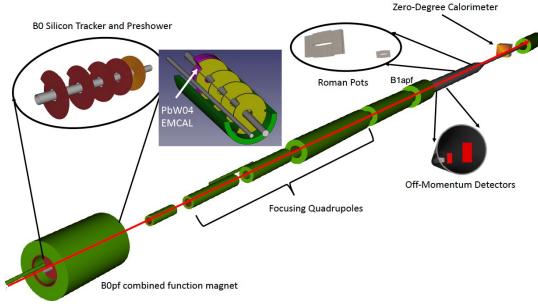
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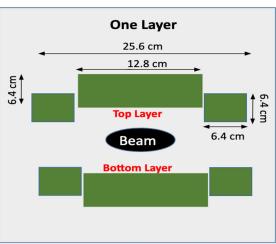
AC-LGAD at EIC

AC-LGAD for TOF/Tracking (G. Kalicy)

- Timing resolution: ~25 ps per hit
- Position resolution: ~30 μm with 500 μm pitch
- Total area: $\sim 15 \text{ m}^2$





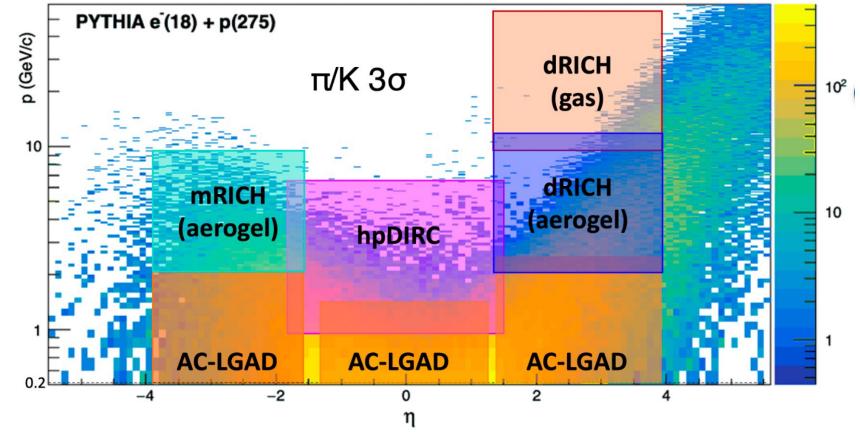


Option for Roman Pots (A. Jentsch):

- AC-LGAD with both fine pixilation (~140 um spatial resolution), and fast timing (~35 ps)
- MAPS + LYSO timing layer

TOF PID for EIC Detector-1

- A nearly 4π TOF coverage for $e/\pi/K/p$ PID at low-to-intermediate p range that sufficiently overlaps with RICH-based PID detectors to cover the interesting phase space at EIC.
- Explore novel technology (AC-LGADs, benefit the tracking) and leverage established designs (DC-LGADs for CMS/ATLAS) to minimize the cost.



- FTTL: 1.5<η<3.5 0.15
- CTTL: $|\eta| < 1.4$ $0.15 < p_T < 1.5 \text{ GeV}$
- ETTL: $-3.7 < \eta < -1.74$ 0.15

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eRD112: AC-LGAD for EIC

- AC LGAD detectors proposed for EIC
 - Roman Pots and B0
 - TOF for PID (and tracking)
- Have common designs in sensor, ASIC etc. when possible, combine R&D efforts [1]

LGAD $p ext{-Si}$ (a) DC contact AC-LGAD AC pad #3 AC pad #1 AC pad #2 coupling oxide resistive n^+ p^+ -gain $\searrow_{p^{++}}$ (b)

p-stop n^{+}

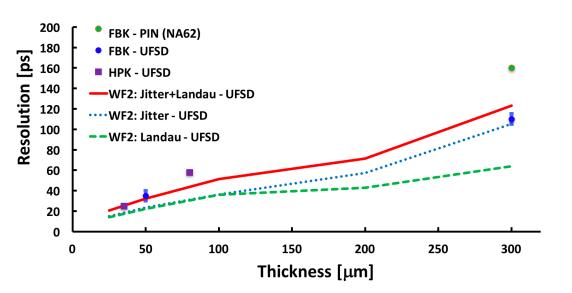
[1] https://wiki.bnl.gov/conferences/index.php/ProjectRandDFY22

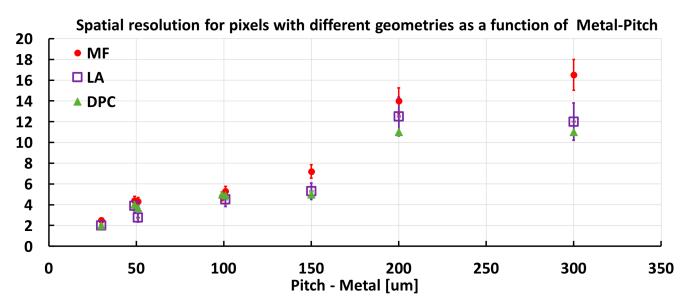
	Time resolution / hit	Position resolution / hit	Material budget / layer
Barrel ToF (Tracker)	<30 ps	(3-30 μm for Tracker)	$< 0.01 X_0$
Endcap ToF (Tracker)	<25 ps	$(30-50 \ \mu m \text{ for Tracker})$	e-direction $< 0.05X_0$
			h-direction $< 0.15X_0$
Roman Pots	<50 ps	$< 500/\sqrt{12} \ \mu m$	N/A
B0	<50 ps	$O(50) \mu m$	$< 0.01 X_0$

6/8/22

Nicolo Cartiglia

Comparison WF2 Simulation - Data Band bars show variation with temperature (T = -20C - 20C), and gain (G = 20 - 30)





R&D Goals

- 15-20 ps timing resolution, O(3-50 μm) position resolution where needed
- Minimal readout channel density (long strip, rectangular pixel) for reduced power, material and cost

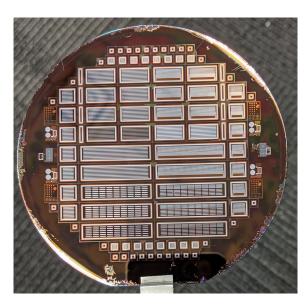
Plan

- Produce and test sensors with thinner active volume to achieve the desired timing resolution
- Optimize implantation parameters and AC-pad segmentation through simulation and real device studies
- Engage commercial vendors to improve fabrication process and yield

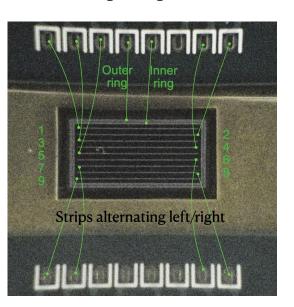
eRD112: AC-LGAD Sensor R&D

• FY22:

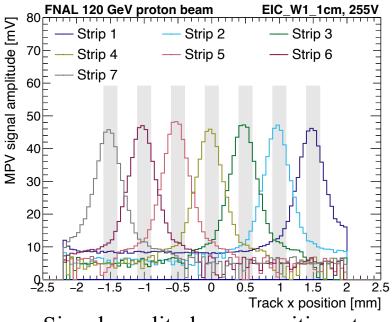
- Production of thin (20 and 30 um) sensors for ToF application with time resolution ~20 ps by BNL IO.
- Production of medium/large-area sensors with different doping concentration, pitch, and gap sizes between electrodes to optimize performance by BNL IO and HPK.
- FY23 Q3: Design and submission for fabrication of advanced sensor prototypes with <20 ps time resolution and space resolution that matches RPs, ToF, and Tracker requirements. This will be baseline for CD2/3A.
- **FY24 Q2**: Sensor batch submission with optimized sensor layouts and performance, based on laboratory and test-beam results. This sensor design will be used as baseline for the CD3 review.
- FY25: Module-size sensor fabrication with target time and space performance.



Strip AC-LGAD Sensor Wafer for EIC by BNL

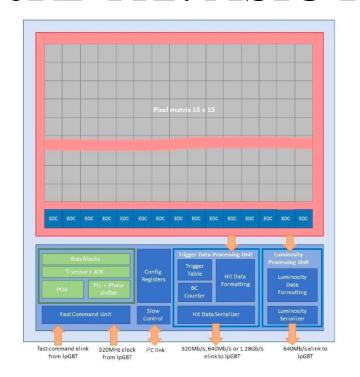


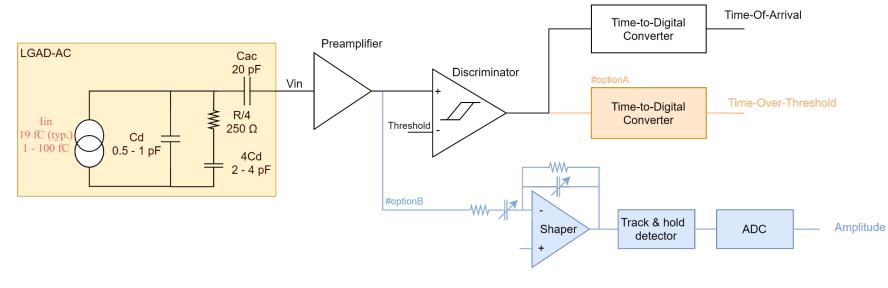
500 um*1cm strip AC-LGAD sensor mounted on test board



Signal amplitude vs x position at 2022 Fermilab test beam

eRD112: ASIC R&D





R&D Goals

• 15-20 ps jitter with minimal (1-2 mW/ch) power consumption, match AC LGAD sensors for EIC

Plan

- Continue the ASIC prototyping effort for RPs by IJCLAB/Omega (1st submission in FY22 funded externally)
- Utilize the design and experience in ASICs for fast-timing detectors from ATLAS and CMS, and investigate common ASIC design and development for RP/B0 and ToF

eRD112: ASIC R&D

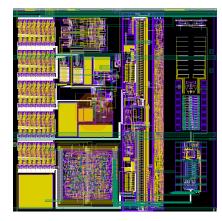
EICROC0 (submitted in 3/2022) by Omega/Irfu/AGH

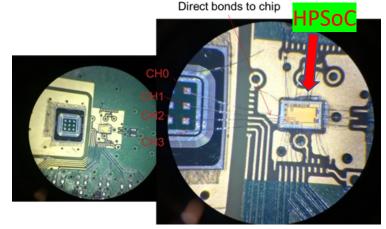
- Preamp, discri. taken from ATLAS ALTIROC
- I2C slow control taken from CMS HGCROC
- TOA TDC adapted by IRFU Saclay
- ADC adapted to 8bits by AGH Krakow
- Digital readout: FIFO depth8 (200 ns)

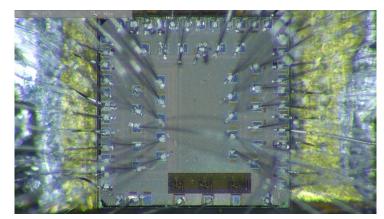
ASIC Efforts at UC Santa Cruz

- Adapt the Constant Fraction Discriminator (CFD) principle in a pixel when a CFD is paired with a TDC, one time measurement gives the final answer.
- Charge injection consistent with simulations: ~30 ps at 5fC, and <10 ps at 30 fC, with LGAD like pulses
- Tests with beta sources and beam are planned

Institution		Technology	Output	# of Chan	Funding	Specific Goals	Status
INFN Torino	FAST	110 nm CMOS	Discrim. & TDC	20	INFN	Large Capacitance TDC	Testing
NALU Scientific	HPSoC	65 nm CMOS	Waveform	5 (Prototype) > 81 (Final)	DoE SBIR	Digital back-end	Testing
Anadyne Inc	ASROC	Si-Ge BiCMOS	Discrim.	16	DoE SBIR	Low Power	Simulations, final Layout, Board design







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Summary and Outlook

- AC-LGAD is a very promising technology for 4D detectors at future high energy experiments
- In order to meet the EIC project timeline, eRD112 plan to
 - FY22
 - Finalize the requirements by EIC Detector-1 through simulation
 - Funds for AC-LGAD sensor R&D: sensor fabrication through BNL IO and HPK, build up expertise
 - Externally funded front-end ASICs: submission and testing
 - Start looking into other detector system components: mechanical, cooling, on and off-detector electronics
 - FY23
 - Continue sensor R&D, ramp up efforts on ASIC, realistic design of other detector system components
 - Come up with preliminary system designs of AC-LGAD detectors for CD2/3A review (Oct 2023)
- Please join us if you are interested
 - Indico page: https://indico.bnl.gov/category/323/
 - Mailing list: https://mailman.rice.edu/mailman/listinfo/lgads-eic
 - FY22 Proposal: https://wiki.bnl.gov/conferences/index.php/ProjectRandDFY22