Athena DAQ overview

Detector 1 DAQ WG kick-off meeting
April 26th 2022
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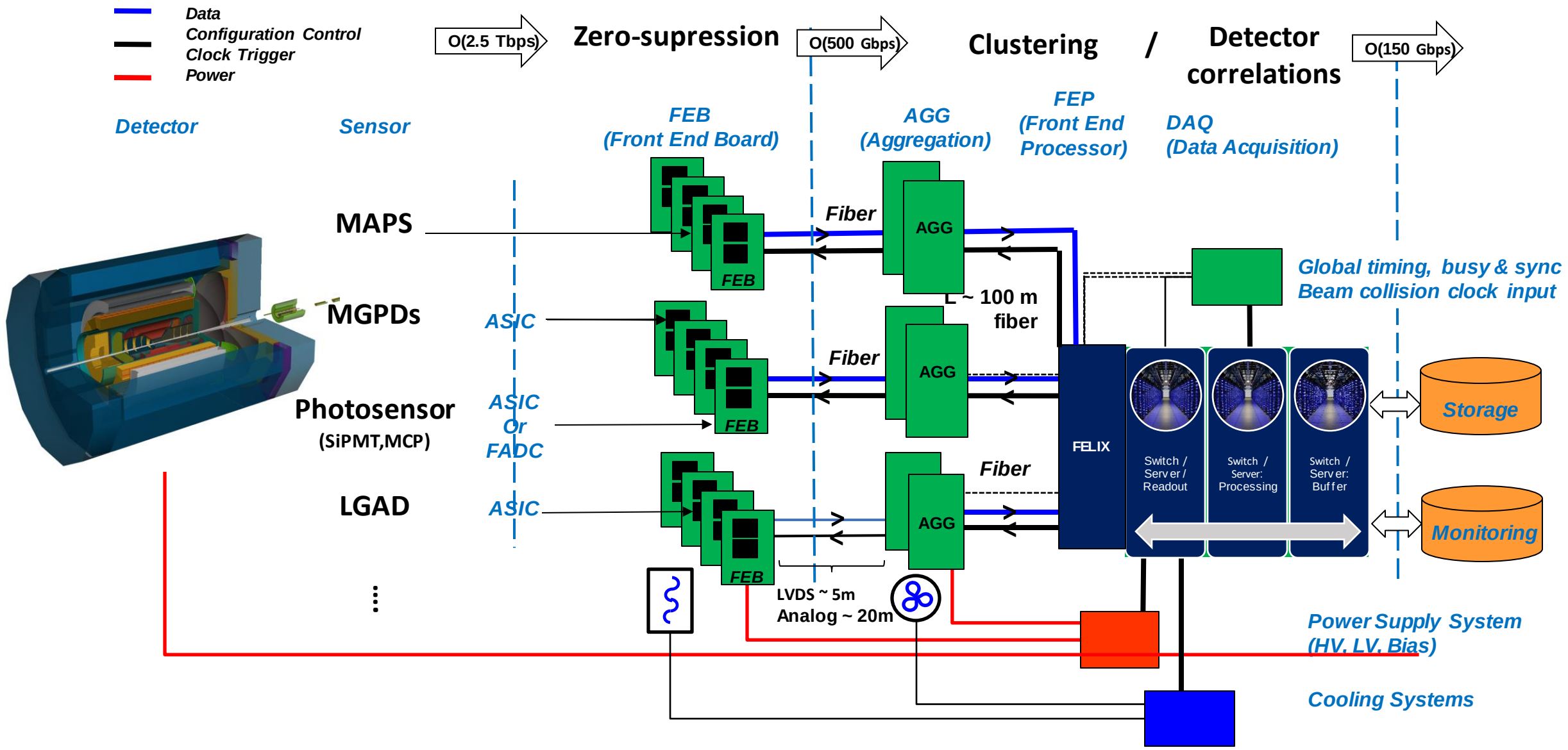
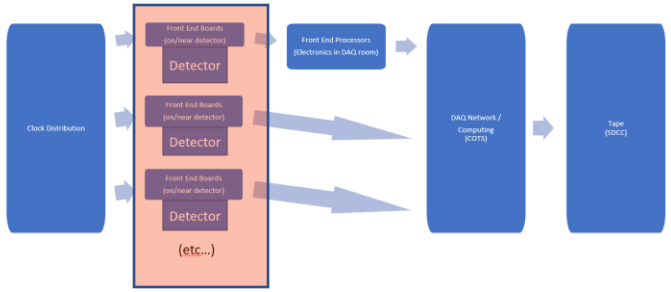
ATHENA Streaming Readout Architecture



Front End Boards (FEB)



- The collider performance:
  - ~500KHz of collisions
  - ~60-100Gbps zero suppressed data
  - ~15 KB/event
  - ~100 bytes/bunch crossing
- We have an enormous number of channels but the Silicon MAPS readouts test the relevance of the concept of channel.
- Challenging data compression scheme
  - Noise reduction
  - Zero suppression
  - Background elimination

Detector	Readout Technology	Channel Count
Silicon Tracking	Si MAPS	37B
GEM/MMG Layer	GEM	217K
Cylindrical MPGD *	GEM	60M
HP-DIRC	MAP/MT	100-330k
ECAL	SiPM	1.7K
HCAL	SiPM	24K
ECAL imaging	Si MAPS	480M
dRICH	PMT/SiPM	350K
mRICH	PMT/SiPM	330K
B0	Si MAPS	32M + 320K
Off-Momentum	AC-LGAD (eRD24)	750K
Roman Pots	AC-LGAD (eRD24)	500K
ZDC	LGAD + ASIC eRD27	225+366
TOF	AC-LGAD	15M

Electronics

Summarize in a tabular form the current state of the readout chain. Examples of development stages can include "R&D", "conceptual design", "pre-prototype","full functionality prototype", "integration tests with detector", "ready for production", etc.

Detector	Functionality	Sensor technology	FEE/ASIC	Status (det/asic)
DIRC	Position//Time (Amplitude)	MCP-PMT	HDSOC	Ready/prototype
dRICH	Time / Time over threshold/position	SiPM *	Updated ALCOR	Ready/prototype
eRICH	Time / Time over threshold/position	SiPM *	Updated ALCOR	Ready/prototype
EcalBarrelScFi	Amplitude	SiPM	Amplifier	Ready/prototype
EcalImgBarrel	Position/Time/Time over threshold	ASTROPIX (MAPS)	-	Prototype
EcalEndcapN	Amplitude	SiPM	Amplifier	Ready/prototype
EcalEndcapP	Amplitude	SiPM	Amplifier	Ready/prototype
HcalEndcapN	Amplitude	SiPM	Amplifier	Ready/prototype
HcalEndcapP	Amplitude	SiPM	Amplifier	Ready/prototype
HcalBarrel	Amplitude	SiPM	Amplifier	Ready/prototype
Inner Vertex Tracker	Position/Amplitude/Time	ALPIDE 65 nm(MAPS)	-	Prototype
MPGDTrackerBarrel	Position/Amplitude/Time	Micromegas	SALSA	Ready/conceptual*
urWELLTrackerEndcap	Position/Amplitude/Time	uRWELL	SALSA	Prototype/conceptual*
GEMTrackerEndcap	Position/Amplitude/Time	GEM	SALSA	Ready/conceptual*
B0Silicon	Position/Amplitude/Time	MAPS*	ALPIDE ITS2	Ready/ready
B0preshower	Time / Time over threshold	AC-LGAD	Updated ALTIROC	Prototype/prototype
RP	Time / Time over threshold	AC-LGAD	Updated ALTIROC	Prototype/prototype
OffM	Time / Time over threshold	AC-LGAD	Updated ALTIROC	Prototype/prototype
ffiZDCSi	Time / Time over threshold	Silicon strip detectors - DC-LGADs	Updated ALTIROC	Prototype/prototype
ffiSDCSciFi	Amplitude/Time	PMTs	Amplifier	Ready/conceptual
ZDCSiPb	Amplitude/Time	If silicon used, less if silicon fibers used.	Amplifier	Ready/conceptual
ZDCScint	Amplitude/Time	PMTs; depends on whether two sections are read-out indepdenently.	Amplifier	Ready/conceptual
TOF	Time / Time over threshold	AC-LGAD	Updated ALTIROC	Prototype/prototype
Luminosity monitoring and Low Q tagging	Amplitude/Time	6 PMT based calorimeters *	Select existing ASIC	Protype/conceptual

ASICs R&D

Provide a summary (e.g., in tabular format) of the specific R&D goals and development timescale for each individual ASIC, including each fallback option. For each ASIC, include estimate of when the decision needs to be taken whether to go with the baseline ASIC or the fallback option.

ASIC proposed	Institution(s)	R&D	Fall back option
ALCOR	INFN	Current version for low rate. Increase data throughput. Test streaming mode	(low risk)
ASTROPIX	ANL in collaboration with NASA	Customization for Imaging calorimeter, improved power and energy resolution	(low risk)
ALPIDE	EIC R&D silicon consortium in collaboration with CERN	65 nm technology ITS3, lower material budget and lower	180 nm ITS2
SALSA	CEA SACLAY in collaboration with University of Sao Paulo	Updated version of SAMPA for better performance and better support for streaming	SAMPA or VMM3
ALTIROC	CEA SACLAY/CNRS	Customization for EIC / AC LGAD Streaming	
HDSOC64	NALU	64 channels version of HDSOC	HDSOC32

Advanced prototype for TDR - start production around 2026 and ASIC choice will be frozen at that date
All ASICs are based on existing design : development of new chip mostly for improved data links for better rate capability and streaming support making the R&D fairly low risk,
SALSA is a new iteration of SAMPA with higher channel density / higher sampling rate / lower power consumption
Other ASICs will be chosen in conjunction with project from available ASICs for better standardization

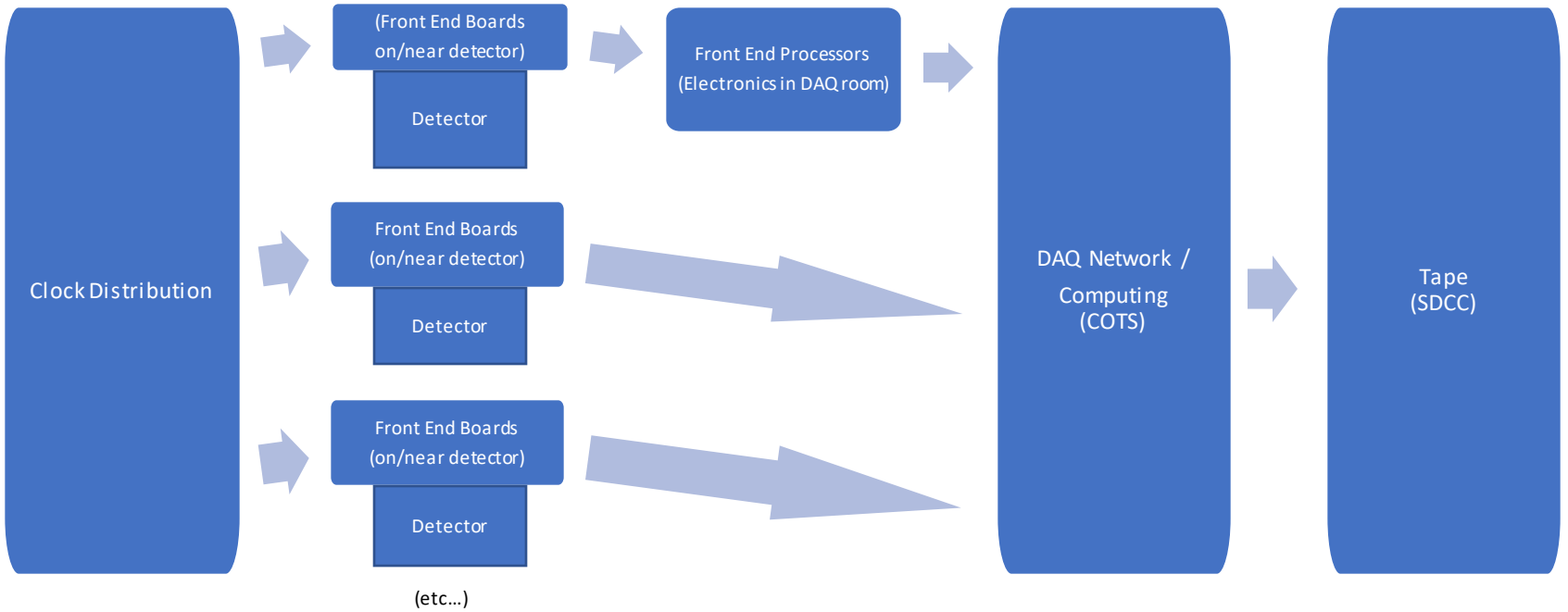
ASICs timeline

Describe the development plan and timeline for the customization and prototyping of electronics specific to each sub-detector concept.

Detector type	ASIC proposed	R&D	Conceptual design	Preprototype	Full functional prototype	Integration with readout chain and detector	Ready for production	Fall back
MCP PMT	HDSOC 64 channels	done	done	done	2022	2023		HDSOC32
SiPMT	ALCOR	done	done	2022	2023-24	2025		
Pixel detector Imaging calorimeter	ASTROPIX	2015	2018/19	March 2020	2021	2022	2023	
MAPS	ALPIDE ITS3	done	2019	2021	2023	2024	2025	ALPIDE ITS2
MPGD	SALSA	2021	2022	2023	2025			SAMPA or VMM3
AC-LGAD	ALTIROC	done	done	2022	2026	2027	2028	

Rough timeline : final details need to be worked out with different groups after detector selection

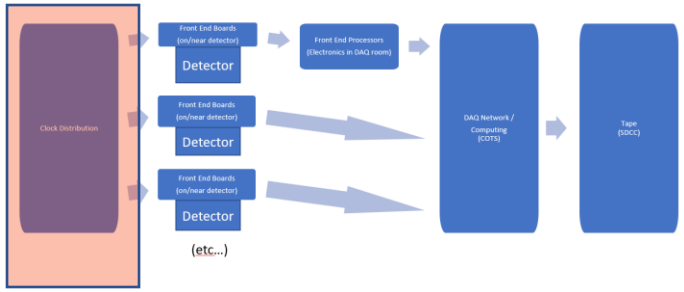
Athena DAQ Overview



We envision a triggerless streaming DAQ system following the outline described in the Yellow Report

- Gets rid of many latency constraints
- Gets of the need for a hardware trigger
- Amplifies the need for robust zero-suppression / data compression

Clock Distribution:



Function:

- Distribute a synchronized clock,
- Synchronize detector timing with bunch structure,
- Tag data with BX to synchronize detector data
- share other information between detectors
  - bunch polarization
  - “prescaling”

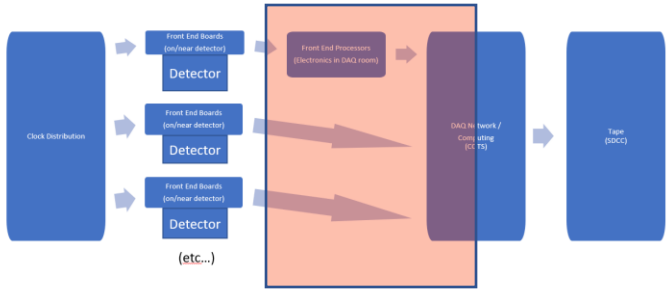
Promising Technology:

- lpGBT ecosystem

Attainable specs:

- 100Mhz clock rate (variable within reasonable parameters due to beam energy)
- ~5ps clock jitter
- 20gps transfer speeds

Front End Processors (FEP):



Consist of:

- FELIX boards
- Crates with FPGA based boards (ATCA, open VPX)

Function:

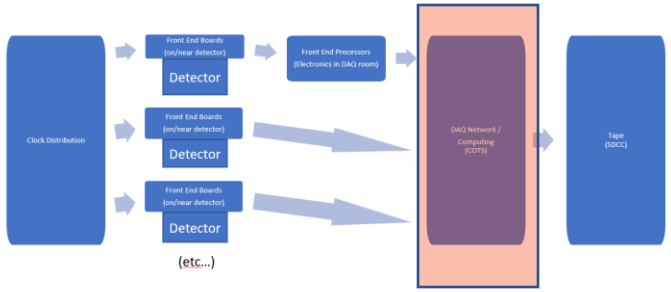
- Aggregation of links from the FEBs
- Data Compression
- High level trigger processing
  - Event identification
  - Pattern recognition
  - Tracking

In general the FPGA processing has tradeoffs

- Pro: Low latency, deterministic timing, well suited to Neural Nets / ML Algorithms
- Con: Harder to program and adapt than CPUs, quickly become obsolete
- Some of the disadvantages are mitigated by solutions such as the FELIX boards

The details of the aggregation, and the need for data compression in specific parts of the system will define the needs of the front-end processors of the system

DAQ Network and Computing:

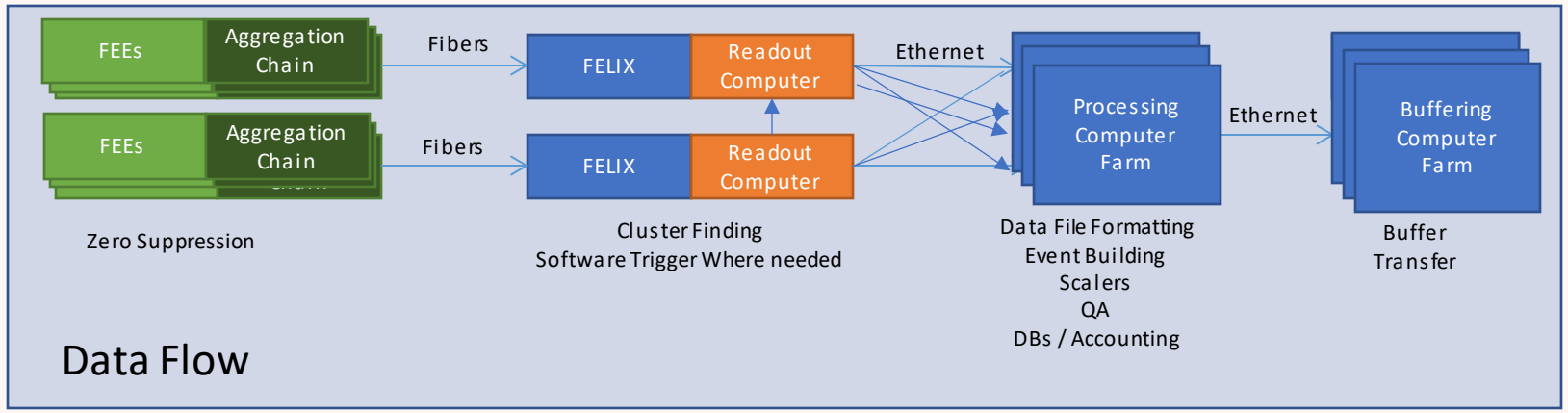


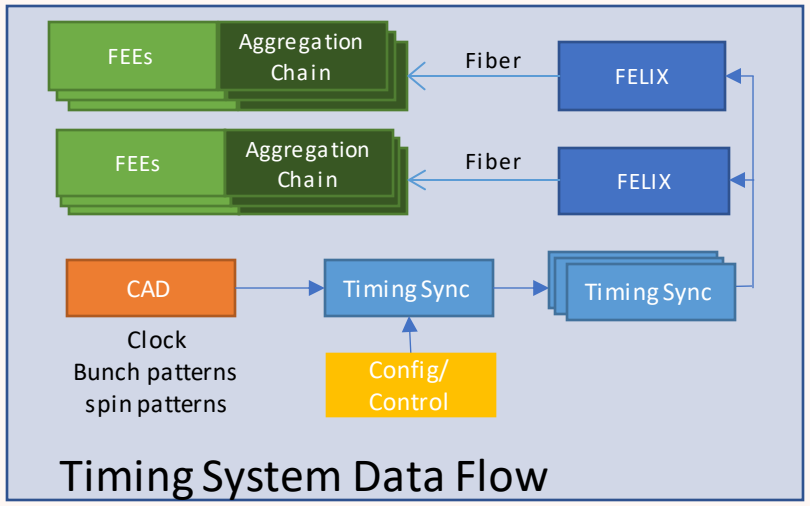
- Commercial Off-the-shelf hardware / networks
  - The problem of data transport is easily manageable with a small farm
    - Many experiments CERN experiments, sPHENIX have higher rates

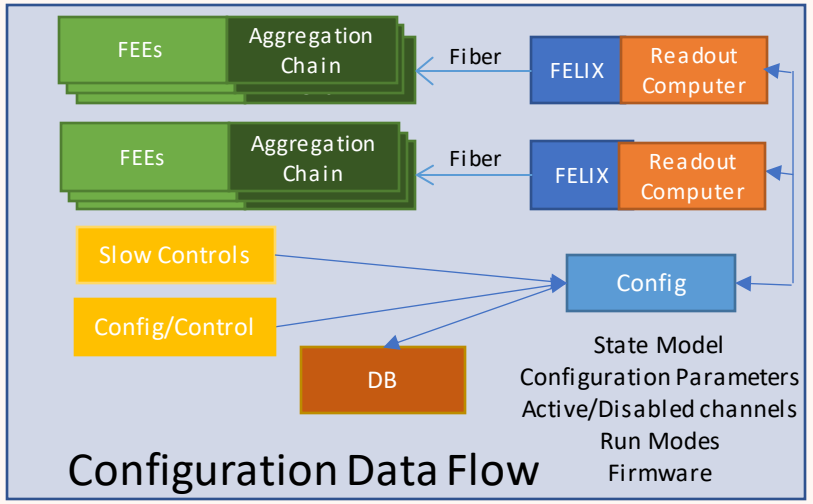
- Event identification is not built into the hardware architecture of the streaming readout so new schemes will need to be built for:
  - Event identification, tracking, and accounting
  - Scalers
  - Data formatting and event building
  - High level triggering
    - Background reduction
    - Event tagging
  - Online QA

- System control and configuration

Summary of the Athena Streaming Readout Concept:







Characteristics of Athena Streaming Model

- Very large number of channels
- Very low occupancy
- Connection limited rather than throughput limited, so extra throughput capacity in most detectors
- No trigger, but FEEs perform aggressive zero suppression
- Collision Hit + Background Hit data volumes low enough to be read out to tape

- Low Detector Noise expected (except for single photon sensitive SiPM)
- Readout time windows near single bunch crossing time expected (except for MAPS with ~200usec readout time expected)

Key points regarding Athena's proposal (Page 1)

- We de-emphasized the FEP to some degree relative to yellow report
  - The FEP was limited to
    - FELIX board FPGA
    - Relatively undefined "aggregation boards" assumed to be, effectively, FELIX boards themselves minus the CPU interface
    - The specific use-case's were:
      - Reducing data volume specifically for the dRICH and pfRICH by using ML/AI to find the rings and convert the noise-susceptible SiPM readout to particle parameters. But this faces un-investigated issues
        - Segmentation details
        - Calibration details
        - The potential for staged readout in this section (as the luminosity AND radiation damage increase over time) leading to changes in segmentation and hence firmware.
      - General "data reduction" / noise reduction for other detectors, although generally track parameters do not save much over hits, so reduction must be in the form of removing hits.

Key points regarding Athena's proposal (page 2)

- The timing system was assumed to be a relatively small tree of nodes distributing information to the FELIX boards. The timing system interface to the detectors was assumed to be part of the FEEs.
  - For DAQ costing the timing system ~$200k, ~3 years labor for ~10 boards
    - Recent discussions have demonstrated that this approach leaves out the FEE part of the timing system, which has complexity that gets imposed by DAQ that needs common FEE interface/functionality.
  - The timing system is also assumed to be feature rich
    - Potential trigger interface
    - Controllable "busy / inhibit" signal by detector
    - Interface to collider clocks (including, for example the decoding of filled bunches, spin states etc…)
  - The functions of the timing system are:
    - Synchronizing the DAQ system which implies the need for a large number of bits labelling bx times. Recall: 33 bits = 1 sec which is too short → 40 bits (3 hours), or 64 bits (5k years)
    - Detector timing (~15ps resolution)
    - Bunch crossing windows for reducing data volume(~<1ns resolution combined with detector resolution)
  - The timing system is also "early" in the schedule. It must be defined before the FEE designs are finalized because it's features need to be supported by the all detectors

Key points regarding Athena's proposal (page 3)

- Configuration Subsystem
  - Standard configuration of the system
    - ASIC parameters
    - Special run types
    - "Triggers" are specified both as a fallback option in Athena, and also at the software level as a
    - Complex, but standard…
  - Data volumes are small, but number of channels are high
    - Absurd but illustrative calculation: BX frequency is .1 GHz, so a single 64 bit channel floating high could contribute 6.4Gbps, ~5% of the assumed data volume of the entire system
    - There need to be safeguards built into the components at each level of the DAQ that:
      - Ensure that a given component can't exceed the data volume it is allowed to send out
      - Ensure that if a source component IS exceeding it's allowed data rate it can be turned off
      - Ensure that these two features can be controlled and monitored dynamically by the full system

Key points regarding Athena's proposal (page 4)

- The dRICH in Athena
  - ~300k SiPM based channels (Another 225k channels in pfRICH)
  - Radiation dependent dark currents in the SiPM lead to high dark currents, indistinguishable from the single photon sensing required by the detectors
  - Data Volumes
    - Absolutely raw dark currents between: .2 – 18 Mbps per channel
    - Maximum absolute raw rate to dRICH: 5400 Gbps (4050 Gbps)
    - After application of time window on bunch crossings: 1800Gbps (1350 Gbps)
  - Athena approach was:
    - FEEs must apply the time window reduction
    - DAQ must provide sufficient bandwidth capability to read the data into the DAQ
    - DAQ must be able to produce a collision trigger (using calorimeters, presumably) and remove hits not associated with a collisions
    - ML/AI approach directly on the RICH data in FEP was mentioned as R&D, but not guaranteed.
  - Note, that the same dynamic is at play for the far backward detectors. They produce a low volume of histogrammed data, but also a total zs data volume that could approach 50-100Gbps due to high bremsstrahlung rate and would be reduced in the same fashion.

Key points regarding Athena's proposal (page 5)

- The offline analysis and data format questions (such as event building) were not fully defined, however, the key points we specified regarding offline interface were:
  - Calibration:
    - We did not envision doing full "offline calibration" within the DAQ
    - We did explicitly differentiate between full calibrations, and the standard gain/slewing/timing/threshold setting calibrations needed by DAQ to take valid data, and explicitly mentioned that we would support the rapid evaluation of these.
  - Online analysis
    - We rejected performing true physics analysis online (final form tracking for example)
      - The need is not there because zero-suppression / combined with special handling for RICH/far backward detectors would be sufficient to write out all collision data
      - Full detector calibrations in real time, along with full analysis code development prior to running would impose a lot of unspecified requirements on the DAQ
      - There would be potential risks associated with removal of collision data
  - We did envision the need for QA online, (or at least in real time). This QA would involve cross-detector correlation, and some level of online reconstruction and shared tools with the collaboration's software frameworks.