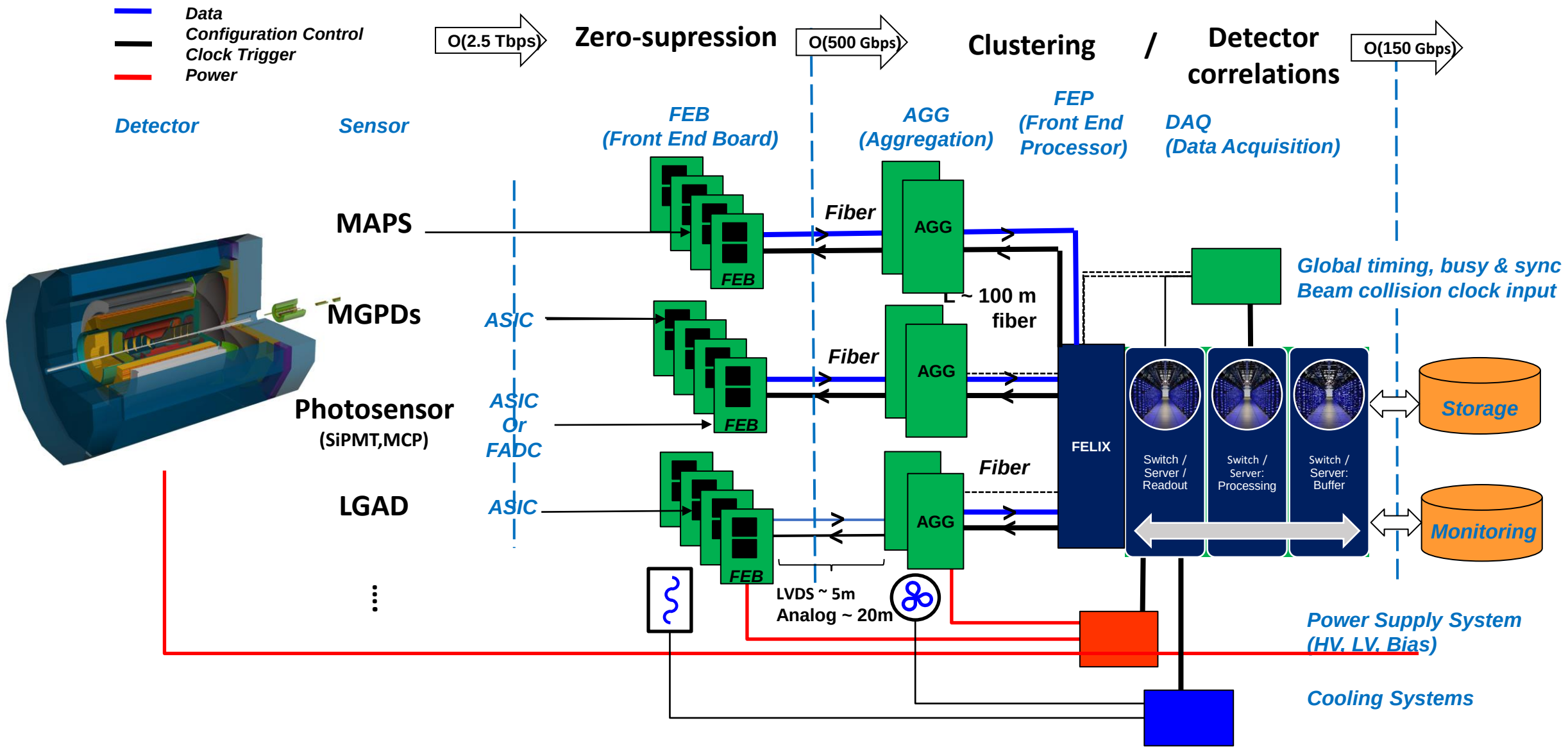
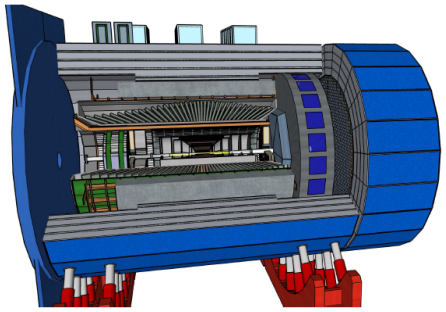
Athena / ECCE comparison
and
summary kick-off meeting

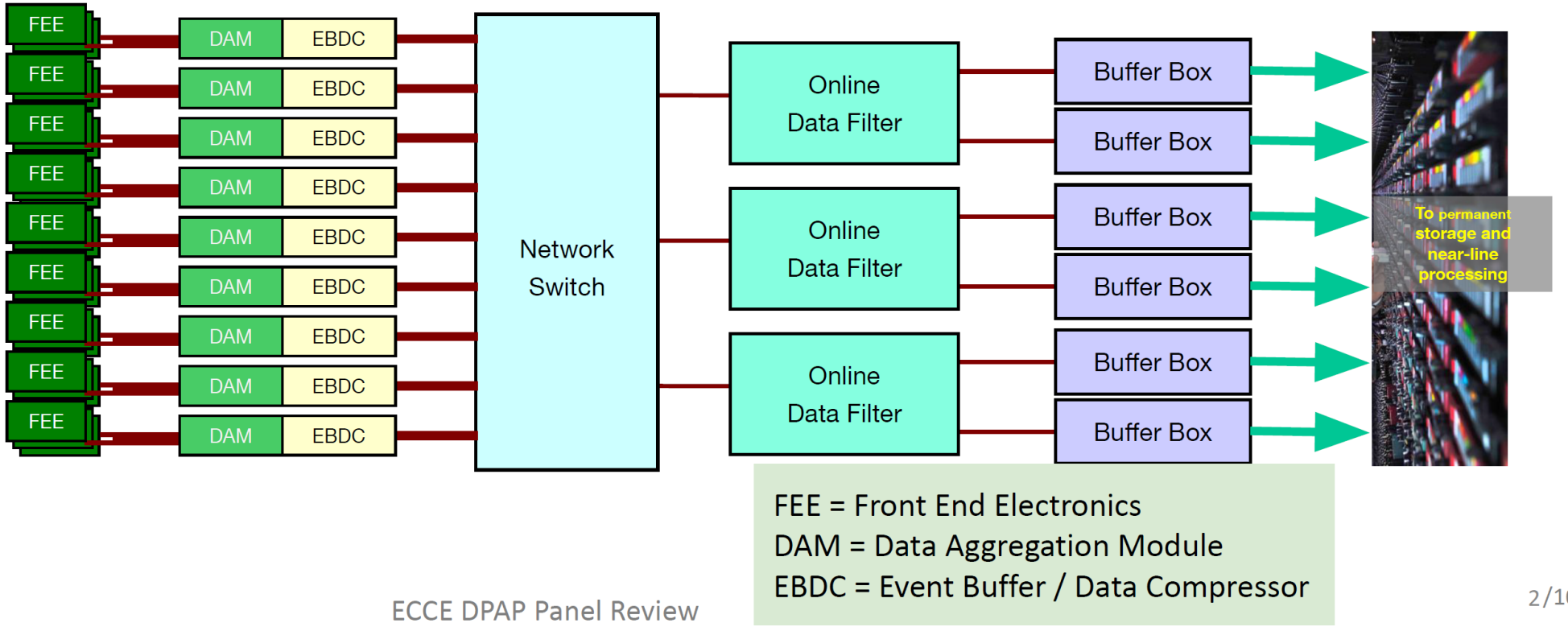
Detector 1 DAQ WG
April 28th 2022

ATHENA Streaming Readout Architecture



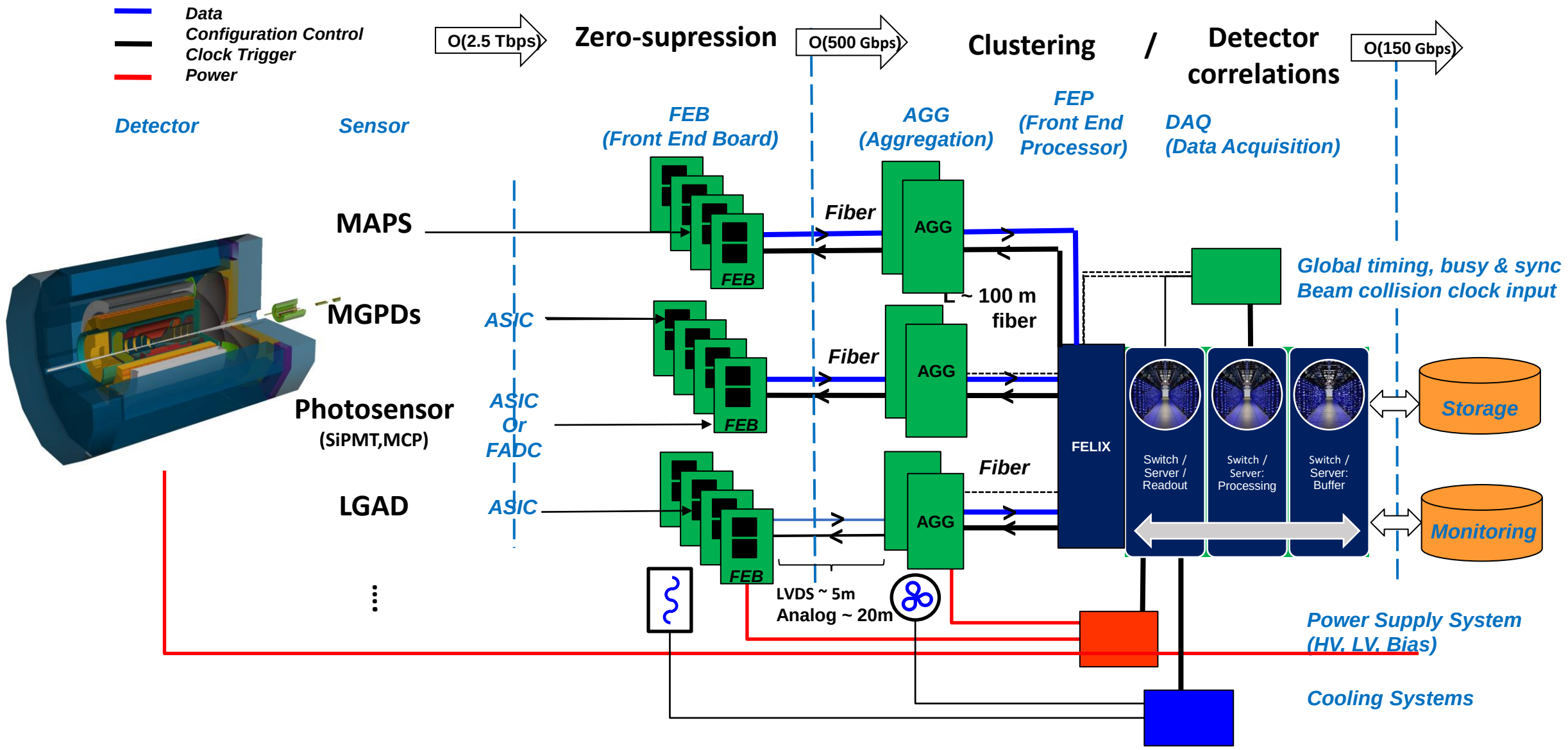
ECCE Streaming Readout Architecture



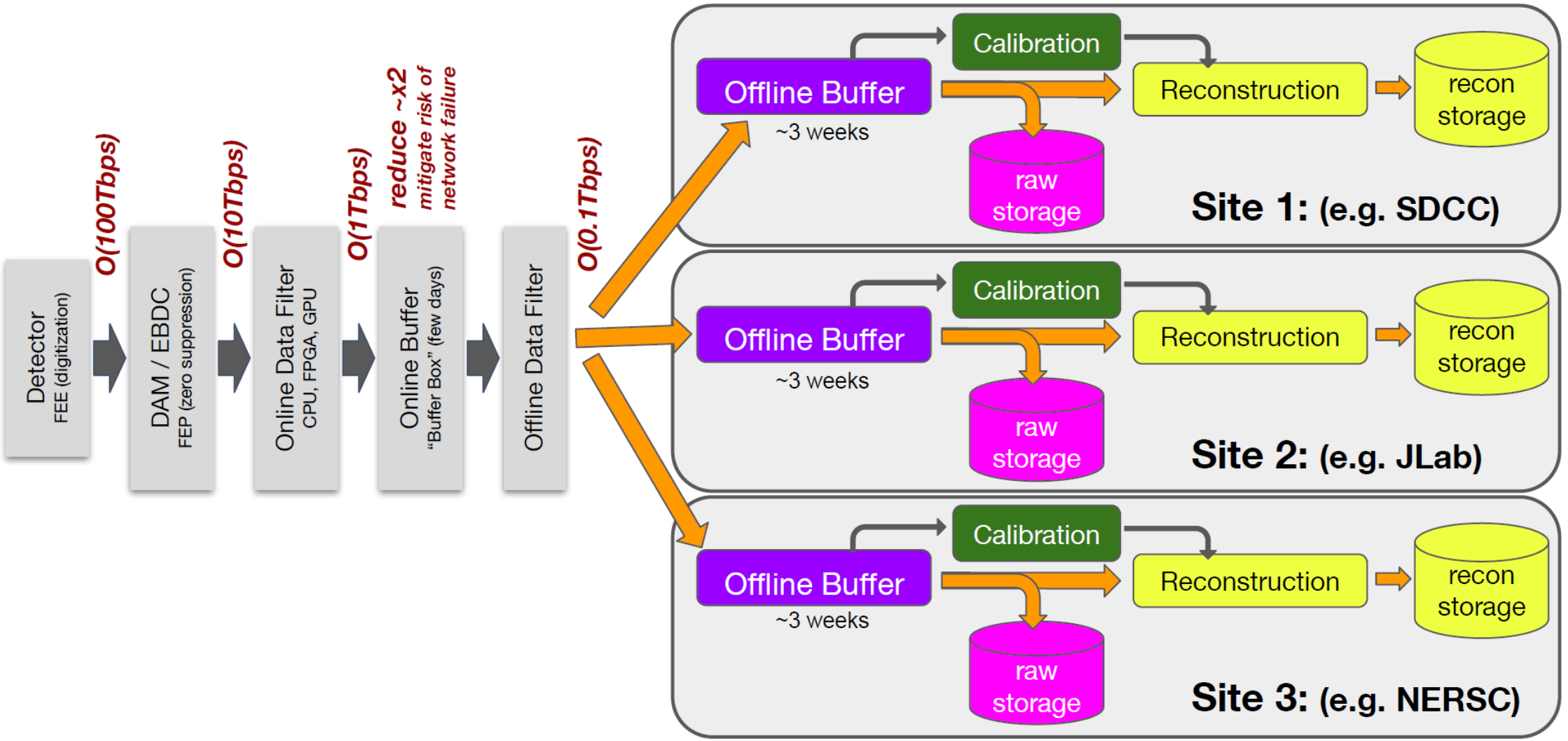


FEE = Front End Electronics
DAM = Data Aggregation Module
EBDC = Event Buffer / Data Compressor

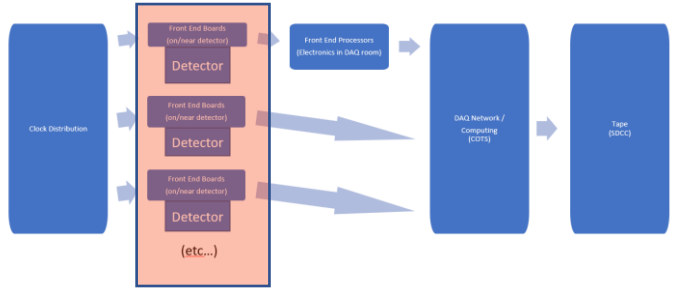
ATHENA Streaming Readout Architecture



Computing: Online to Offline Stream



Front End Boards (FEB)



- The collider performance:
  - ~500KHz of collisions
  - ~60-100Gbps zero suppressed data
  - ~15 KB/event
  - ~100 bytes/bunch crossing

- We have an enormous number of channels but the Silicon MAPS readouts test the relevance of the concept of channel.

- Challenging data compression scheme
  - Noise reduction
  - Zero suppression
  - Background elimination

Detector	Readout Technology	Channel Count
Silicon Tracking	Si MAPS	37B
GEM/MMG Layer	GEM	217K
Cylindrical MPGD *	GEM	60M
HP-DIRC	MAP/MT	100-330k
ECAL	SiPM	1.7K
HCAL	SiPM	24K
ECAL imaging	Si MAPS	480M
dRICH	PMT/SiPM	350K
mRICH	PMT/SiPM	330K
B0	Si MAPS	32M + 320K
Off-Momentum	AC-LGAD (eRD24)	750K
Roman Pots	AC-LGAD (eRD24)	500K
ZDC	LGAD + ASIC eRD27	225+366
TOF	AC-LGAD	15M

Side by side ATHENA/ECCE

ATHENA

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ECCE

PID WBS Name	Detector	ASIC	Channels
Barrel PID	hpDIRC	High Density SoC	69,632
	TOF	eRD112 development	8,600,000
Electron Endcap	mRICH	High Density SoC	65,536
	TOF	eRD112 development	920,000
Hadron Endcap	dRICH	MAROC3	5,376
	TOF	eRD112 development	1,840,000
Far-Forward Detectors	Roman Pots	eRD112 development	524,288
	B0 Detector	eRD112 development	2.6M
	Off-Momentum Detectors	eRD112 development	1.8M
Far-Backward Detectors	Low-Q^2 Tagger	eRD112 development	4.6M
	Luminosity Monitor	eRD112 development	268,441

Electronics

Summarize in a tabular form the current state of the readout chain. Examples of development stages can include "R&D", "conceptual design", "pre-prototype","full functionality prototype", "integration tests with detector", "ready for production", etc.

Detector	Functionality	Sensor technology	FEE/ASIC	Status (det/asic)
DIRC	Position//Time (Amplitude)	MCP-PMT	HDSOC	Ready/prototype
dRICH	Time / Time over threshold/position	SiPM *	Updated ALCOR	Ready/prototype
eRICH	Time / Time over threshold/position	SiPM *	Updated ALCOR	Ready/prototype
EcalBarrelScFi	Amplitude	SiPM	Amplifier	Ready/prototype
EcalImgBarrel	Position/Time/Time over threshold	ASTROPIX (MAPS)	-	Prototype
EcalEndcapN	Amplitude	SiPM	Amplifier	Ready/prototype
EcalEndcapP	Amplitude	SiPM	Amplifier	Ready/prototype
HcalEndcapN	Amplitude	SiPM	Amplifier	Ready/prototype
HcalEndcapP	Amplitude	SiPM	Amplifier	Ready/prototype
HcalBarrel	Amplitude	SiPM	Amplifier	Ready/prototype
Inner Vertex Tracker	Position/Amplitude/Time	ALPIDE 65 nm(MAPS)	-	Prototype
MPGDTrackerBarrel	Position/Amplitude/Time	Micromegas	SALSA	Ready/conceptual*
urWELLTrackerEndcap	Position/Amplitude/Time	uRWELL	SALSA	Prototype/conceptual*
GEMTrackerEndcap	Position/Amplitude/Time	GEM	SALSA	Ready/conceptual*
B0Silicon	Position/Amplitude/Time	MAPS*	ALPIDE ITS2	Ready/ready
B0preshower	Time / Time over threshold	AC-LGAD	Updated ALTIROC	Prototype/prototype
RP	Time / Time over threshold	AC-LGAD	Updated ALTIROC	Prototype/prototype
OffM	Time / Time over threshold	AC-LGAD	Updated ALTIROC	Prototype/prototype
ffiZDCSi	Time / Time over threshold	Silicon strip detectors - DC-LGADs	Updated ALTIROC	Prototype/prototype
ffiSDCSciFi	Amplitude/Time	PMTs	Amplifier	Ready/conceptual
ZDCSiPb	Amplitude/Time	If silicon used, less if silicon fibers used.	Amplifier	Ready/conceptual
ZDCScint	Amplitude/Time	PMTs; depends on whether two sections are read-out independently.	Amplifier	Ready/conceptual
TOF	Time / Time over threshold	AC-LGAD	Updated ALTIROC	Prototype/prototype
Luminosity monitoring and Low Q tagging	Amplitude/Time	6 PMT based calorimeters *	Select existing ASIC	Protype/conceptual

ASICs R&D

Provide a summary (e.g., in tabular format) of the specific R&D goals and development timescale for each individual ASIC, including each fallback option. For each ASIC, include estimate of when the decision needs to be taken whether to go with the baseline ASIC or the fallback option.

ASIC proposed	Institution(s)	R&D	Fall back option
ALCOR	INFN	Current version for low rate. Increase data throughput. Test streaming mode	(low risk)
ASTROPIX	ANL in collaboration with NASA	Customization for Imaging calorimeter, improved power and energy resolution	(low risk)
ALPIDE	EIC R&D silicon consortium in collaboration with CERN	65 nm technology ITS3, lower material budget and lower	180 nm ITS2
SALSA	CEA SACLAY in collaboration with University of Sao Paulo	Updated version of SAMPA for better performance and better support for streaming	SAMPA or VMM3
ALTIROC	CEA SACLAY/CNRS	Customization for EIC / AC LGAD Streaming	
HDSOC64	NALU	64 channels version of HDSOC	HDSOC32

Advanced prototype for TDR - start production around 2026 and ASIC choice will be frozen at that date
All ASICs are based on existing design : development of new chip mostly for improved data links for better rate capability and streaming support making the R&D fairly low risk,
SALSA is a new iteration of SAMPA with higher channel density / higher sampling rate / lower power consumption
Other ASICs will be chosen in conjunction with project from available ASICs for better standardization

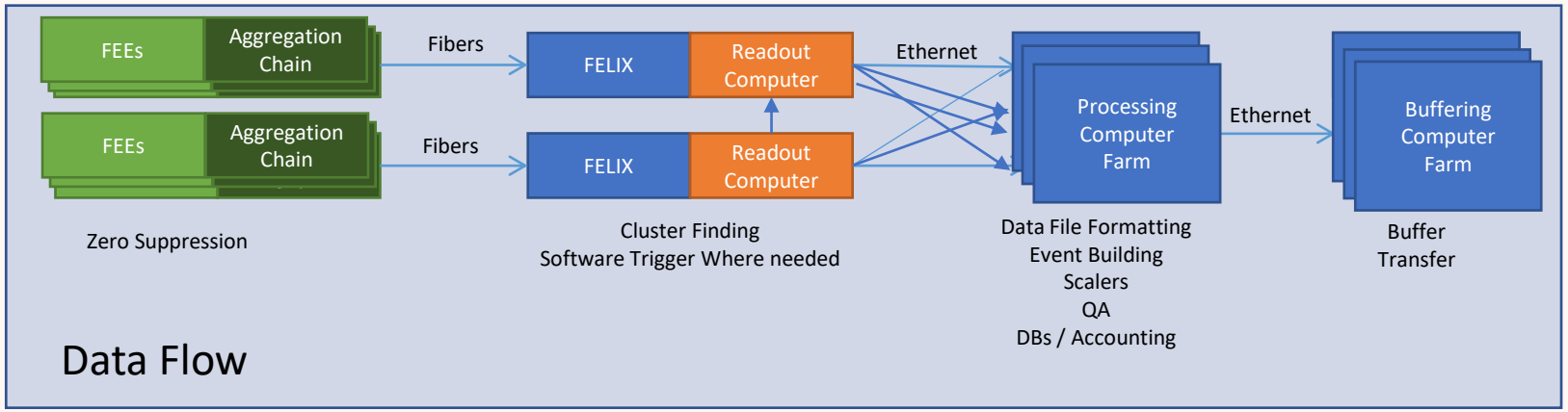
ASICs timeline

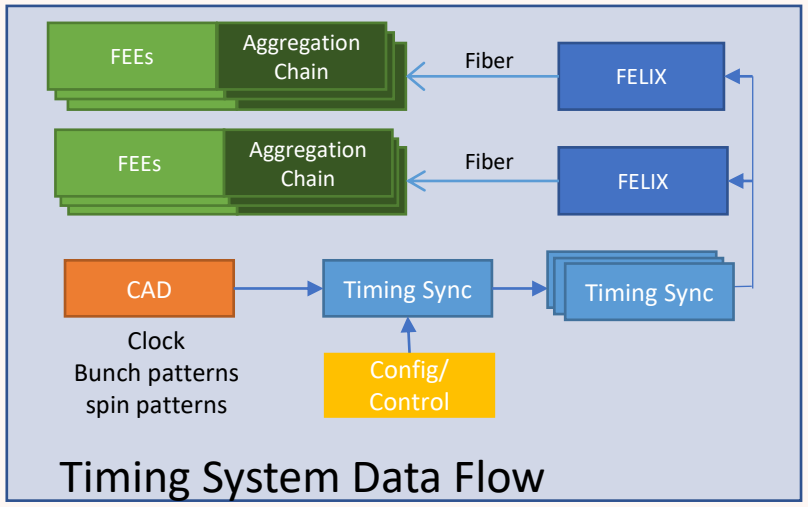
Describe the development plan and timeline for the customization and prototyping of electronics specific to each sub-detector concept.

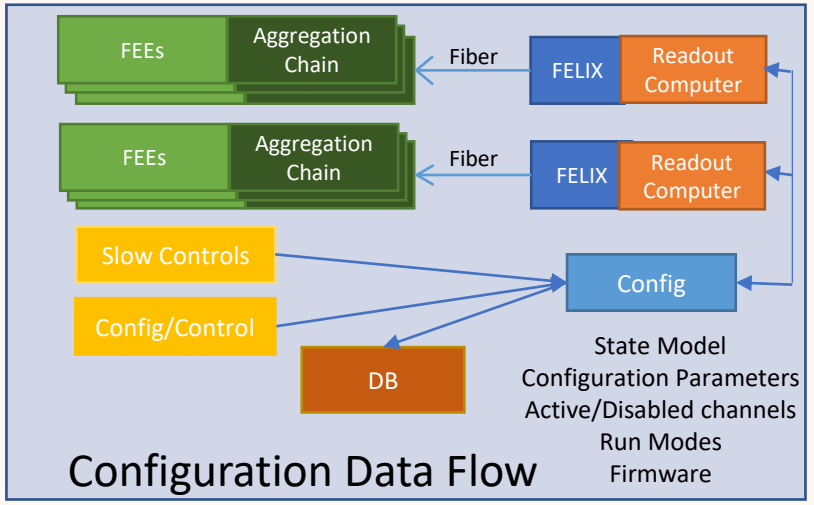
Detector type	ASIC proposed	R&D	Conceptual design	Preprototype	Full functional prototype	Integration with readout chain and detector	Ready for production	Fall back
MCP PMT	HDSOC 64 channels	done	done	done	2022	2023		HDSOC32
SiPMT	ALCOR	done	done	2022	2023-24	2025		
Pixel detector Imaging calorimeter	ASTROPIX	2015	2018/19	March 2020	2021	2022	2023	
MAPS	ALPIDE ITS3	done	2019	2021	2023	2024	2025	ALPIDE ITS2
MPGD	SALSA	2021	2022	2023	2025			SAMPA or VMM3
AC-LGAD	ALTIROC	done	done	2022	2026	2027	2028	

Rough timeline : final details need to be worked out with different groups after detector selection

Summary of the Athena Streaming Readout Concept:







Characteristics of Athena Streaming Model

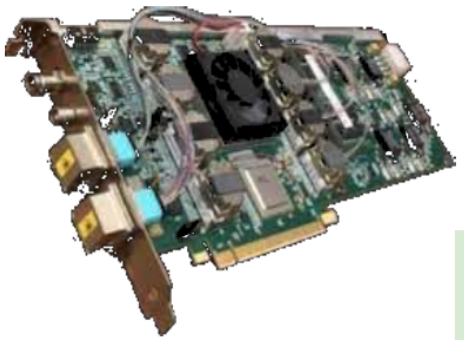
- Very large number of channels
- Very low occupancy
- Connection limited rather than throughput limited, so extra throughput capacity in most detectors
- No trigger, but FEEs perform aggressive zero suppression
- Collision Hit + Background Hit data volumes low enough to be read out to tape

- Low Detector Noise expected (except for single photon sensitive SiPM)
- Readout time windows near single bunch crossing time expected (except for MAPS with ~200usec readout time expected)

Detector system	DAM boards	Channel/Fiber Count
Barrel		
Si Tracker	4	100 fibers
uRWell	12	278,000 channels, 576 fibers
AC-LGAD TOF	30	1400 fibers
hpDIRC	5	200 fibers
BECAL	2	9,088 channels , 72 fibers
iHCAL + oHCAL	1	3,264 channels, 26 fibers
Forward		
AC-LGAD TOF	6	300 fibers
dRICH	5	220 fibers
FEMC	8	47,850 channels, 375 fibers
LFHCAL	10	58,590 channels, 460 fibers
Backwards		
mRICH	7	288 fibers
AC-LGAD TOF	3	150 fibers
EEMC	1	2878 channels, 24 fibers
Far-Forward		
B0 Detector, Roman Pots, Off-Momentum Detectors, ZDC	26	7.4M
Far-Backward		
Luminosity Monitor & Low-Q^2 Tagger	18	4.9M
Sum	**138**	

DAM Boards

- Transition data to COTS Computing
- Built-in FPGA provides processing/Data aggregation



ATLAS FELIX board is an example of a DAM board

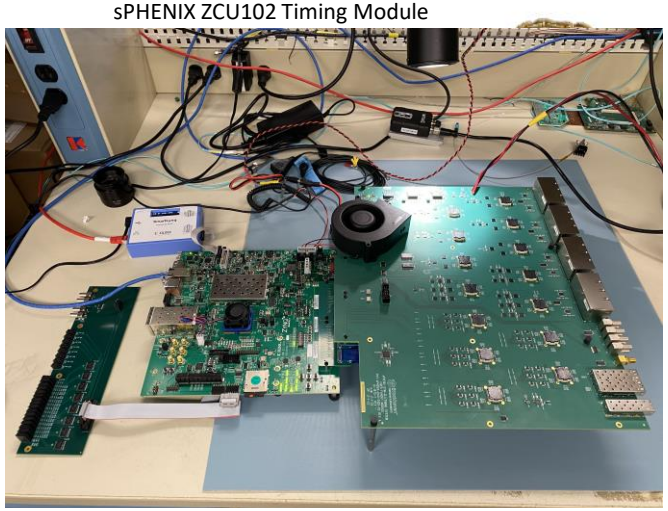
COTS = Commercial Off The Shelf
DAM = Data Aggregation Module

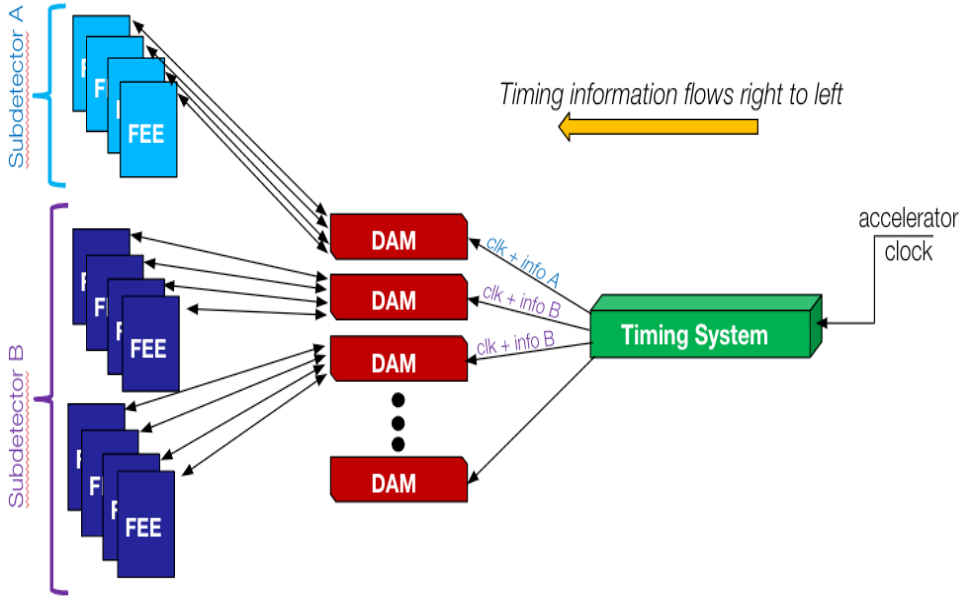
DAQ: Timing System

- Each beam crossing identified with unique 64-bit value
- Communicated to DAM boards which distribute to FEE
  - Data transferred at multiple of accelerator clock (e.g. x6)
    - 16bits per transfer *(16x6 = 96bits/crossing)*
  - Additional data embedded across transfers
    - "mode" bits can indicate different actions to FEE
  - Crossing number used to stamp all data from front end
    - Specifics of timing will be detector dependent
  - System modeled after working sPHENIX system

FEE = Front End Electronics
DAM = Data Aggregation Module

sPHENIX ZCU102 Timing Module





Raw Data Requirements *(estimated)*

ECCE Runs	year-1	year-2	year-3
Luminosity	$10^{33}\text{cm}^{-2}\text{s}^{-1}$	$2 \times 10^{33}\text{cm}^{-2}\text{s}^{-1}$	$10^{34}\text{cm}^{-2}\text{s}^{-1}$
Weeks of Running	10	20	30
Operational efficiency	40%	50%	60%
Disk (temporary)	1.2PB	3.0PB	18.1PB
Disk (permanent)	0.4PB	2.4PB	20.6PB
Data Rate to Storage	6.7Gbps	16.7Gbps	100Gbps
Raw Data Storage (no duplicates)	4PB	20PB	181PB
Recon process time/core	5.4s/ev	5.4s/ev	5.4s/ev
Streaming-unpacked event size	33kB	33kB	33kB
Number of events produced	121 billion	605 billion	5,443 billion
Recon Storage	0.4PB	2PB	18PB
CPU-core hours (recon+calib)	191Mcore-hrs	953Mcore-hrs	8,573Mcore-hrs
2020-cores needed to process in 30 weeks	38k	189k	1,701k

Few items from kick-off meeting

- DAQ design pretty close to each other
- Not clear can use MCP-PMT or LAPPD for RICHes, if use SiPMT issue of dark-noise remain
- Timing / clock distribution : lpGBT vs separate like sPHENIX or JLAB
  - Less / no radiation hardness required : can save cost and overhead of lpGBT
  - lpGBT sastifies requirements (if works at required clock frequency)
  - Maybe hybrid, with lpGBT for TOF only
- Would like to add to all other detector WG charge
  - Have on detector WG Point of Contact to set up dialog which each individual detector to define protocols and requirements of readout
  - Estimate data rates from detector subsystems from physics, physics background, noise and dark noise, define zero suppression strategy
- Early specification of protocols and standards is beneficial
- Stay open to other solutions (custom or commercial) which could offer better performance for similar cost without increasing risk
  (example FELIX, FERS, ARISTA FPGA for aggregation module)