

eRD104: “Readout Services Reduction” Updates

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ORNL is managed by UT-Battelle, LLC for the US Department of Energy

eRD104 Overall Plan

Services Reduction intent is to investigate methods to significantly reduce the services load for an EIC MAPS based tracking detector. This can be broken down into the largest components:

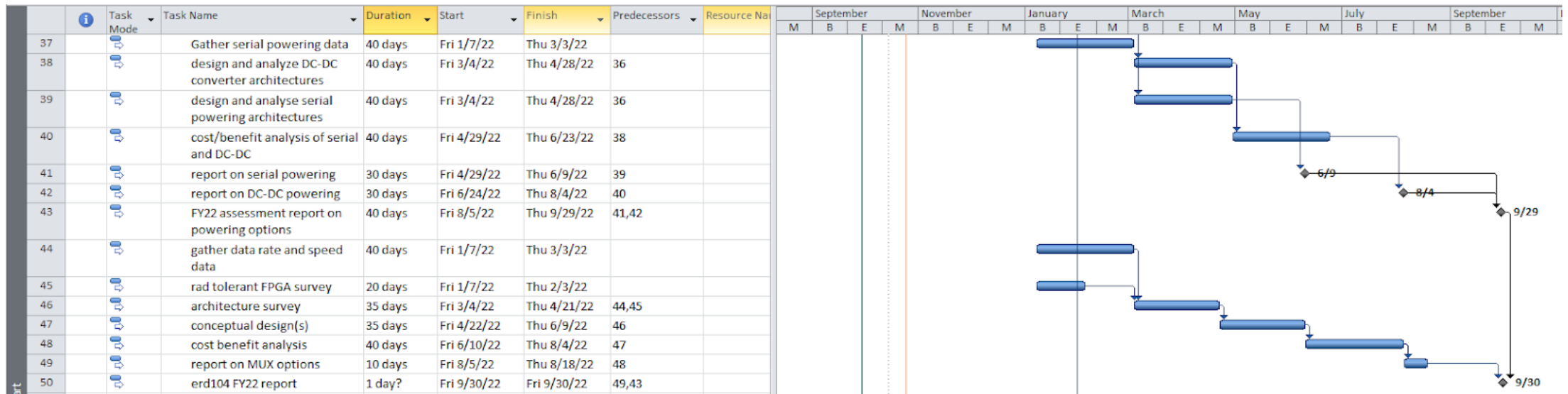
Powering (Birmingham, RAL)

- Investigate the use of DC-DC converter-based architectures to significantly reduce the number of wires needed to power the detector. This will require that we introduce radiation tolerant DC-DC converters into the detector structure in proximity to the disc/stave connection points.
- Investigate the use of serial powering architectures with the same effect. This will require that we introduce regulation at the (stitched) sensor level either on die or as a hybrid arrangement.
- Assess detector design goals and apply the best overall optimization of available technologies studied under R&D to the final implementation of the detector (tracking and others who are interested in working on this)

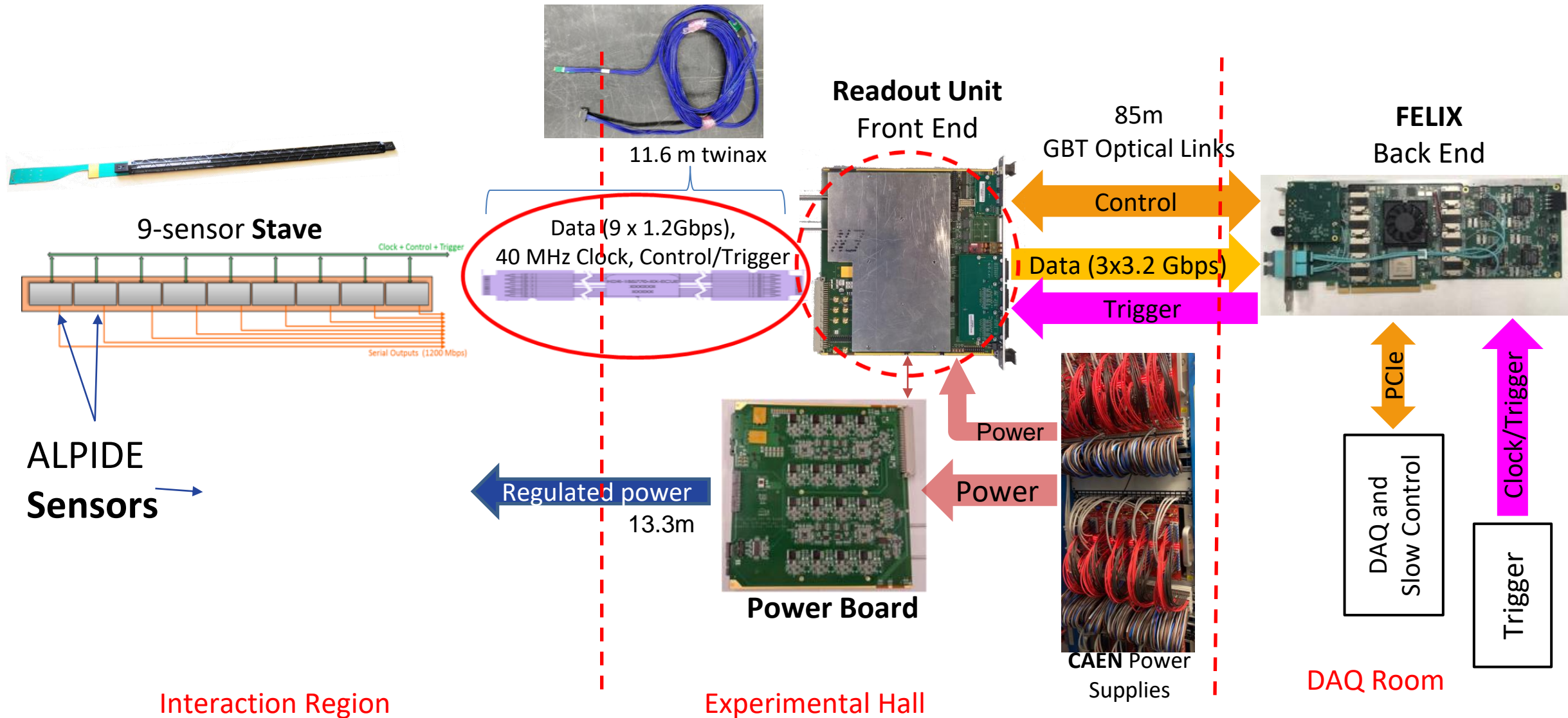
Data (ORNL, BNL)

- Investigate the use of data aggregation on detector using radiation tolerant FPGAs to receive multiple data streams from sensor blocks (over twinax/FPC) and multiplex and transmit the data out via high-speed fiber ribbon connections to RDO boards (or FELIX). This will require functionality in the MUX boards to steer control and configuration and additional power for the MUX boards in detector. Again, the final R&D goal is to develop an optimized viable system for minimizing the services loads due to signal transmission.

2022 Work Plan and Schedule



Starting Point: Current ALICE ITS-2 / sPHENIX MVTX



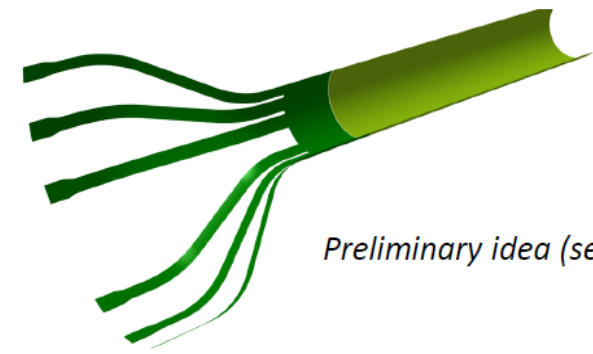
Conversation with Gianluca:

- Marcel (Utrecht) has shown experimentally that the line rate limits on the ITS2 data cables are not much above 2Gb/s. Certainly NOT possible to transmit much faster than that on those distances.
- Marcel has experimentally studied and demonstrated experimentally a solution with active re-generation of the signals by active repeaters on small break-boards at the junction off cable segments.
- Current estimates for one 'stave' of the ITS3 sensor (that is one standalone module, not one chip), is that we might have up to 8 links at 5 Gb/s.
- The inner layer chip, half cylinder, would be made with three staves on one die, that is 24 links at 5 Gb/s from the half cylinder of the innermost layer, total 120 Gb/s.
- The equivalent ITS2 innermost layer is 6 staves * 9 chips * 1.2 Gb/s = 64.8 Gb/s
- Encoding is also supposed to change, going from 8b10b to a more efficient and better performing code compatible with FPGA receivers (Marcel looked into 64b/66b I think).

FPC development has started

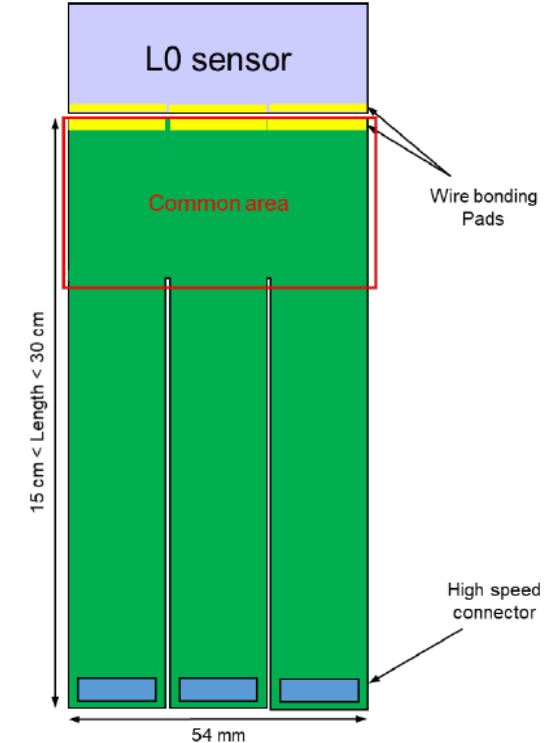
For each sensor unit of 18 mm in r-phi (3,4,5 for Half-L0,L1,L2):

- DATA: 40 Gb/s total bandwidth over 8 x 5 Gb/s transmitters
- POWER domains: analog, digital, HSdata
 - density: 40 mW/cm² over whole area + 30-50 mW per transmitter
 - backbone bus power to be evaluated; need for sense wires
- LAYOUT: Cu on A-side, Al/Cu FPC or power cables on C-side
 - investigate multi-layer solutions (bending radii, stiffness, resistances)
- SERVICE BARREL:
 - HSdata repeaters, optical links, power regulators under evaluation

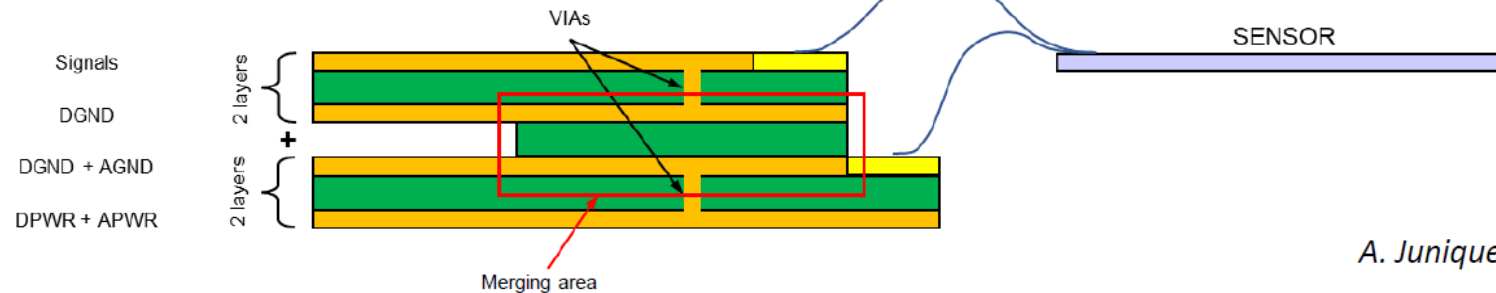


Preliminary idea (see WP5)

FPC top view: common area option (preliminary idea)

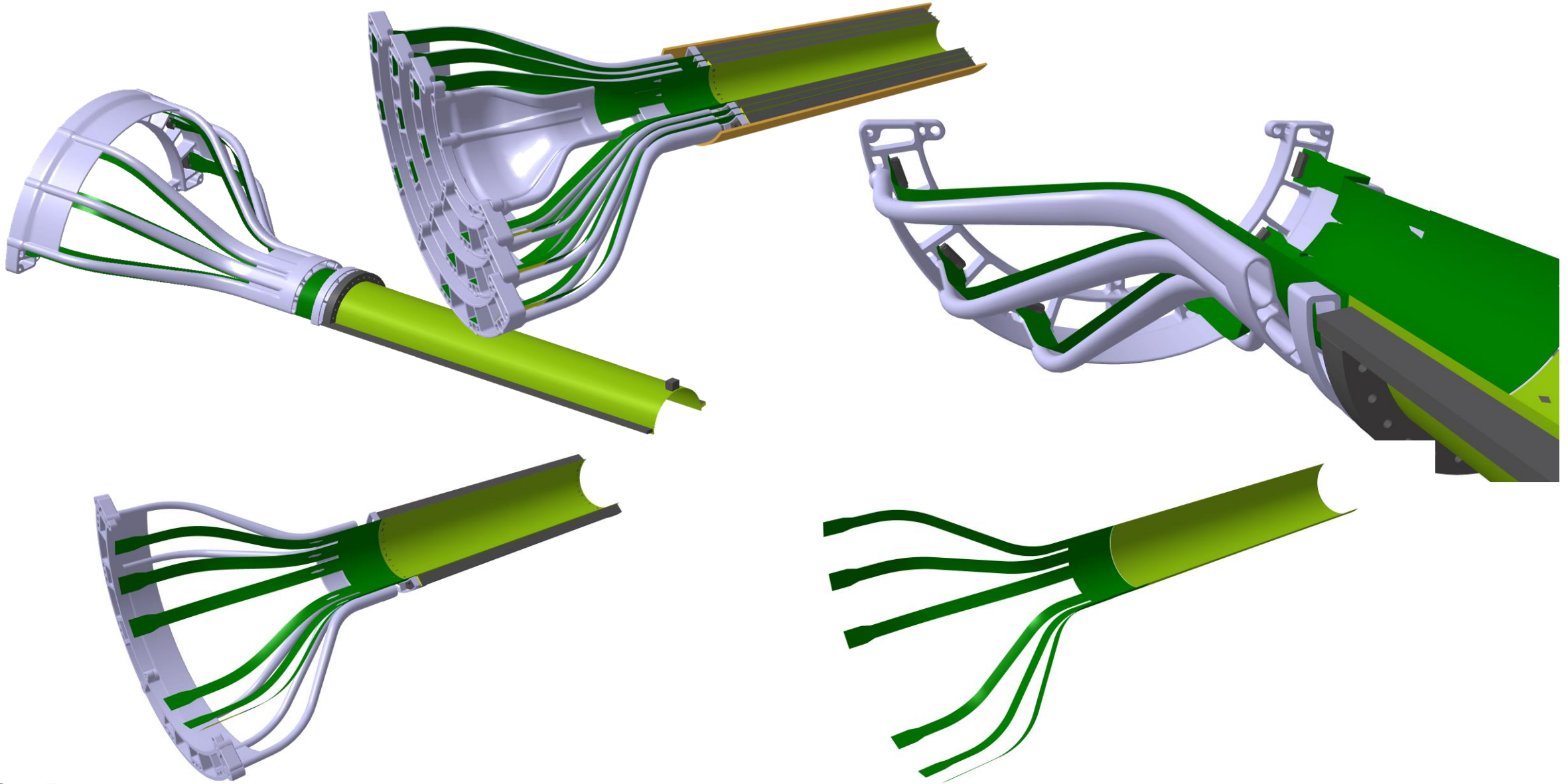


Stack-up preliminary ideas: 4 layers + merging area



A. Junique et al.

Sensor FPC



eRD104 data services reduction plans

- ORNL has a setup similar to the MVTX setup shown in the earlier slide, including the FELIX board and a stave with 9 ALPIDEs, that could serve as a testbed for a MUX board prototype
- Initial work on this eRD is mostly intellectual and can proceed in the absence of funding
- Funding was mostly requested to pay for consultation with engineers at ORNL and BNL
- Concept probably needs some kind of processing on the service reduction (MUX) board in order to reduce bandwidth
- Investigate actual bandwidth requirements
- Investigate environment of possible location of such a MUX board (radiation, magnetic field, cooling, ...)
- Survey of commercial components, special components for radiation tolerance
- Initial work after a conceptual design would be focused on evaluation of the concept with evaluation boards of the various components chosen
- BNL instrumentation investigating possible variation of the sensor design for data transmission optimization, including verification of the design with OO-simulations (UVM)

Radiation Tolerant FPGAs

e.g.:

The screenshot displays the Microchip website's product page for Radiation Tolerant FPGAs. The top navigation bar includes links for Products & Services, Applications, Ordering, Company, Partners, and Support. A search bar is located in the top right corner. The left sidebar lists various FPGA & SoC categories, with 'Rad-Tolerant FPGAs' expanded to show sub-categories like Sub-QML FPGAs, RTAX-S/SL, RTAX-DSP, Prototyping Solutions, RTSX-SU, RT PolarFire FPGAs, RT ProASIC3, RTG4 Radiation-Tolerant FPGAs, Policies & Certifications, and Radiation & Reliability Data. The main content area features a banner for 'Sub-QML FPGAs Bridge the Gap Between COTS and QML Components' and a breadcrumb trail: Home / Products & Services / FPGA & SoC / Rad-Tolerant FPGAs. The 'Rad-Tolerant FPGAs' section includes tabs for Overview, Family Comparison, Flight Heritage, Legacy, Discontinued, Applications, Parametric Search, Ordering, and Support. The 'Overview' tab is active, showing a list of product families: RT PolarFire FPGAs, RTG4 FPGAs, RTAX FPGAs, RT ProASIC3 FPGAs, and RTSX-SU FPGAs. Each family has a brief description and a link to the 'RTAX-DSP' or 'RTAX-S/SL' page. On the right side, there are two callout boxes: 'Radiation-Tolerant Spacecraft Telemetry Controller LX7730' and 'Radiation-Tolerant Spacecraft Motor Controller with Position Sensing LX7720'. A video player is also visible at the bottom right.

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Sub-QML FPGAs Bridge the Gap Between COTS and QML Components
Enabling Cost Reduction and Shorter Lead Times for High Volume Satellite Constellations

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Rad-Tolerant FPGAs

Overview Family Comparison Flight Heritage Legacy Discontinued Applications Parametric Search Ordering Support

RT PolarFire FPGAs

- High-speed signal processing, SONOS-based FPGAs
- 40 to 50% lower power, SEU immune, path to QML-V qualification
- 481,000 LEs, 250 Gbps SERDES bandwidth, 33 Mbits memory, 1480 multipliers

» RT PolarFire FPGA

RTG4 FPGAs

- Radiation Hardened by Design Flash-based FPGA with proven flight heritage
- 300 MHz performance, up to 150,000 LEs, 5 Mbit SRAM
- 462 multipliers, 75 Gbit / second SERDES bandwidth

» RTG4 FPGA

RTAX FPGAs

- High-reliability, radiation-tolerant, antifuse-based FPGAs
- Available with embedded multiply-accumulate blocks for DSP applications
- Qualified to QML Class Q and QML Class V

» RTAX-S/SL » RTAX-DSP

RT ProASIC3 FPGAs

- Reprogrammable, nonvolatile, radiation-tolerant, flash-based FPGAs
- For low-power space applications, requiring up to 350 MHz operation
- Qualified to QML Class Q

» RT ProASIC3

RTSX-SU FPGAs

- High-reliability, radiation-tolerant antifuse-based FPGAs
- Compact packaging for command and control applications
- Flight heritage established on many programs

» RTSX-SU

Space System Managers are companion devices that can be used with any Radiation-Tolerant FPGAs

Radiation-Tolerant Spacecraft Telemetry Controller LX7730

Radiation-Tolerant Spacecraft Motor Controller with Position Sensing LX7720

Microsemi: Lea...

Microchip PolarFire FPGA

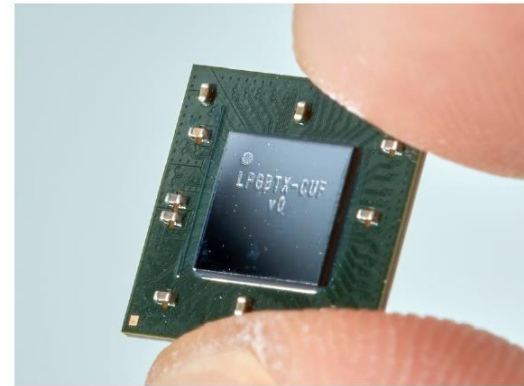


		MPF050	MPF100	MPF200	MPF300	MPF500
FPGA Fabric	Logic Elements (4LUT + DFF)	48K	109K	192K	300K	481K
	Math Blocks (18 × 18 MACC)	150	336	588	924	1480
	LSRAM Blocks (20 Kb)	160	352	616	952	1520
	uSRAM Blocks (64 × 12)	450	1008	1764	2772	4440
	Total RAM (Mb)	3.6	7.6	13.3	20.6	33
	uPROM (Kb)	216	297	297	459	513
	User DLLs/PLLs	8	8 each	8 each	8 each	8 each
High-Speed I/O	250 Mbps–12.7 Gbps Transceiver Lanes	4	8	16	16	24
	PCIe® Gen 2 Endpoints/Root Ports	2	2	2	2	2
Total I/O	Total User I/O	176	296	364	512	584

Rad-Hard Optical Interconnect: “IpGBT”

More than a “Communications ASIC”

- Capable of
 - 5.12 or 10.24 Gbps (for uplinks)
 - 2.56 Gbps (for downlinks)
- Enables the implementation of RadTol links
 - DAQ
 - Trigger (constant and deterministic latency)
 - Experiment control [slow control]
- Implements Control and Monitoring Functions
 - Three I2C Masters
 - 16 – bit General Purpose I/O port
 - Output reset pin
 - 10 – bit ADC (8 multiplexed inputs)
 - 8 – bit voltage DAC
 - 8 – bit current DAC
 - Temperature sensor
- Designed for radiation hardness
 - Total Ionizing Dose (TID): 200 Mrad
 - Extensive SEU protection (TMR, FEC)



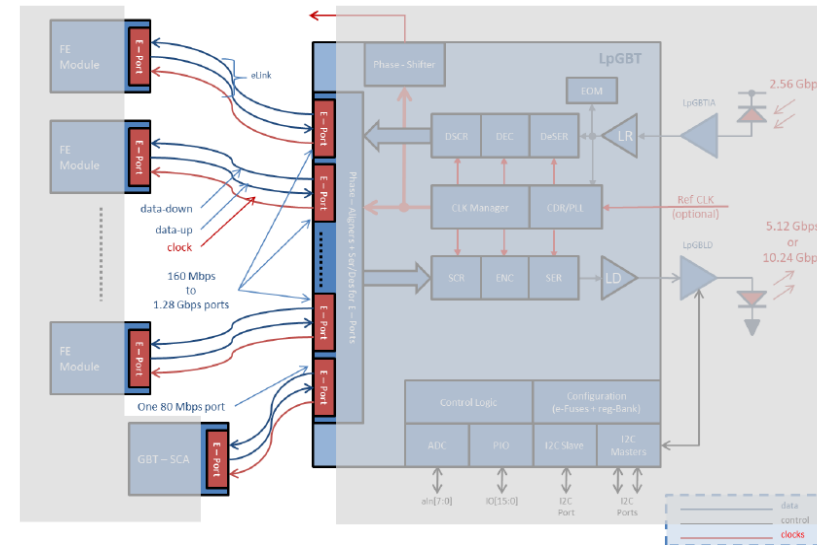
Pin count: 289 (17 x 17)
Pitch: 0.5 mm
Size: 9 mm x 9 mm x 1.25 mm

M. Firlej, et al., “An IpGBT sub-system for environmental monitoring and control of experiments” (Fri @ 09:50)

IpGBT Capabilities

Communicates with

- The counting room
 - Optical fibre links
- The FE modules / ASICs
 - Electrical links (eLinks)
- The Number and Bandwidth of eLinks is programmable
- For Down eLinks
 - Bandwidth: 80/160/320 Mbps
 - Count: 16/8/4
- For Up eLinks



Input eLinks (uplink)												
uplink bandwidth [Gbps]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mbps]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

High-Speed Interconnects

FUTURE-PROOF MICRO FOOTPRINT

Flexibility of copper and optical using the same micro connector allows for increased density, simplified PCB and reduced power dissipation.

HIGH PERFORMANCE VERSATILITY

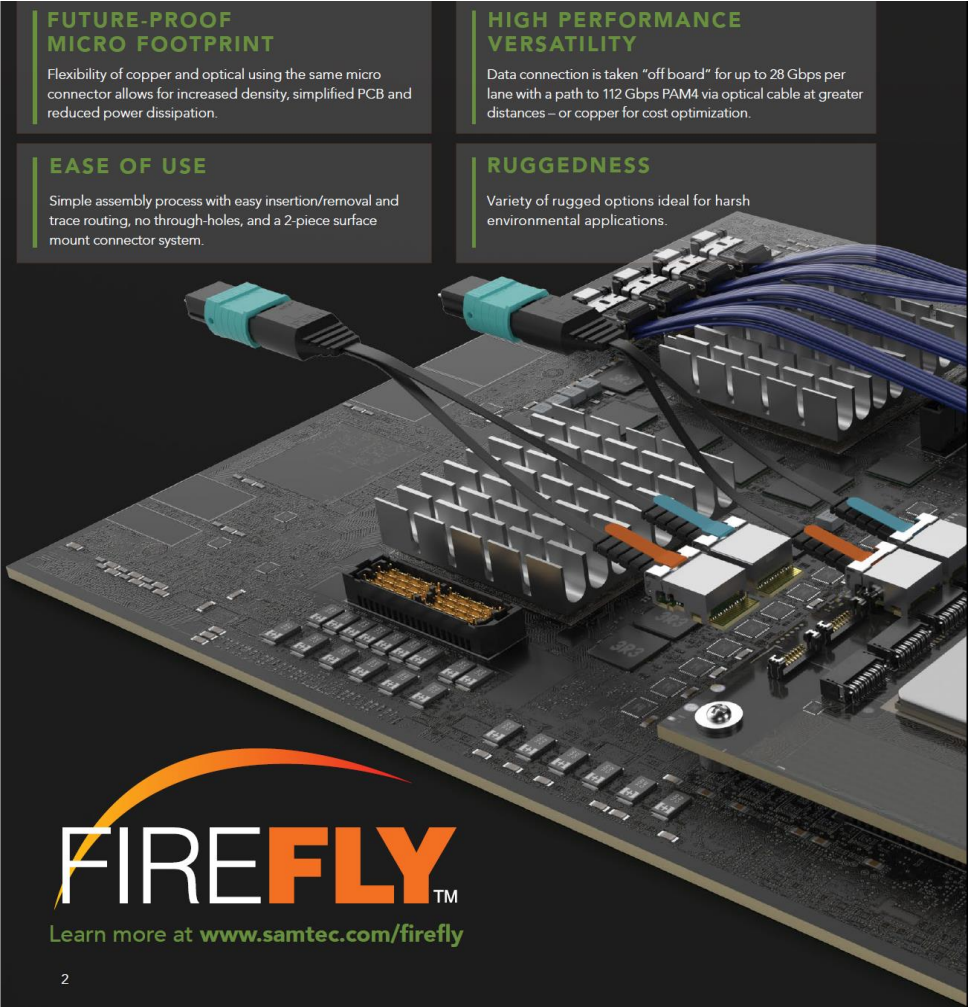
Data connection is taken "off board" for up to 28 Gbps per lane with a path to 112 Gbps PAM4 via optical cable at greater distances – or copper for cost optimization.


EASE OF USE

Simple assembly process with easy insertion/removal and trace routing, no through-holes, and a 2-piece surface mount connector system.

RUGGEDNESS

Variety of rugged options ideal for harsh environmental applications.





Learn more at www.samtec.com/firefly

COMMERCIAL
FIREFLY™



FIREFLY™

Actual Size

Data connection is taken "off board," simplifying board layout and enhancing signal integrity from IC to faceplate

- Up to 28 Gbps per channel via optical cable for greater reach
- Industry leading miniature footprint allows for higher density close to the data source
- Simple to use system with easy insertion/removal and trace routing, no through-holes, and a surface mount connector system
- Supports data center, HPC and FPGA protocols, including 10/40/100 GbE Ethernet, InfiniBand™, Fibre Channel and Aurora

14 G b p s	x4 x12	25 G b p s	x4 x12
16 G b p s	x12	28 G b p s	x4

ECUO	WIDTH	DATA RATE	CABLE LENGTH	0	HEAT SINK	1	FIBER TYPE	END 2 OPTIONS*
-B04 = 4 Tx + 4 Rx -T12 = 12 Tx -R12 = 12 Rx -Y12 = 12 Tx + 12 Rx -U12 = 12 Channel AOC (Unidirectional)	-14 = 14 Gbps per lane -16 = 16.1 Gbps per lane (N/A -B04) -25 = 25.7 Gbps per lane -28 = 28.1 Gbps per lane (-B04 only)	- "XXX" = Overall Length in Centimeters	-1 = Flat -2 = Pin-fin (-14 & -16 only) -3 = Flat with groove -4 = PCIe® Pin-fin (-14 & -16 only) -5 = 1.75 cm tall Pin-fin (-B04 only)	-4 = Aqua loose tube with Boot -5 = Jacketed ribbon with boot -6 = Jacketed ribbon -7 = Black loose tube with boot -8 = Black loose tube	-Y12 requires -2X end option (Leave blank for -U12) 12 Fibers -01 = MTP® Male -02 = MTP® Female -07 = MXC® Internal Plug -0E = MPO Plus®, Male, bayonet 24 Fibers -21 = MTP® Male -22 = MTP® Female -27 = MXC® Internal Plug -2E = MPO Plus®, Male, bayonet			

* These are standard options. See page 5 for other end options available.

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