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eRD104: "Readout Services Reduction" Updates

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ORNL

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U.S. DEPARTMENT OF ENERGY

eRD104 Overall Plan

Services Reduction intent is to investigate methods to significantly reduce the services load for an EIC MAPS based tracking detector. This can be broken down into the largest components:

Powering (Birmingham, RAL)

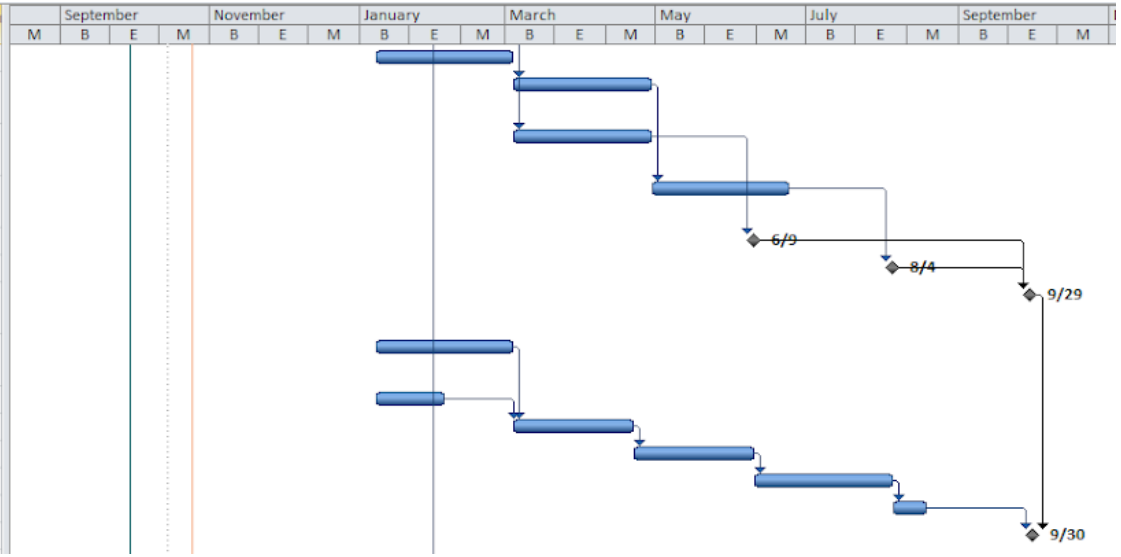
- Investigate the use of DC-DC converter-based architectures to significantly reduce the number of wires needed to power the detector. This will require that we introduce radiation tolerant DC-DC converters into the detector structure in proximity to the disc/stave connection points.
- Investigate the use of serial powering architectures with the same effect. This will require that we introduce regulation at the (stitched) sensor level either on die or as a hybrid arrangement.
- Assess detector design goals and apply the best overall optimization of available technologies studied under R&D to the final implementation of the detector (tracking and others who are interested in working on this)

Data (ORNL, BNL)

- Investigate the use of data aggregation on detector using radiation tolerant FPGAs to receive multiple data streams from sensor blocks (over twinax/FPC) and multiplex and transmit the data out via high-speed fiber ribbon connections to RDO boards (or FELIX). This will require functionality in the MUX boards to steer control and configuration and additional power for the MUX boards in detector. Again, the final R&D goal is to develop an optimized viable system for minimizing the services loads due to signal transmission.

2022 Work Plan and Schedule

	Task Mode	Task Name	Duration	Start	Finish	Predecessors	Resource Na
37		Gather serial powering data	40 days	Fri 1/7/22	Thu 3/3/22		
38		design and analyze DC-DC converter architectures	40 days	Fri 3/4/22	Thu 4/28/22	36	
39		design and analyse serial powering architectures	40 days	Fri 3/4/22	Thu 4/28/22	36	
40		cost/benefit analysis of serial and DC-DC	40 days	Fri 4/29/22	Thu 6/23/22	38	
41		report on serial powering	30 days	Fri 4/29/22	Thu 6/9/22	39	
42		report on DC-DC powering	30 days	Fri 6/24/22	Thu 8/4/22	40	
43		FY22 assessment report on powering options	40 days	Fri 8/5/22	Thu 9/29/22	41,42	
44		gather data rate and speed data	40 days	Fri 1/7/22	Thu 3/3/22		
45		rad tolerant FPGA survey	20 days	Fri 1/7/22	Thu 2/3/22		
46		architecture survey	35 days	Fri 3/4/22	Thu 4/21/22	44,45	
47		conceptual design(s)	35 days	Fri 4/22/22	Thu 6/9/22	46	
48		cost benefit analysis	40 days	Fri 6/10/22	Thu 8/4/22	47	
49		report on MUX options	10 days	Fri 8/5/22	Thu 8/18/22	48	
50		erd104 FY22 report	1 day?	Fri 9/30/22	Fri 9/30/22	49,43	



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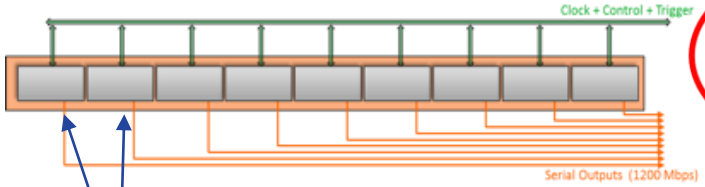
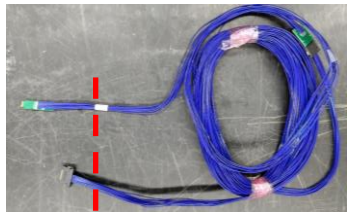
Starting Point: Current ALICE ITS-2 / sPHENIX MVTX

9-sensor **Stave**



ALPIDE **Sensors**



11.6 m twinax

Data (9 x 1.2Gbps),
40 MHz Clock, Control/Trigger

Readout Unit
Front End

85m
GBT Optical Links

Control

Data (3x3.2 Gbps)

Trigger

FELIX
Back End

PCIe

Clock/Trigger

DAQ and Slow Control

Trigger

DAQ Room

Power

Power

CAEN Power Supplies

Regulated power

13.3m

Power Board

Interaction Region

Experimental Hall

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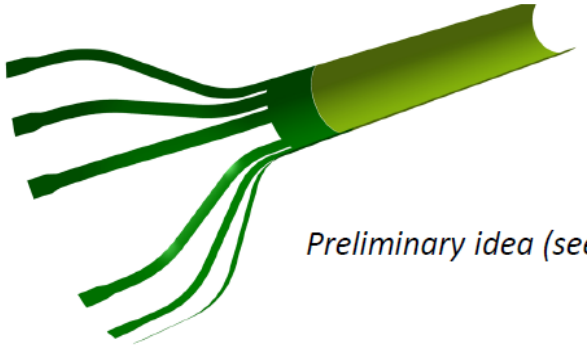
Conversation with Gianluca:

- Marcel (Utrecht) has shown experimentally that the line rate limits on the ITS2 data cables are not much above 2Gb/s. Certainly NOT possible to transmit much faster than that on those distances.
- Marcel has experimentally studied and demonstrated experimentally a solution with active re-generation of the signals by active repeaters on small break-boards at the junction off cable segments.
- Current estimates for one 'stave' of the ITS3 sensor (that is one standalone module, not one chip), is that we might have up to 8 links at 5 Gb/s.
- The inner layer chip, half cylinder, would be made with three staves on one die, that is 24 links at 5 Gb/s from the half cylinder of the innermost layer, total 120 Gb/s.
- The equivalent ITS2 innermost layer is 6 staves * 9 chips * 1.2 Gb/s = 64.8 Gb/s
- Encoding is also supposed to change, going from 8b10b to a more efficient and better performing code compatible with FPGA receivers (Marcel looked into 64b/66b I think).

FPC development has started

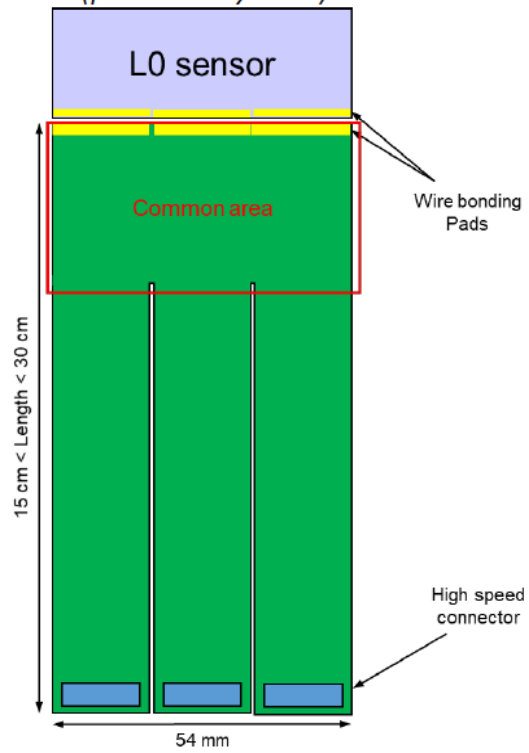


Preliminary idea (see WP5)

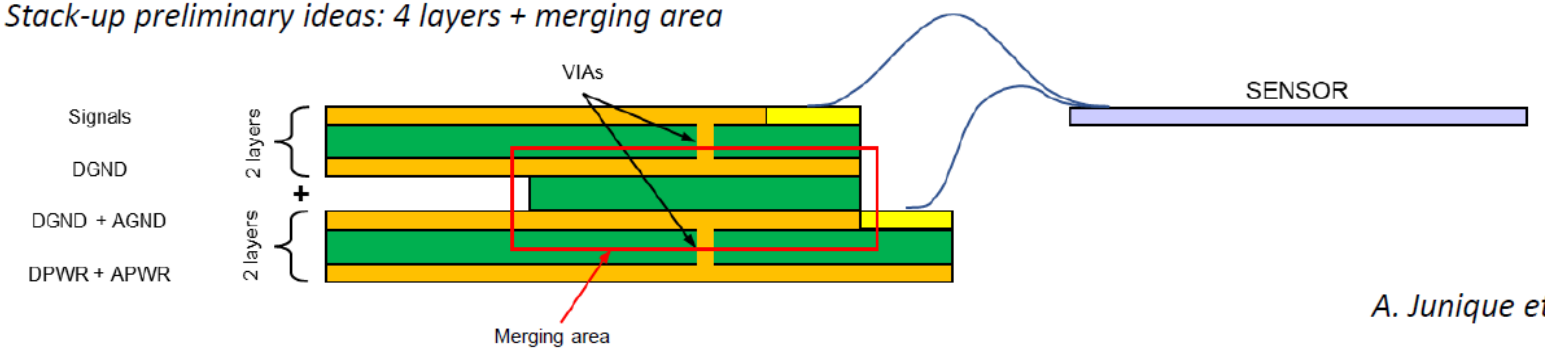
For each sensor unit of 18 mm in r-phi (3,4,5 for Half-L0,L1,L2):

- DATA: 40 Gb/s total bandwidth over 8 x 5 Gb/s transmitters
- POWER domains: analog, digital, HSdata
  - density: 40 mW/cm^2 over whole area + 30-50 mW per transmitter
  - backbone bus power to be evaluated; need for sense wires
- LAYOUT: Cu on A-side, Al/Cu FPC or power cables on C-side
  - investigate multi-layer solutions (bending radii, stiffness, resistances)
- SERVICE BARREL:
  - HSdata repeaters, optical links, power regulators under evaluation

FPC top view: common area option (preliminary idea)

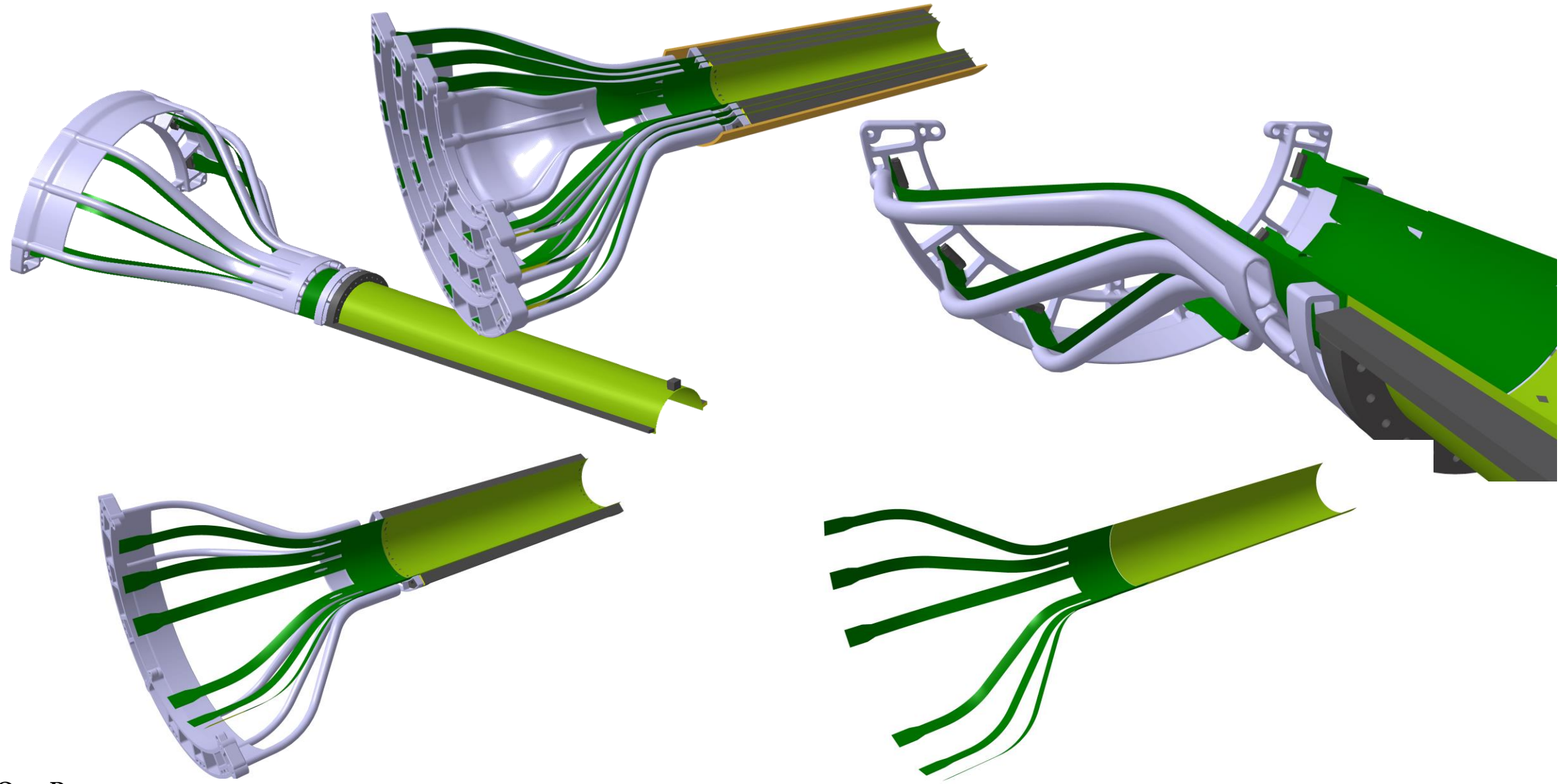


Stack-up preliminary ideas: 4 layers + merging area



A. Junique et al.

Sensor FPC

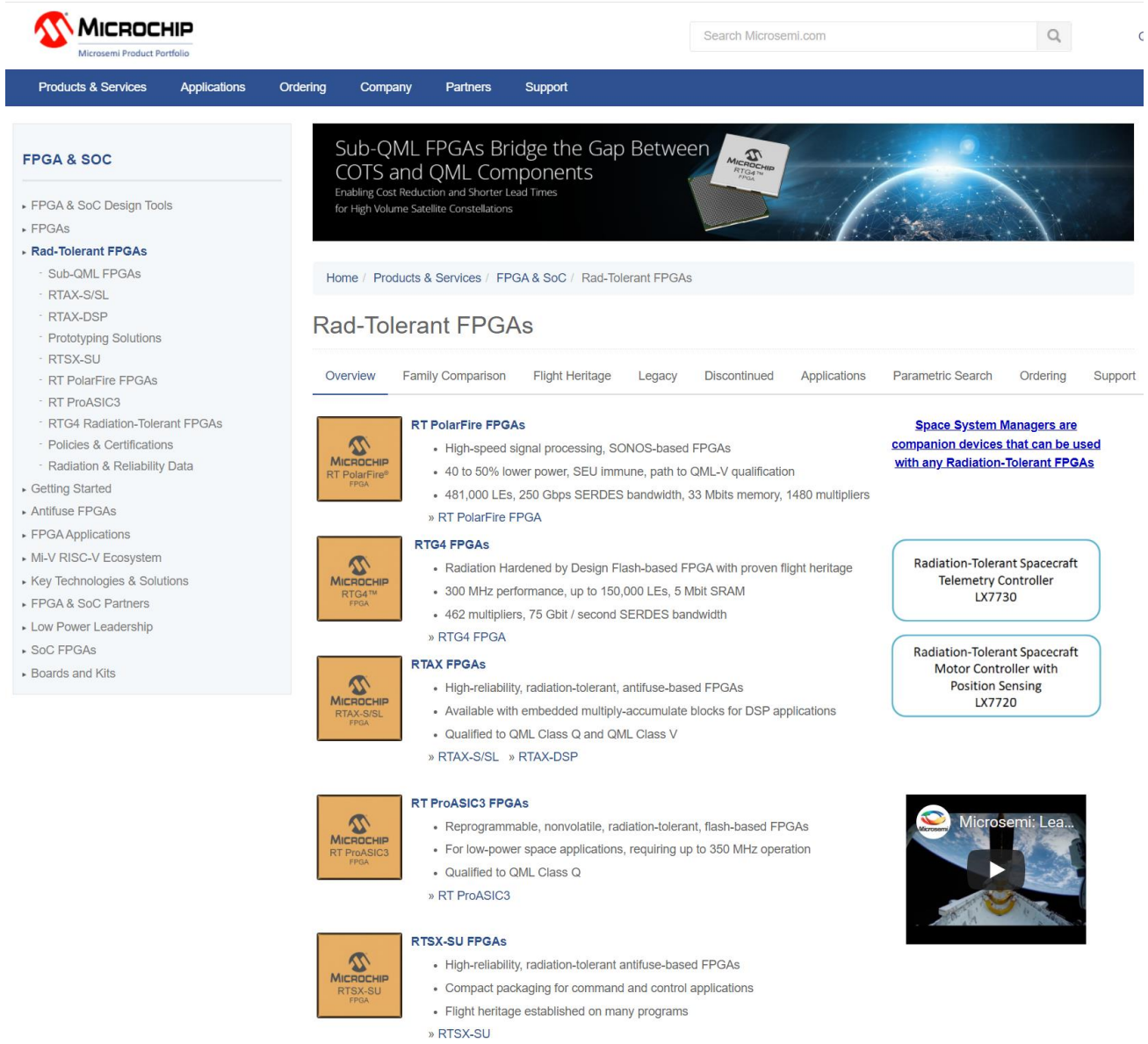


eRD104 data services reduction plans

- ORNL has a setup similar to the MVTX setup shown in the earlier slide, including the FELIX board and a stave with 9 ALPIDEs, that could serve as a testbed for a MUX board prototype
- Initial work on this eRD is mostly intellectual and can proceed in the absence of funding
- Funding was mostly requested to pay for consultation with engineers at ORNL and BNL
- Concept probably needs some kind of processing on the service reduction (MUX) board in order to reduce bandwidth
- Investigate actual bandwidth requirements
- Investigate environment of possible location of such a MUX board (radiation, magnetic field, cooling, …)
- Survey of commercial components, special components for radiation tolerance
- Initial work after a conceptual design would be focused on evaluation of the concept with evaluation boards of the various components chosen
- BNL instrumentation investigating possible variation of the sensor design for data transmission optimization, including verification of the design with OO-simulations (UVM)

Radiation Tolerant FPGAs

e.g.:



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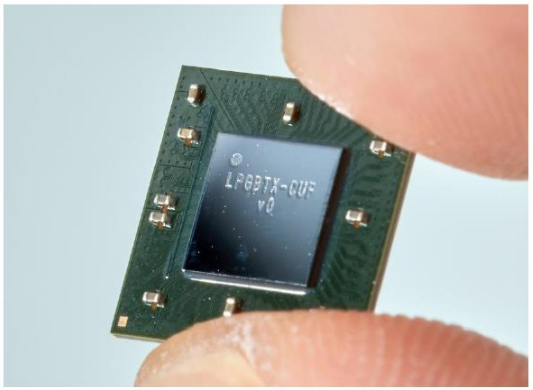
Microchip PolarFire FPGA

		MPF050	MPF100	MPF200	MPF300	MPF500
FPGA Fabric	Logic Elements (4LUT + DFF)	48K	109K	192K	300K	481K
	Math Blocks (18 × 18 MACC)	150	336	588	924	1480
	LSRAM Blocks (20 Kb)	160	352	616)	952	1520
	uSRAM Blocks (64 × 12)	450	1008	1764	2772	4440
	Total RAM (Mb)	3.6	7.6	13.3	20.6	33
	uPROM (Kb)	216	297	297	459	513
	User DLLs/PLLs	8	8 each	8 each	8 each	8 each
High-Speed I/O	250 Mbps–12.7 Gbps Transceiver Lanes	4	8	16	16	24
	PCIe® Gen 2 Endpoints/Root Ports	2	2	2	2	2
Total I/O	Total User I/O	176	296	364	512	584

Rad-Hard Optical Interconnect: "lpGBT"

More than a "Communications ASIC"

- Capable of
  - 5.12 or 10.24 Gbps (for uplinks)
  - 2.56 Gbps (for downlinks)
- Enables the implementation of RadTol links
  - DAQ
  - Trigger (constant and deterministic latency)
  - Experiment control [slow control]
- Implements Control and Monitoring Functions
  - Three I2C Masters
  - 16 – bit General Purpose I/O port
  - Output reset pin
  - 10 – bit ADC (8 multiplexed inputs)
  - 8 – bit voltage DAC
  - 8 – bit current DAC
  - Temperature sensor
- Designed for radiation hardness
  - Total Ionizing Dose (TID): 200 Mrad
  - Extensive SEU protection (TMR, FEC)



Pin count: 289 (17 x 17)
Pitch: 0.5 mm
Size: 9 mm x 9 mm x 1.25 mm

M. Firlej, et al., "An lpGBT sub-system for environmental monitoring and control of experiments" (Fri @ 09:50)

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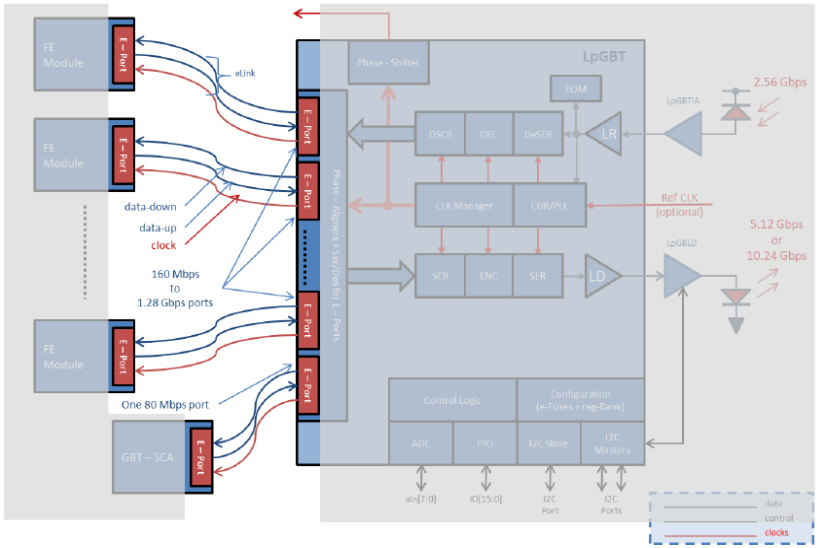
lpGBT Capabilities

Communicates with

- The counting room
  - Optical fibre links
- The FE modules / ASICs
  - Electrical links (eLinks)
- The Number and Bandwidth of eLinks is programmable
- For Down eLinks
  - Bandwidth: 80/160/320 Mbps
  - Count: 16/8/4
- For Up eLinks



Input eLinks (uplink)												
uplink bandwidth [Gbps]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mbps]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

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High-Speed Interconnects