Forward Calorimeter Readout options

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Forward Calorimeter requirements

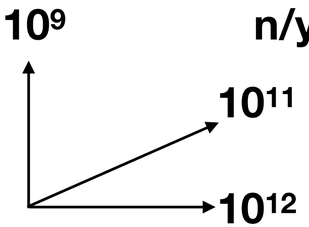
ECal:
- 1 MIP ~ 350 MeV
- Maximum range ~ 100 GeV
  - 300 MIPs per channel

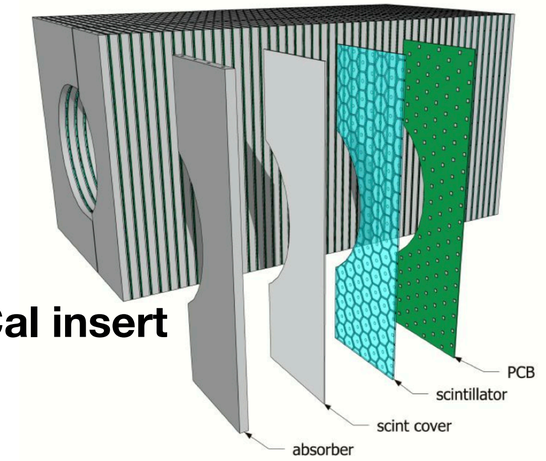
HCal:
- 1 MIP ~ 200 MeV per channel
- Max range 120 GeV:
  - ~50 GeV per channel (longitudinal segmented)
  - 250 MIP range (could be also higher)

HCal Insert:
- Based on CALICE prototype

Total number of channels:
~ 63k channels for LFHCAL
~ 25k channels for ECAL
~ 8k channels for the insert
- sPHENIX readout method is maybe not feasible for this calorimeter due to the limiter (10 cm) space in Z

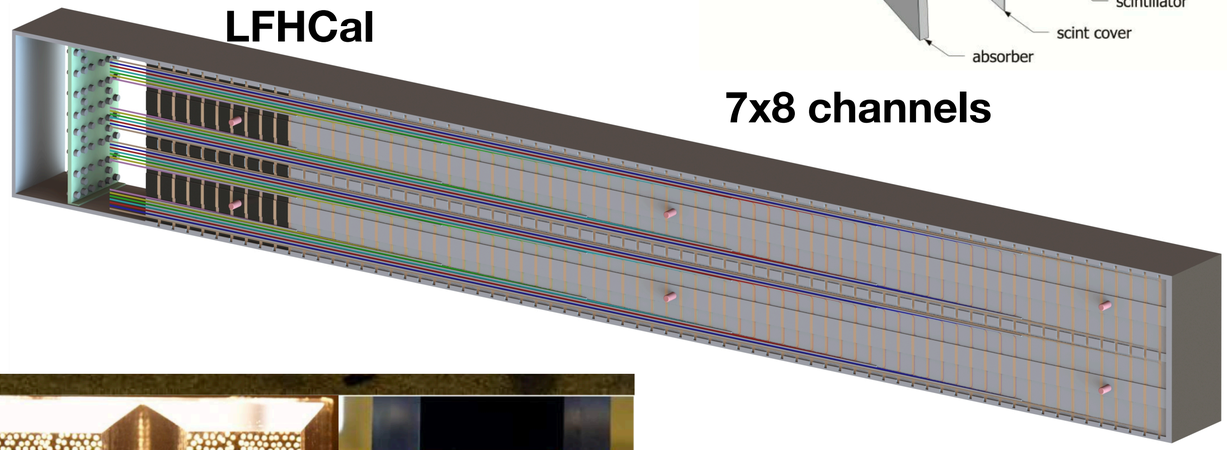
RadHard requirements



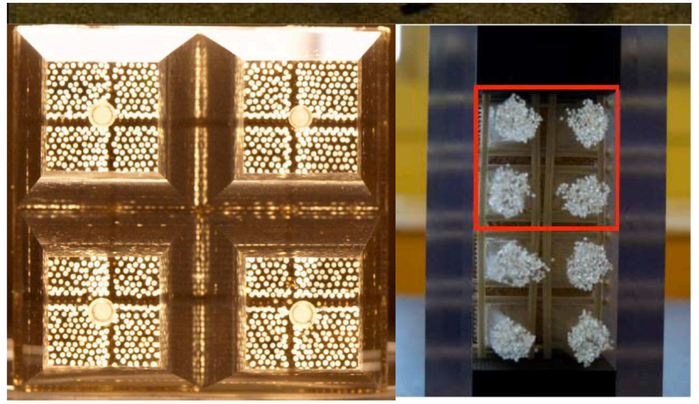


HCal insert

LFHCal



7x8 channels



ECal

Options discussed

1. **STAR FCS solution:**
   - 2000 channels readout at STAR
   - 180mW/channel
   - Cables bring up the signal to the ADC:
     - STAR 32 ch 80MSPS 12 bit ADC (can be upgraded to 14 bit, pin compatible)
     - 2x 3.2 Gb/s fiber links
   - ADC can be on the detector also (see option 3 then)
2. **HGCROCv3 from CMS HGCAL:**
   - 80 channel per ASIC
   - 20 mW/channel
   - Low noise < 0.3 fC
   - Large dynamic range 0.2 fC - 10 pC
   - Output of 2x1.28 Gb/s for data and 4x1.28 Gb/s for trigger
   - R&D:
     - Clock adaption from 40 MHz to 100 MHz
     - Input capacitance up to 2 nF
3. **ASIC from Pacific MicroCHIP Corp:**
   - 32 channel per ASIC
   - 25-36 mW/channel
   - 500 MS/s sampling rate
   - 32x8Gb/s output rate
   - R&D:
     - Available from end of 2022 (pre-Covid schedule)
     - RadHard? It is made for x-ray and gamma-ray detector, maybe not enough for EIC

STAR FCS readout

ECal:
44x34 towers ~ 1496 ch

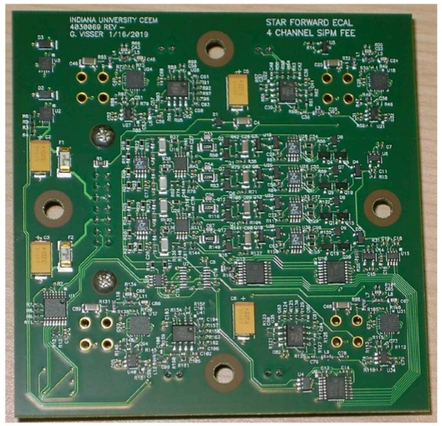
HCal:
26x20 towers ~ 520 ch

Frontend amplifier and shaper on detector

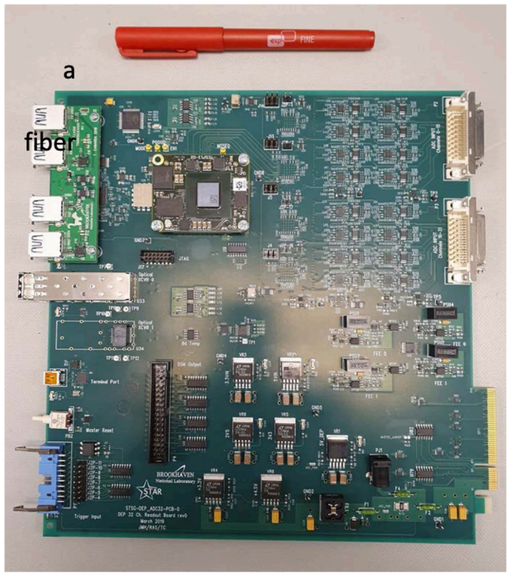
SiPM bias voltage control on detector

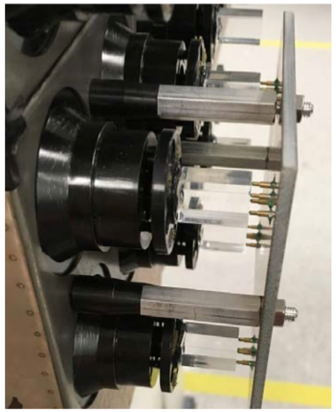
FEE is magnetic tolerant

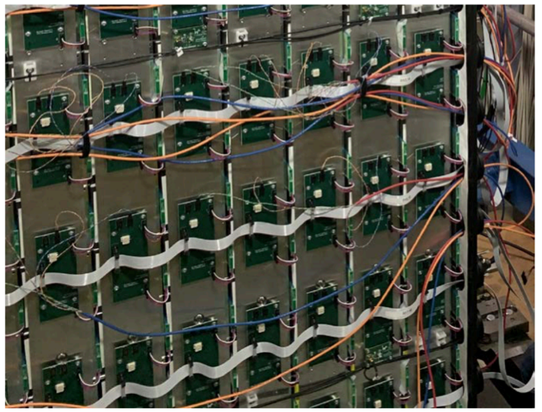
80 MSPS, 12 bits - can be upgraded to 14 bits (same pinout)



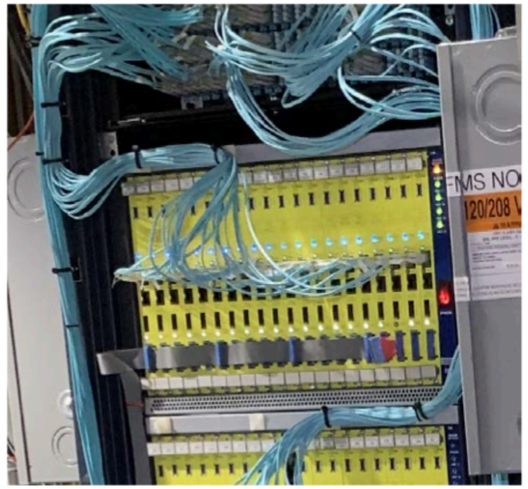
FEE Implementation – ECAL





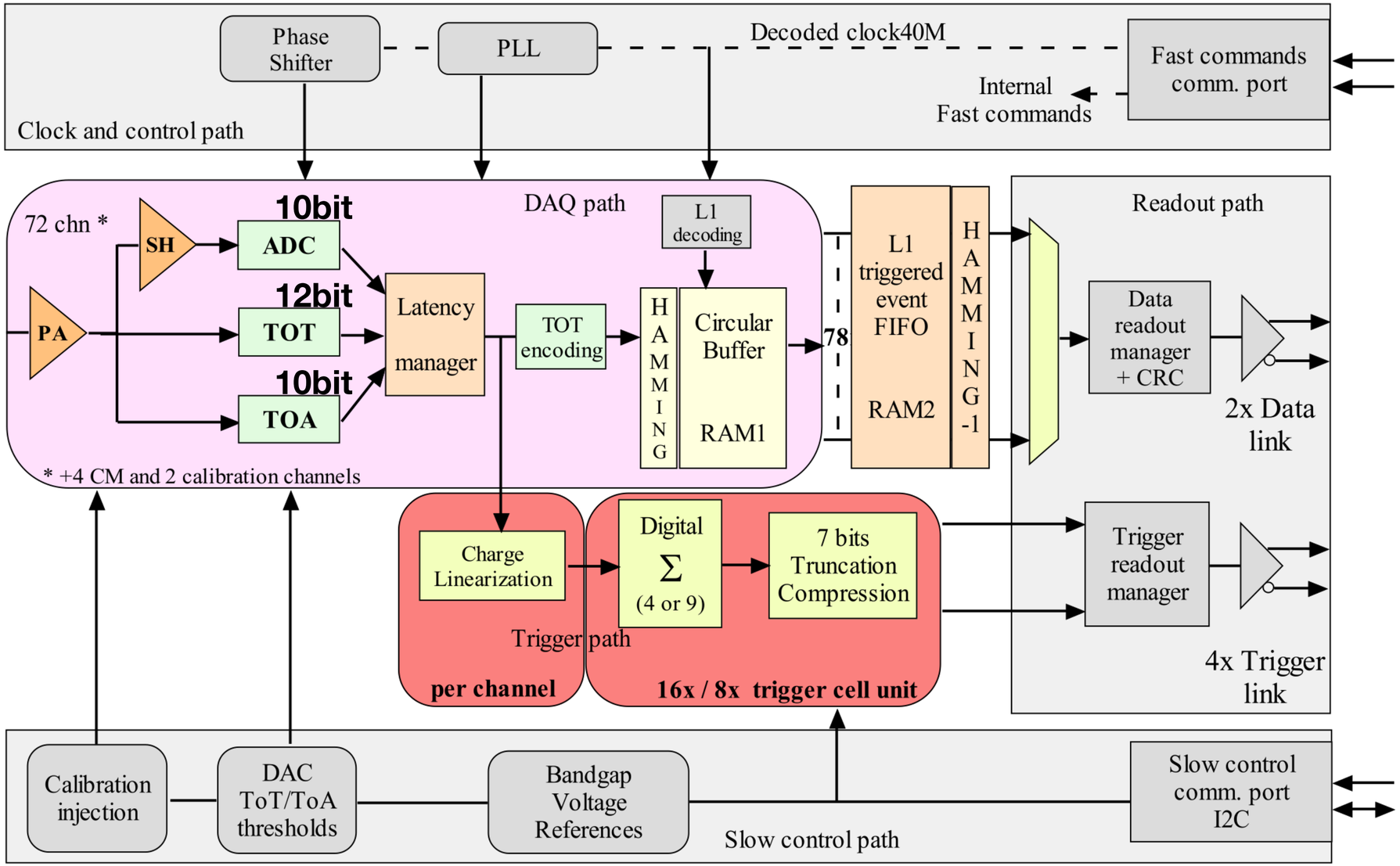


HCAL: Same concepts, except short cable connection to SiPM board instead of pogo pin connection. Much more room than on ECAL.



HGCROC Overview II

- Low noise and large dynamic range 0.2 fC to 10 pC
- Linearity better than 1% on the full range
- Fast shaping time (peak time < 20 ns)
  - *Reduction of overlap hits in LHC (with 40 MHz)*
- High speed readout links (1.28 Gb/s)
  - *Max readout is 960 kHz*
  - *Possible 'virtual streaming' readout at 500 kHz EIC interaction rate*
- Low power budget < 20 mW
  - *No cooling*
  - *Each channel can adjust bias voltage*
- High radiation resistance
  - *Up to 10^{13} neutron per year (forward LHC-HL run)*



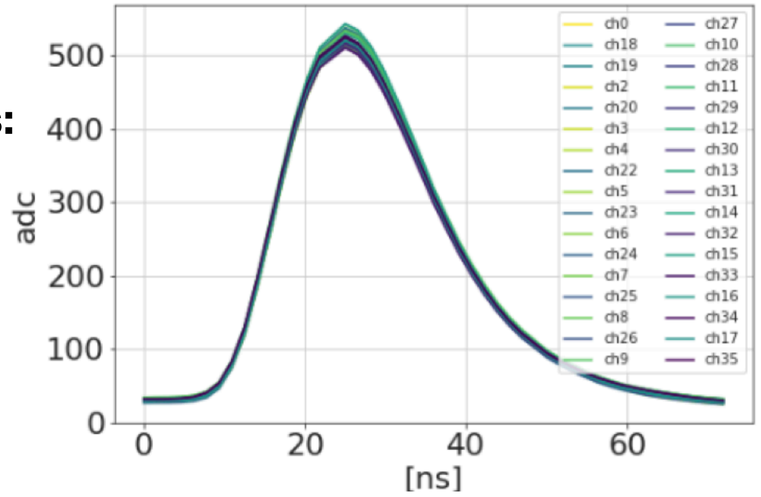
The development group (Omega) is exploring some modifications to suit the EIC needs better

Do they exists? - Yes

20 euro/chip

Test the ASIC electronics:

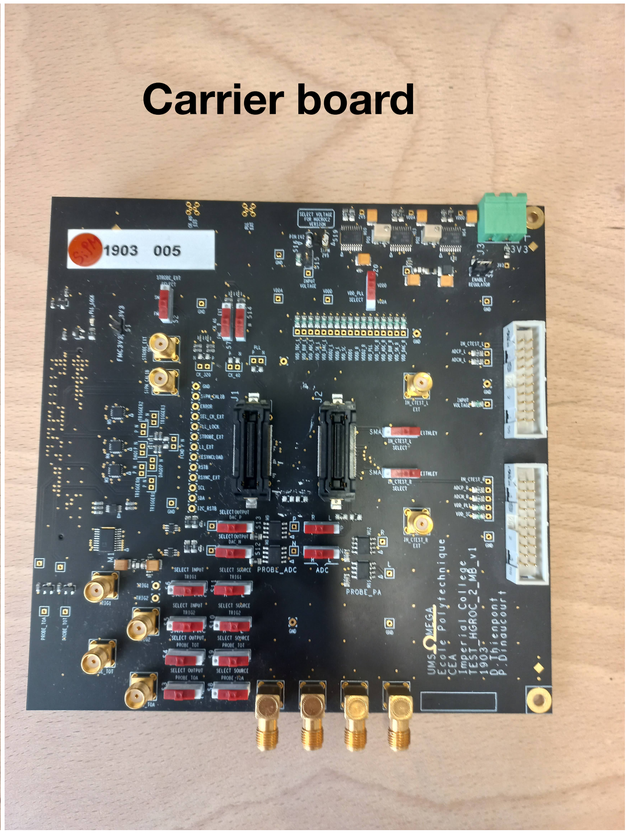
- Chip with mezzanine board
- Carrier board
- KCU board
- Firmware



HGCROCv3 will be delivered to ORNL by end of Aug.

Chip + mezzanine

Carrier board



Few outstanding issues to consider:

- Clock is 40 MHz (and 320 MHz derived)
  - Maybe with some R&D they can increase it 50 MHz
  - 40 MHz might be enough for the EIC:
    - Low occupancy
    - < 500 kHz interaction rate
- We plan to test with multiple SiPM for readout

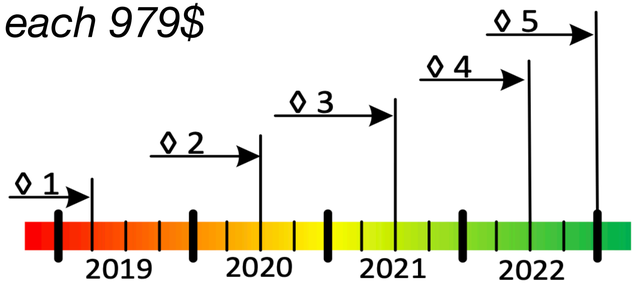
Consideration of readout electronics:
The HGCROC can be connected to an FPGA board (safely outer of the high radiation area) and the FPGA can communicate to the FELIX board. The FPGA code is simple, just shipping the data (maybe zero suppression), so it can be triple multiplied to avoid SEU.

A 32 channel ASIC for X- and ɣ-ray

Pacific MicroCHIP Corp.

- 32 independently operated channels
- Programmable sampling rate of 200/100/50 MS/s
- 1Vpp differential input swing
- Digitizing ENOB > 10-bit
- Input signal bandwidth > 0.2GHz
- Integrated 32ch event-building digital back-end
- Optional direct ADC output through JESD204B interface • Event data packet output through UART interface
- Power consumption < 4.5mW/channel (JESD204B is off) • Total power with ADC data interface <880mW.
- I2C interface for ASIC control
- Chip layout footprint 7.8mm2
- 15mm x 15mm 361 ball BGA package

For ~4k chips each 979$



Questions:

- **RadHard?**
- **Does it exist already?**

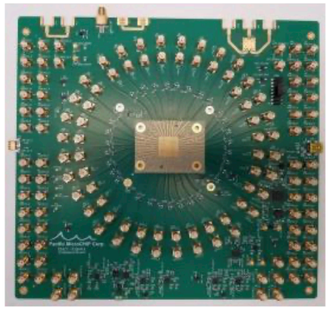


Figure 2. A Chip photo (left), BGA package (center) and the ball array (right).

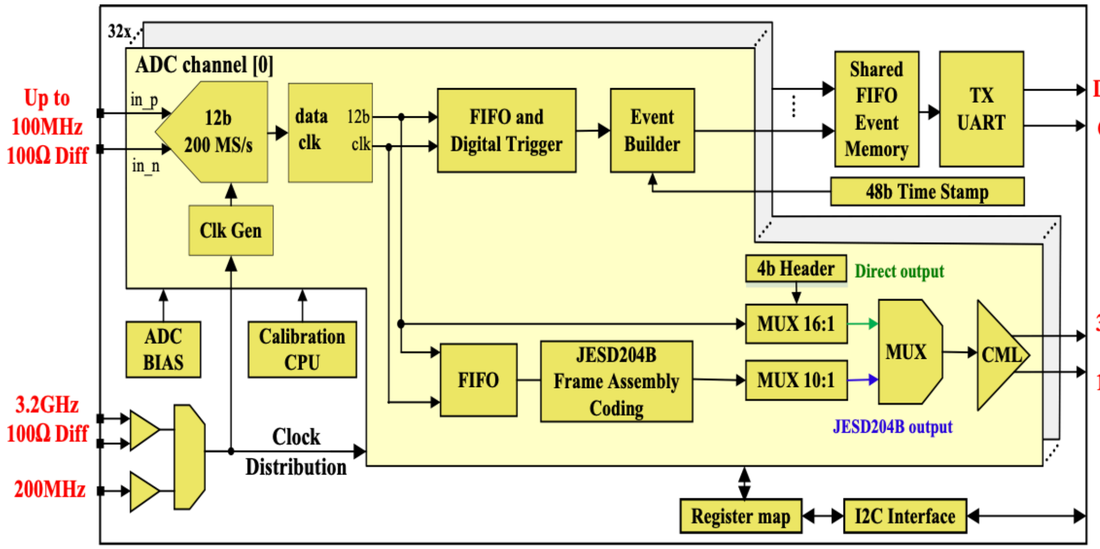


Figure 1. A block diagram of the ASIC.

Summary

Readout electronics requirements for the forward calorimetry:

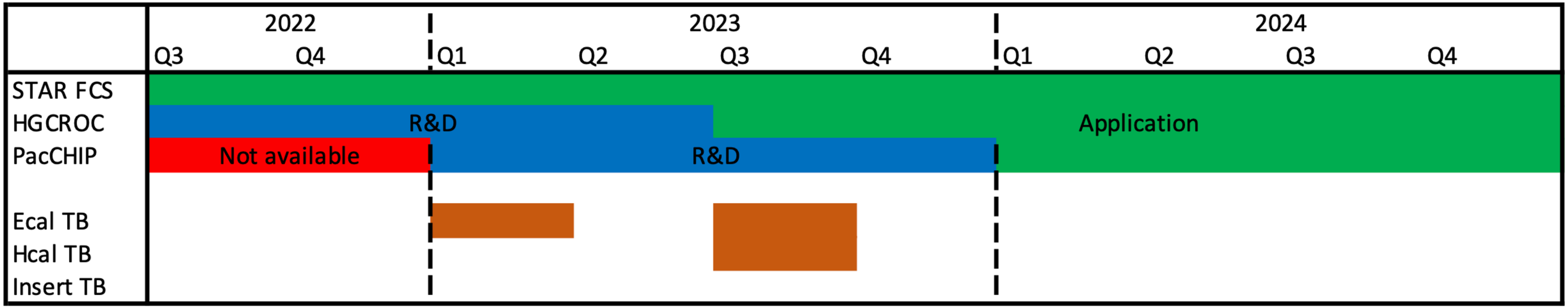
- Dynamic range had to cover from 1 MIP to 100 GeV showers (~300 MIP)
- Compact readout due to the lack of space
- Cost effective to cover ~100k channels
- Low power consumption (no cooling)

We discussed three options:

- Short term solution with the STAR FCS:
  - Ready to use for testbeam next year
  - Move the ADC towards the detector
- Long term solution:
  - 2 different ASICs in consideration now:
    - HGCROC:
      - Good, need some R&D to check the clock and input capacitance
    - Pacific MicroCHIP ASIC:
      - Good, more pricey, RadHard and availability in question

Timeline

Very very first plans

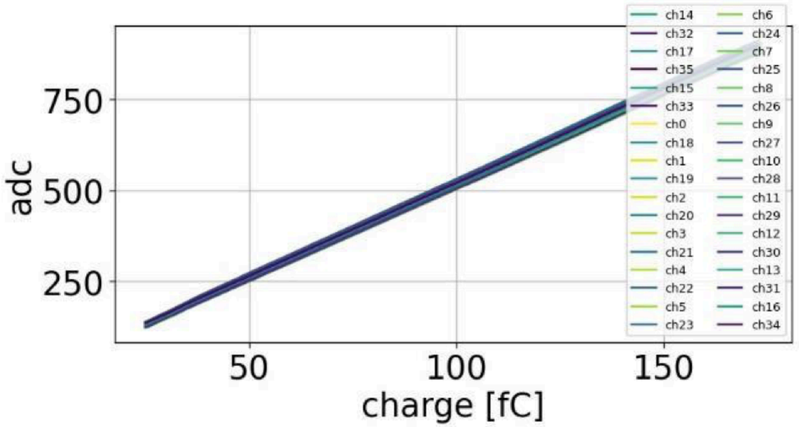


Backup

Some of the results

Results from the Silicon sensor testing (not yet from SiPM version):

- Large dynamic range - 1 MIP … 4000 MIP/channel
- Can tune the gain to enhance the S/B ratios



Very good linearity