Preliminary Thoughts on the Electronics & DAQ of the EIC Detector TOF

(a pre-Strawman)

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Geometry (taken from ECCE Proposal)

- Barrel: 63 cm radius, 128+128 cm length
  - 102000 cm2 area
  - 396 cm circumference
  - assuming 5cm wide staves ⇒ 400cm/5cm ⇒ 80 x 2 sides ⇒ 160 [1] staves
    - BTW, I call “stave” the 2D readout module for lack of a better name
    - Assumption: each “stave” is readout by 1 Readout Board (“RDO”) with 1 fiber to DAQ located at its end
- Endcap L: 64 cm radius (5 cm annulus; ignored)
  - 13000 cm2 area
  - 402 cm circumference
  - I will assume # of staves scales with the area from above + 1.5x fudge factor ⇒ 30 [2] “staves”
- Endcap R: 85 cm radius (5 cm annulus; ignored)
  - 23000 cm2 area
  - 534 cm circumference
  - argument from above ⇒ 50 [3] “staves”
- Total stave count: 240

“Stave” Interconnects to External Services

- recap: stave average size 5 cm X 128 cm ⇒ 640 cm2
  - assuming pixel size 500 um X 1 cm [4] ⇒ ~13000 channels per stave
  - assuming 225 channels per ASIC ⇒ ~60 ASICs per stave (likely not right, depends on EICROC)
  - FLEX cables and interconnect? weight?
- 1 fiber pair data link to DAQ Receiver Board
  - detector data from TOF **to** DAQ e.g. ~10 Gb/s fiber rate
  - control data **from** DAQ to TOF ASIC etc
- 1 fiber (pair?) from DAQ for the clock (e.g. 10-100 MHz)
  - also for framing/triggering primitives sent in deterministic real-time? TBD
- 1 copper cable for the bias voltage
  - xx V? power? current? control? status?
  - dimensions? weight?
- 1 copper cable for the low voltage
  - with 300 mW/cm2 for the ASIC (e.g. ALTIROC) ⇒ 640 cm2 X 300 mW ⇒ 192 W per stave
  - naively, 1.2V requires 160 Amperes
  - and also add e.g. 20-50 W for other electronics: PLL, fiber transmitters/receivers, FPGA?, etc.
    - likely at 3.3V or 1.5V or 1.0 V, etc…
  - dimensions? weight?
  - we need a less naive powering scheme (CERN DC-DC converters, e.g.) – TBD
- 1 cooling tube
  - dimensions? weight? This is a problem we should know how to solve from past experience…

DAQ rates (from detector to DAQ)

- recap: assuming strip size of 500 um x 1 cm and total area 138000 cm2
  - ⇒ 2.8 million channels
- over 240 staves (aka fibers) ⇒ ~13000 channels (strips) per stave
- assume an average EIC event fires 150 TOF strips
  - 50 [5] particles, each hits 3 strips due to AC-LGAD charge sharing
- collision rate 500 kHz [6] ⇒ 75 Mhits/second (== 500k * 50 * 3)
  - ~32 bits per hit ⇒ 300 MB/second (not much really…)
    - BTW, 32 bits is likely too low → depends on the ASIC so TBD
  - with 240 staves (fibers) ⇒ ~1 MB/s of actual signal per fiber (==> trivial)
- but… noise…
  - no idea what is the noise of LGAD+ASIC but let's just invent 1 kHz [7] per channel
    - NOTE: this is a number we can tune/change, it depends on the ASIC discriminator threshold but I'm "inventing" a number here
  - 2.8 Mchannels x 1 kHz x 4 bytes ⇒ 11 GB/s of just noise (whoa!!!)
  - HOWEVER, over 240 fibers ⇒ 50 MB/s per fiber (not that much at all…)
- **Conclusion 1:** rates [could be? will be?] dominated by noise *but* we can easily ship all of this over our 240 fibers
- **Conclusion 2:** since we are **not rate limited** the number of fibers is mostly driven by the detector geometry and practicalities of the readout

Rates incoming into TOF DAQ PCs

- recap: 240 fibers each carrying 50 MB/s
  - data is <1 MB/s, noise is 50 MB/s
- assume the Receiver Board houses 24 fibers (e.g. ATLAS FELIX houses 48)
- 1 Receiver Board per “DAQ PC” connected over PCIe
  - ⇒ we need 10 DAQ PCs (not a particular problem)
  - ⇒ 1.2 GB/s per PC is not a problem either ⇒ e.g. *current* STAR TPC DAQ PCs analyze this rate
- Noise suppression in 2 stages
  - **stage 1:** remove single channels where the time info is obviously outside the RHIC crossing
    - assumed factor of 10 suppression
  - **stage 2:** 3D cluster finding: form clusters by requiring:
    - 2+ adjacent pixels (factor of 10 suppression)
    - all pixels in a cluster should have the same time value (another factor of 10 suppression)
      - ⇒ total factor of 100 suppression in Stage 2
    - BTW, similar algorithms already exist for the STAR TPC which operates a software 2D cluster finder at >1 GB/s per DAQ PC
  - **conclusion:** we assume we can reach a factor of 1000 noise suppression (similar existing systems/algorithms already perform at this rate)

Outgoing DAQ rates to the EVBs

- recap: 75 Mpixels/second total event rate over 10 DAQ PCs
  - 8 Mpixels/second into a DAQ PCs
- assume 3 pixels on average merge into a cluster
  - assume a cluster is 16 bytes (2 space coordinates, 1 time, total charge)
  - ⇒ 8 Mpixels/s / 3 ⇒ 3 Mclusters/s x 16 bytes ⇒ 48 MB/s per DAQ PC
    - can be shipped to EVBs over a single 1 Gbs ethernet link easily!
- *aggregate* TOF rate to DAQ EVBs (and tape) ⇒ 480 MB/s
  - it is not that much, HOWEVER we need to be good citizens and
    - see how this rate compares to other detectors within the Global DAQ
    - perhaps cut this down even more → TBD

Required numbers

#		Jun 2022 (this talk)	Jun+ 2022
1	count of Barrel Readout Modules (fibers)	160	
2	count of Endcap L Readout Modules (fibers)	30	
3	count of Endcap R Readout Modules (fibers)	50	
4	**strip size**	500 μm x 1cm	
5	particles in TOF per event (collision)	~50	
6	collision rate	500 kHz	
7	random noise per strip	1 kHz	

Higher Level Primitives

- What can we do with only TOF data in (pseudo)real time? What can be of use for the entire Collaboration? (just talking here…)
  - collision determination & charged particle counting; bunch crossing tagging
    - potentially very useful for e.g. Cherenkov detectors to suppress their SiPM noise
    - could be done in Receiver Board FPGAs and propagated to other detectors in real-time, over fiber?
  - vertexing – time difference between the 2 disks
    - assist simple online tracking?
    - assist the accelerator during setup?
  - time profile of the EIC beam
    - useful during commissioning and as a cross check of bunch patterns
    - potentially correlated with the spin pattern?
  - other?

Next steps

- reiterate all the numbers shown and get them into an agreed form defensible to the rest of the Collaboration
  - especially for the DAQ & Integration subgroups
  - BTW, I was asked to give a presentation to the DAQ Group on 6/14 where I plan to show these (or updated) numbers
- an AC-LGAD+ASIC slow simulator would be useful to have for the various noise suppression & clustering algorithms
- a realistic power distribution scheme should be designed (or at least strawmanned)
- a small prototype board (in progress) with
  - AC-LGAD + ASIC (EICROC but ALTIROC would also be OK now, on day-0)
  - FPGA driven, with *realistic clock cleaner PLLs* and other interfaces
  - external clock interface (e.g. using STAR's Clock Distribution boards would be fine)
  - standard fiber interfaces (no need for CERN rad-hard stuff for this)
  - Receiver Board & DAQ PC (we can use STAR's system)
  - make 2-3 of them and check them out with cosmics: resolution: time & space resolution, efficiency; noise; get experience with the chips
    - and jitter of a "realistic" clock
  - install them in STAR in one of the upcoming RHIC runs?
    - to get a flavor of a "real harsh environment" and really realistic clock jitter coming from RHIC etc

Conclusion

- need to a have more advanced mechanical design
  - and thus Readout Board design, fiber counting, power, cooling, material and other global services
  - iterative process but let's get going
- need better numbers related to DAQ
  - see table on Page 7
  - also needed for costing
- start small RDO prototypes with AC-LGAD & EICROC (as a final set)
  - but might consider various sensor prototypes & ALTIROC (and/or other ASICs?) for quicker progress
  - groups interested? resources available?
- work with Global DAQ on the clock distribution
  - crucial for TOF!
  - groups interested? resources available?
- work with Global DAQ on the fiber readout
  - I am assuming FPGAs but perhaps the decision will be lpGBT (from CERN) or something else?
  - groups interested? resources available?