# MPGD tracker frontend data

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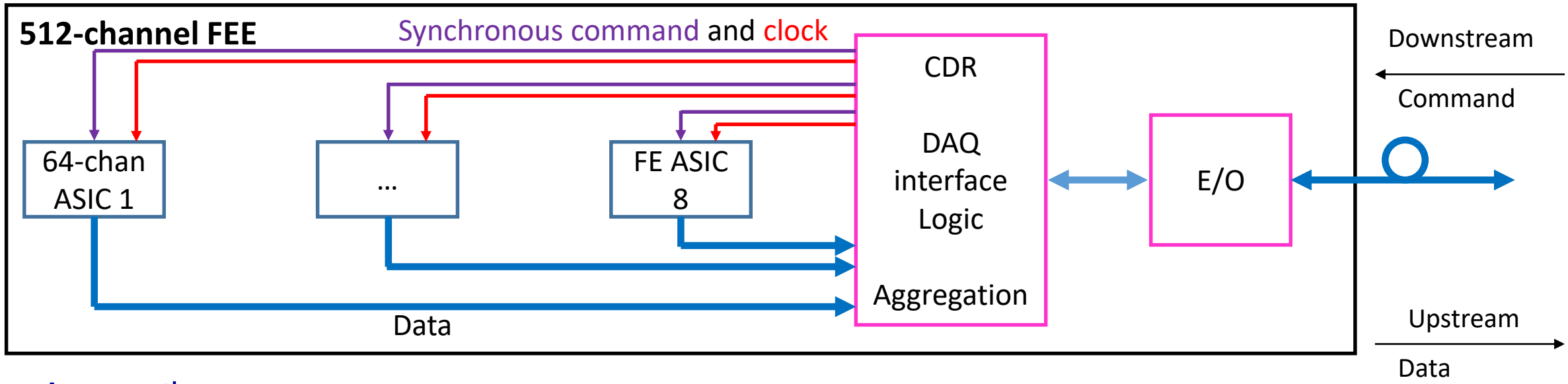
- Asses FEE output bandwidth
  - → Full readout
  - → ZS readout
  - → Calibration

# Frontend model

- A bi-directional optical link for clock, synchronization (run control), data, configuration
  - → Downstream: synchronous commands and slow control requests
    - Clock embedded into the serial bit-stream
  - → Upstream: acquisition data and slow control responses
  - → Several Gbit/s throughput




- Assumptions:
  - → 64-channel sampling ASIC
  - → 512-channel – 8-ASIC – frontend

# Continuous full readout – no ZS

- Assume
  - → 12-bit per sample
  - → 50 MSPS
  - → 10-20% overhead at ASIC and FEE levels
- 64-cannel ASIC data: ~45 Gbit/s
  - → 5 10 Gbit/s links
- 512-channel FEE data: ~420 Gbit/s
  - → 42 10 Gbit/s links
- Not a realistic option for steaming readout: ZS is needed
  - → Common mode noise subtraction, if needed, at FE ASIC level

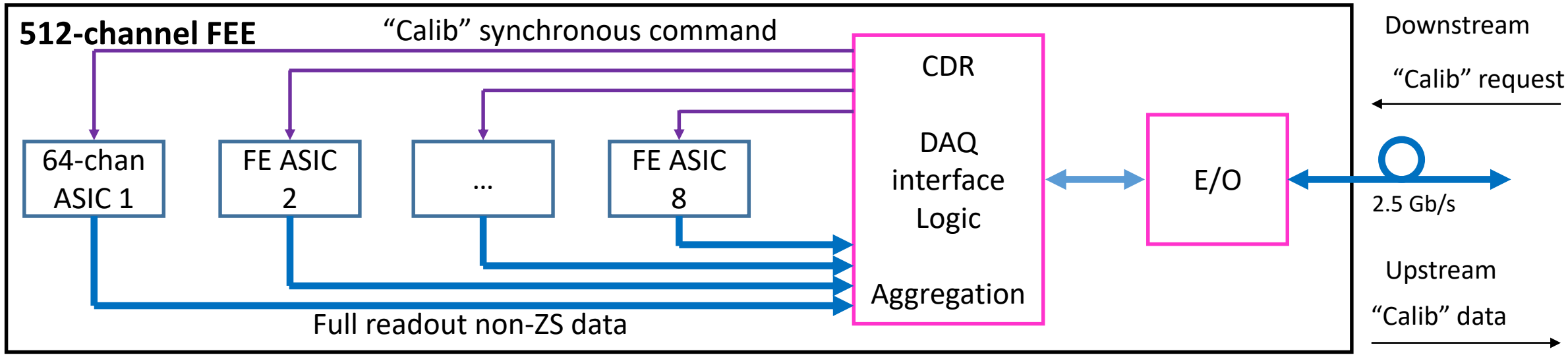
# Streaming ZS readout

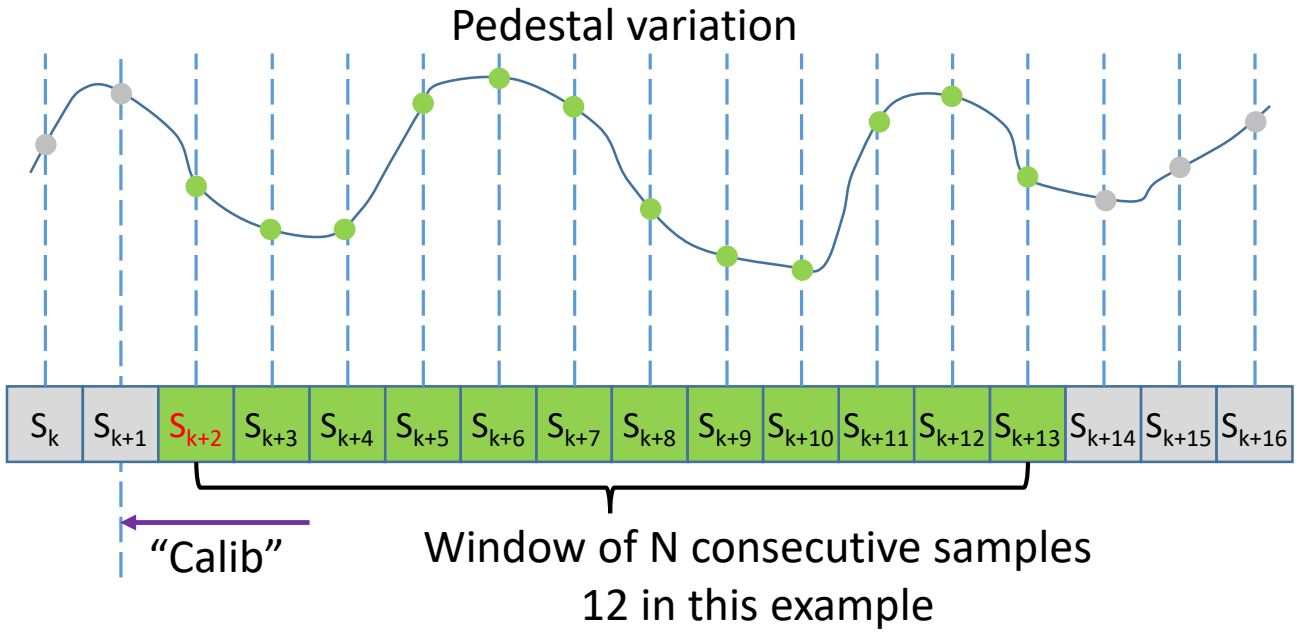
- Assume
  - → 12-bit per sample
  - → 50 MSPS
  - → 10-20% overhead at ASIC and FEE levels
- Signal shape ZS
  - → 500 ns readout window when signal is above threshold
    - 25 samples
- FEE link upstream bandwidth estimation
  - → for the Athena 66K-channel cylindrical Micromegas tracker

| Channel rate kHz | | 64-chanel ASIC Mbit/s | 512-chanel FEE Gbit/s | 50% loaded FE link |
|---|---|---|---|---|
| 2 | (physics) | 46 | 0.4 | 1 Gbit/s |
| **10** | **(safety)** | **230** | **1.9** | **4 Gbit/s** |
| 50 | (Clas12) | 1 150 | 9.5 | 20 Gbit/s |

- Data and bandwidth is significantly less for peak-finding (time-amplitude) readout
  - → 2 Gbit/s link for 50 kHz channel hit rate: see in backup
- Knowledge of channel occupancies (physics, background, noise) is important to optimize aggregation

# Calibration: Single “Calib” request – Window readout




- A “calib” request results in a Window readout
  - → N consecutive samples
  - → Full readout of non-ZS data
    - All channels of all ASICs
  - → Window size programmable
    - Probably same as for ZS readout
      - e.g. able to contain a typical signal shape

More details in backup

# Calibration: full readout on request

- Assume
  - → 12-bit per sample
  - → 50 MSPS
  - → 10-20% overhead at ASIC and FEE levels

- Calibration sequence
  - → 1000 “Calib” commands to FEE at some pace
  - → 1 µs (50-sample) window readout
    - This results to 50k non-ZS samples (1000 x 50) acquired for each channel
  - → See further details in backup

- Questions and answers
  - → What is the FEE calibration data size? ~55 Mbyte
  - → What is the min calibration time? ~265 ms

  - → If DAQ sends “Calib” commands at 100 Hz pace
    - What will be calibration cycle duration? 10 secs
    - What will be occupancy of the 2.5 Gbit/s upstream link due to the calibration data: 2%

- FEE calibration data are small and do not influence the choice of the FEE output link bandwidth
  - → Under the assumptions – even though they are not very favorable
    - An Excel spreadsheet shared to test different assumptions

# Summary for MPGD tracker

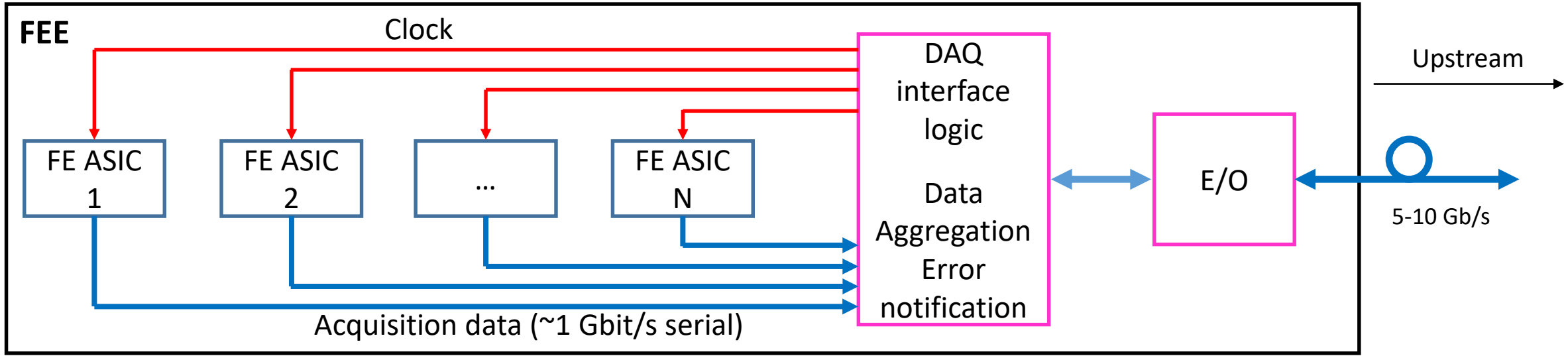
- Full readout is not an option for streaming readout
  → ASIC-level ZS is necessary

- FEE upstream bandwidth seems to be determined by physics run needs
  → Knowledge of channel occupancies is important to conceive aggregation
    - Physics, background, noise
  → Power-hangry aggregation in “buried” frontend might be penalizing

- Calibration data seem to be small and do not influence the choice of the FEE output link bandwidth
  → Perform estimations with existing ASICs: Sampa, VMM
    - Understand the achievable calibration protocol
  → Collect similar information from all sub-detector groups
    - Not only a pedestal run, but may require, for example, *in-situ* calibration runs to improve INL of TDCs

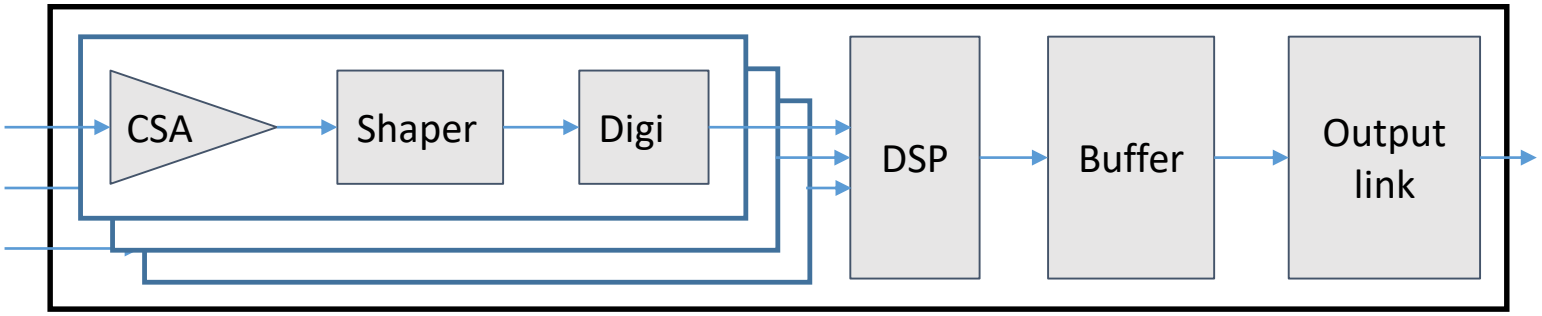
# Backup: Full readout

# Data


FEE
Clock
FE ASIC 1
FE ASIC 2
...
FE ASIC N
DAQ interface logic
Data Aggregation
Error notification
Acquisition data (~1 Gbit/s serial)
E/O
Upstream
5-10 Gb/s

# Example of a multi-channel ASIC for MPGD tracker

- FEE based on multi-channel MPGD ASICs
  - → Compatible with streaming readout
  - → Typical characteristics
    - Gain: 10 down to 4 mV/fC
    - Peaking time: 75 to 300 ns
    - Detector capacitance: up to 400 pF
    - 10-12 bit ADC; 10-20 ns timing




  - → On-chip zero suppression
    - Possibly with common mode noise subtraction
    - Peak finding ZS: amplitude, time and ToT
    - Sampling ZS: signal shape around ToT
    - "Region of interest" ZS: if a strip exceeds a high threshold, forced or lower threshold reading of its neighbors

- ASICs
  - → 64-channel peak finding VMM3a
  - → 32-channel sampling Sampa
  - → Next generation 64-channel sampling Salsa
    - On-going initiative of Brazilian institutes (Sampa) and Irfu (AGET, Dream)
    - See for example: https://indico.cern.ch/event/1040996/contributions/4402636/

# MPGD ASIC data rate: ZS and common mode noise

- Assume a 64-channel sampling ASIC with 12-bit sample per channel
- Full readout of the ASIC - no ZS
  → 50 MSPS: 50 Gbit/s (including 20% overhead)
  Not a realistic option: ZS is needed

- Coherent noise subtraction
  → Based on dedicated CMN channels in ASIC not connected to detector
    - Evaluates noise in chip / board but not coming from detector (and detector interconnect – e.g. cables)
  → Based on group of channels connected to consecutive detector strips
    - External to chip in streaming readout: move 25-50 Gbit/s data out of chip
    - External to chip in triggered readout: doable

  → If needed, perform coherent noise removal on chip prior to ZS

  What about *in-situ* detector studies when full readout is necessary?
  At low frequency with a dedicated “trigger” command? In a pre-scale mode?
  Should not be overlooked when building the DAQ system

# Backup: ZS readout

# MPGD FEE data rate: sampling readout

- Sampling ASIC with 12-bit sample per channel
- Signal shape ZS
  → 500 ns readout window when signal is above threshold

- 64-channel ASIC (e.g. Salsa) and 512-channel FEE with 8 ASICs

| Channel rate kHz | | Sampling MSPS | Number of samples | 64-chanel ASIC Mbit/s | 512-chanel FEE Gbit/s | Remarks |
|---|---|---|---|---|---|---|
| 2 | (physics) | 50 | 25 | 46 | 0.4 | 5-10 Gbit/s aggregation link unjustified |
| **10** | **(safety)** | | | **230** | **1.9** | **5 Gbit/s aggregation link is enough** |
| 50 | (Clas12) | | | 1 150 | 9.5 | 20 Gbit/s aggregation link needed |

- 32-channel (Sampa) based 256-channel FEE
  → 5-10 Gbit/s link can be justified for 50 kHz channel hit rates
  - See in backup

# MPGD FEE data rate: peak-finding readout

- Peak-finding ASIC
- ZS with time-amplitude readout
  → Assume 12-bit timing, 8-bit ToT and 12-bit amplitude

- 64-channel ASIC (e.g. VMM3a)  and 512-channel FEE with 8 ASICs
  → Or a new development

| Channel rate kHz | 64-chanel ASIC Mbit/s | 512-chanel FEB Gbit/s | Remarks |
|---|---|---|---|
| 2 (physics) | 5 | 0.04 | 5-10 Gbit/s aggregation link unjustified |
| **10 (safety)** | **25** | **0.2** | |
| 50 (Clas12) | 125 | 1 | 2 Gbit/s aggregation link is enough |

- Knowledge of channel occupancies (physics, background, noise) is important to optimize aggregation

Is it acceptable to have an important number of high rate links frankly underused?
*e.g.* power, cost
Is it worth to complicate system adjusting link speeds?
*e.g.* 2-stage aggregation, cost

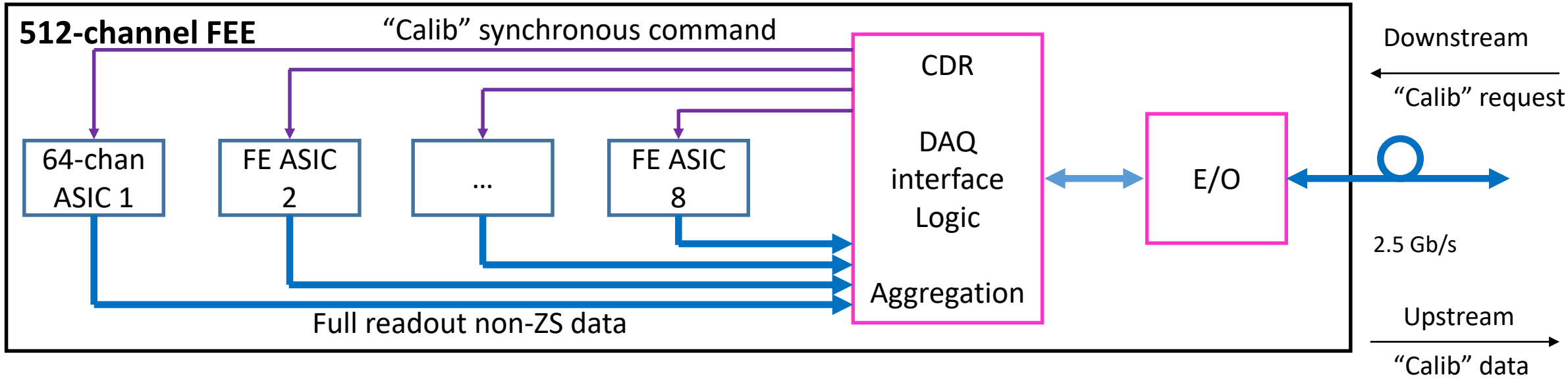
# Backup: Calibration

# Goal, caution and conclusion

- Asses FEE output bandwidth needed for calibration
  - → Do the FEE calibration data influence the choice of the FEE output link bandwidth?
    - As a by product asses FEE and ASIC de-randomization buffer increase due to calibration
- Make some assumptions on
  - → FEE and FE ASIC operation
  - → Calibration sequence
- Though not definitive, the assumptions give a good idea about the expected calibration data volumes
  - → Typical calibration consists of taking non-ZS data to evaluate detector pedestals, noise and ZS thresholds
- A particular set of parameters is considered
  - → The set is deliberately chosen with not favorable parameters
    - e.g. low FEE output link speed, large number of samples
  - → An Excel file is shared for verification and for playing with the parameters
- Conclusions: under the posed assumptions the FEE calibration data are small and do not influence the choice of the FEE output link bandwidth

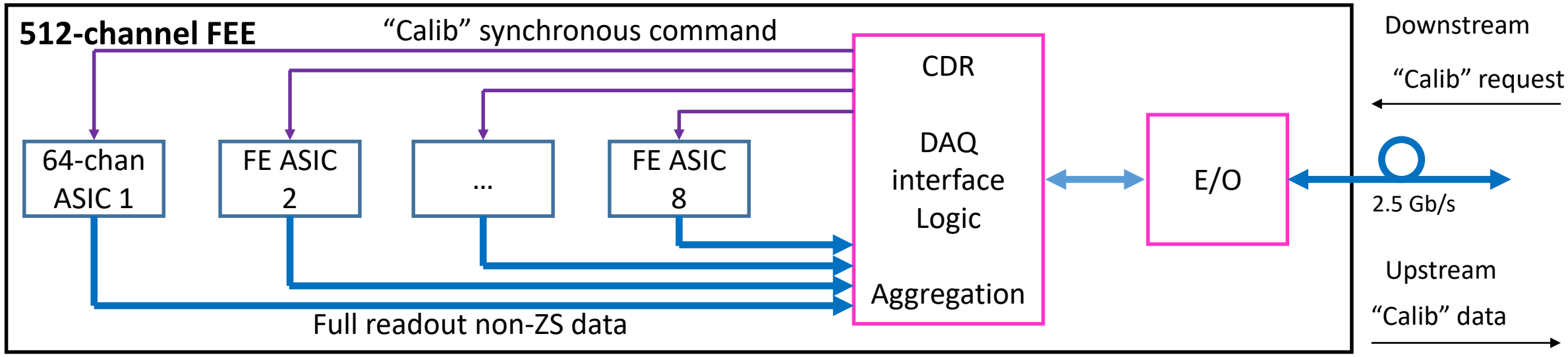
# Calibration request and response

- DAQ sends calibration request to FEE
- FEE conveys calibration request to on-board ASICs
- FEE collects non-ZS calibration data from ASICs
- FEE forms calibration packet and sends it to DAQ

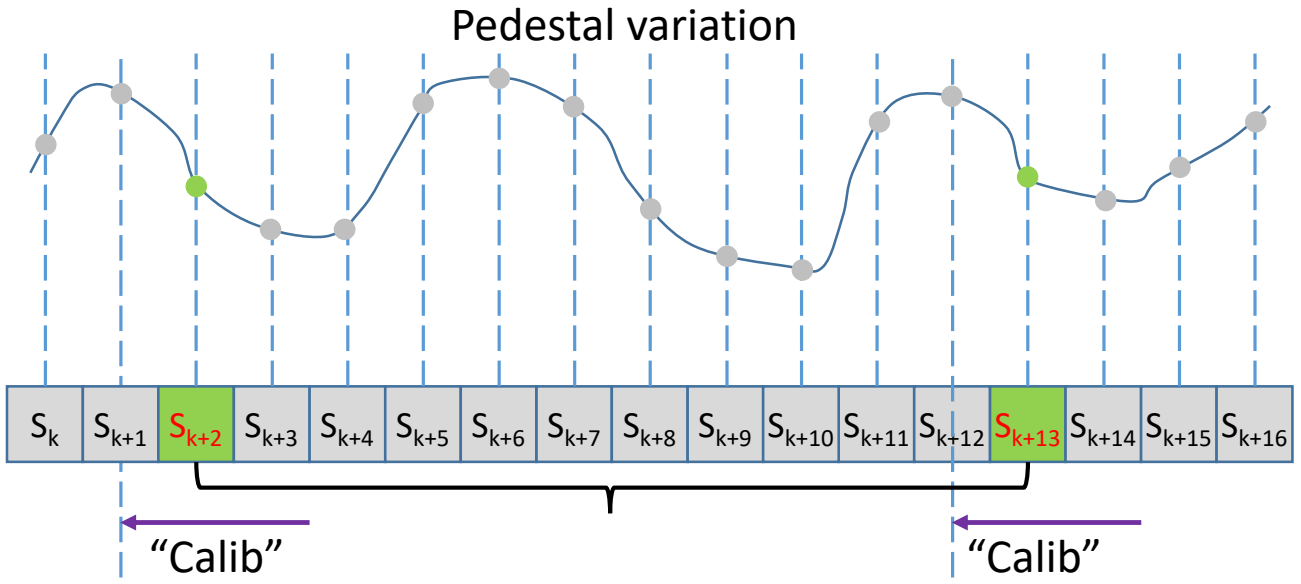



- This sequence repeats programmable number of times to form a complete calibration cycle
- Two calibration types are considered and one of them evaluated

# Calibration type: Single “Calib” request – Single Sample readout

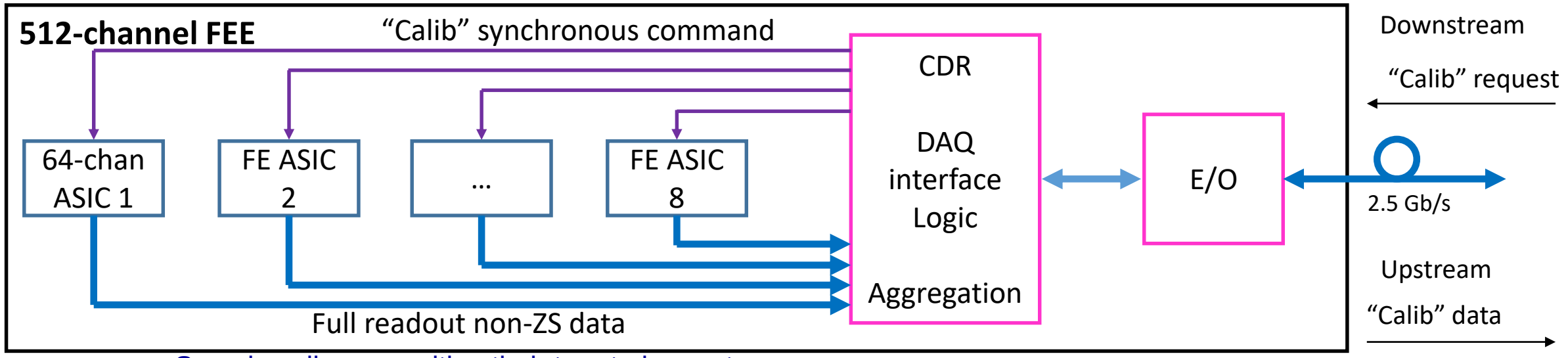



- Determined by ASIC output throughput

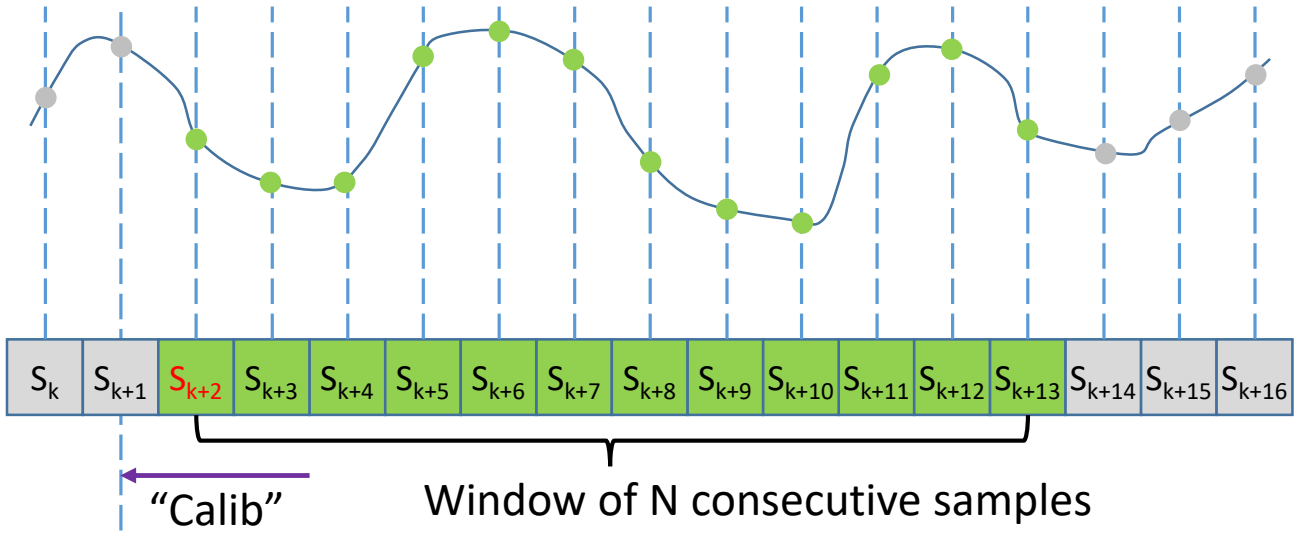



- A “calib” request results to one sample readout
  - → Full readout of non-ZS data
    - All channels of all ASICs
  - → “Calib” request frequency set by DAQ
  - → Consecutive samples cannot be read
    - Unless “Calib” requests pipelined
  - → Needs smaller de-randomizer buffers in ASICs
    - Absorb eventual ZS samples awaiting their turn to be sent
      - Determined by ASIC output throughput

# Calibration type: Single “Calib” request – Window readout



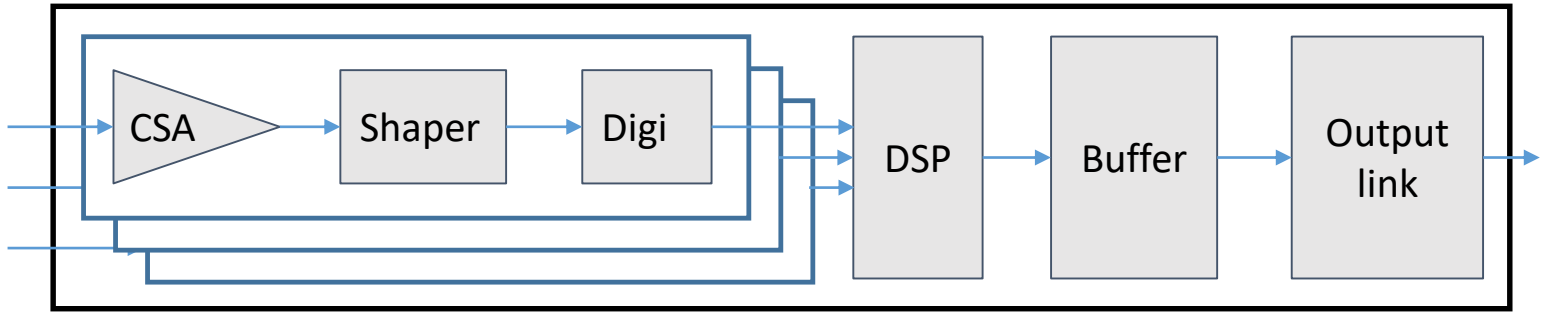

- Samples pile up awaiting their turn to be sent
  - Determined by ASIC output throughput



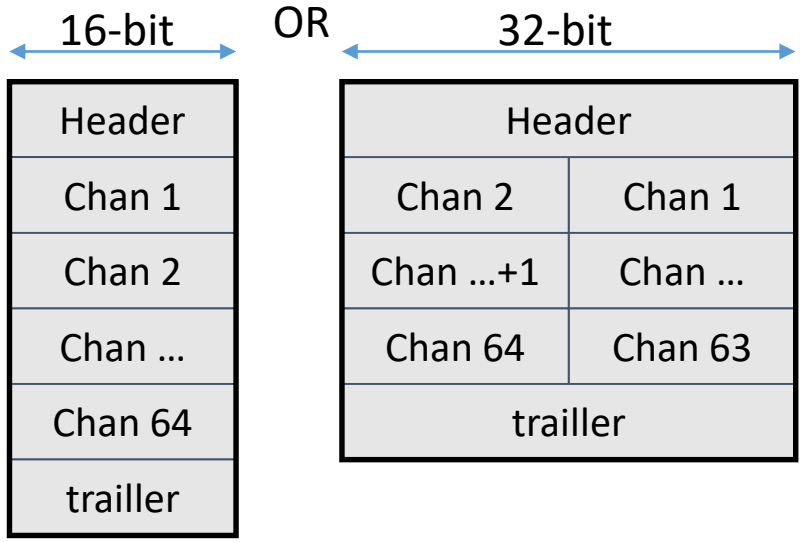

- A “calib” request results to one sample readout
  - → Full readout of non-ZS data
    - All channels of all ASICs
  - → “Calib” request frequency set by DAQ
  - → Consecutive samples cannot be read
    - Unless “Calib” requests pipelined
  - → Needs smaller de-randomizer buffers in ASICs
    - Absorb eventual ZS samples awaiting their turn to be sent
      - Determined by ASIC output throughput

# 64-channel ASIC for MPGD tracker

- ASIC characteristics relevant for calibration
  - → 64 channels
  - → 50 MSPS sampling frequency
  - → 12-bit ADC encoded over 16 bits
  - → 64-bit data overhead
    - Header and trailer
  - → 1 Gbit/s link speed

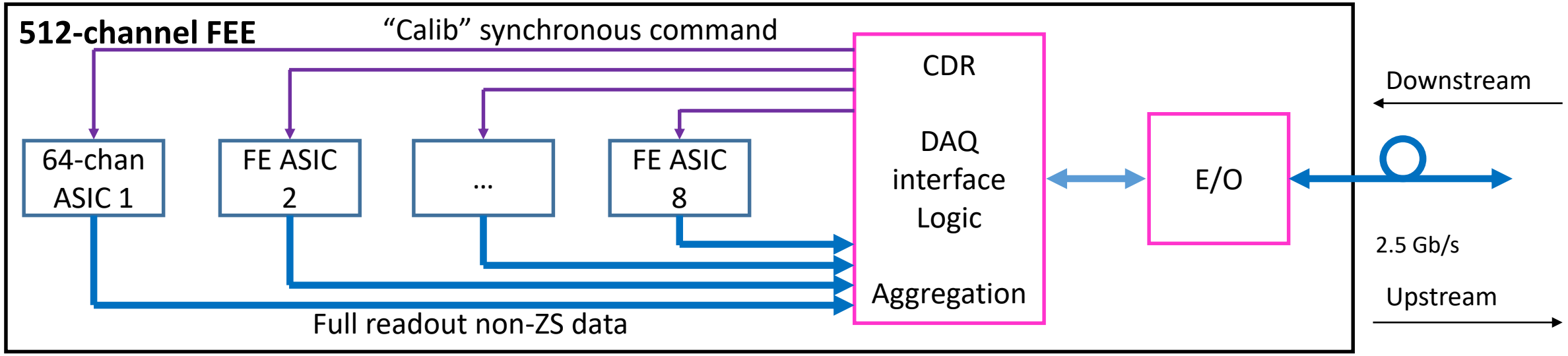



- ASIC full readout data for a sample
  - → Size: 1 088 bit = 136 bytes
    - 64 channels x 16-bit + 64-bit overhead
  - → TX time: 1.088 µs
    - 1 088 bit / 1 Gbit/s
    - 54.4 samples




- ASIC ZS de-randomizing buffer to be augmented by
  - → For single sample readout: as many extra samples as possible “calib” requests within 1.088 µs TX time
  - → For window readout: 1.088 µs * 50 MSPS = 54.4 samples
    - Per channel: 880 bits
    - ASIC: 64 x 880 = 55 Kbits

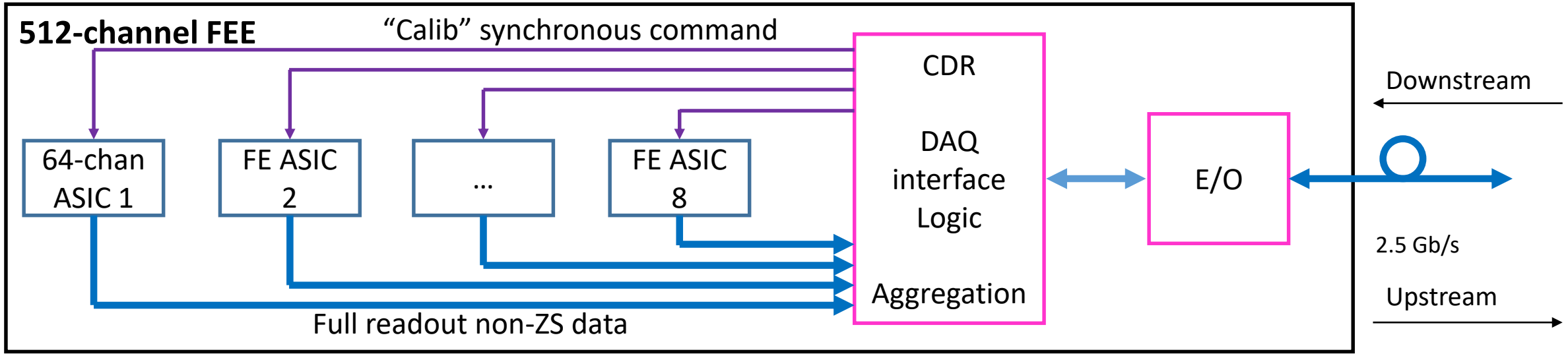
# 512-channel FEE




- FEE characteristics relevant for calibration
  - → 8 64-channel ASICs
  - → 256-bit data overhead
    - Header and trailer
  - → 2.5 Gbit/s link speed
    - 20% transport overhead e.g. 8b/10b encoding
  - → 1 µs pause forced between consecutive calibration packets
- FEE full readout data for a sample
  - → Size : 8.75 Kbit = 1.09 Kbytes
    - 8 ASICs x 1088 bit + 256-bit overhead
  - → TX time : 4.3 µs
    - (8.75 + 20% transport overhead) Kbit / 2.5 Gbit/s

| Header |
|---|
| ASIC 1: 1088 bits |
| ASIC 2: 1088 bits |
| ASIC …: 1088 bits |
| ASIC 8: 1088 bits |
| Trailer |

# 512-channel FEE




- FEE ZS de-randomizing buffer to be augmented by
  - → For single sample readout: as many extra samples as possible "calib" requests within 4.3 µs "calib" data packet sending time
  - → For window readout: ~5 sample
    - (4.3 µs + 1 µs) / 1.088 µs
      - (FEE calib data send time + forced pause) / ASIC calib data receive time)
    - Per ASIC: 5.3 Kbit = 680 byte
      - 5 x 1088 bit of ASIC calib sample size
    - FEE: ~44 Kbit = 5.5 Kbyte
      - 5 x 8.75 of FEE calib packet size

| Header |
|---|
| ASIC 1: 1088 bits |
| ASIC 2: 1088 bits |
| ASIC …: 1088 bits |
| ASIC 8: 1088 bits |
| Trailer |

# Recapitulating the hypothesis

- Pedestal run consists of 1000 acquisition of 1 µs readout windows without ZS
  - → All channels of a FEE are read and sent to off-detector backend electronics
- A 512-channel FEE is composed of 8 64-channel MPGD front-end ASICs
- The 64-channel front-end ASIC is a sampling chip
  - → Sampling rate is 50 GSPS
  - → Channel ADC has 12 bits, but the channel data are sent as a 16-bit word
    - 12 bit ADC value + 4 bit encoding
  - → For each sample all 64 channels are read: 64 x 16-bit
  - → An ASIC overhead of 64 bits is added to the ASIC channel data
    - ASIC header + ASIC trailer
- For each sample FEE transmits the data of 8 ASICs and adds 256-byte overhead
  - → FEE header and trailer
  - → 256 + 8 x (64 + 64 x 16) bits
- FEE upstream link throughput is 2.5 Gbit/s
  - → Transport layer overhead is 20%
    - For example, 8b/10b encoding is used: for every 8 bits of user data 10 bits are transmitted
- FEE respects 1 µs pause between two successive calibration packets
- 1 µs Readout window corresponds to 50 samples at 50 GSPS rate
  - → For each readout window 50 consecutive samples are read

# Window-readout calibration sequence

- Assume the following calibration protocol
  - → To send all samples forming a readout window the FEE needs to receive a single “Calib” command over the downstream link
    - Upon reception of the “Calib” command the FEE performs 50 times the following
      - Sends “calib” command to all ASICs
      - Collects “calib” data from all ASICS
      - Forms data packet containing data of all ASICs and its own overhead
      - Sends the packet over the upstream link
      - Observes 1 µs idle time to let backend electronics to do some housekeeping
  - → To perform complete calibration cycle the DAQ sends 1000 “Calib” commands to FEE at some pace
    - This results to 50k non-ZS samples (1000 x 50) acquired for each channel

- Questions and answers
  - → What is the FEE calibration data size? ~53.4 Mbyte
  - → What is the min calibration time? ~265 ms

  - → If DAQ sends “Calib” commands at 100 Hz pace
    - What will be calibration cycle duration? 10 secs
    - What will be occupancy of the 2.5 Gbit/s upstream link due to the calibration data: 2%

- Conclusions: under these assumptions the FEE calibration data are small and do not influence the choice of the FEE output link bandwidth